

TOSHIBA



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Static RAM

1 9 9 4

DATA BOOK

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

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TOSHIBA

Static RAM
1994

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Standard Static RAM

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High Speed Static RAM

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Package: P = Plastic DIP, F = Flat package (SOP), SP = Slim Plastic DIP, FW = Flat Wide package
 FT = Forward bend TSOP, TR = Reverse bend TSOP, J = SOJ

High Speed Synchronous Static RAM

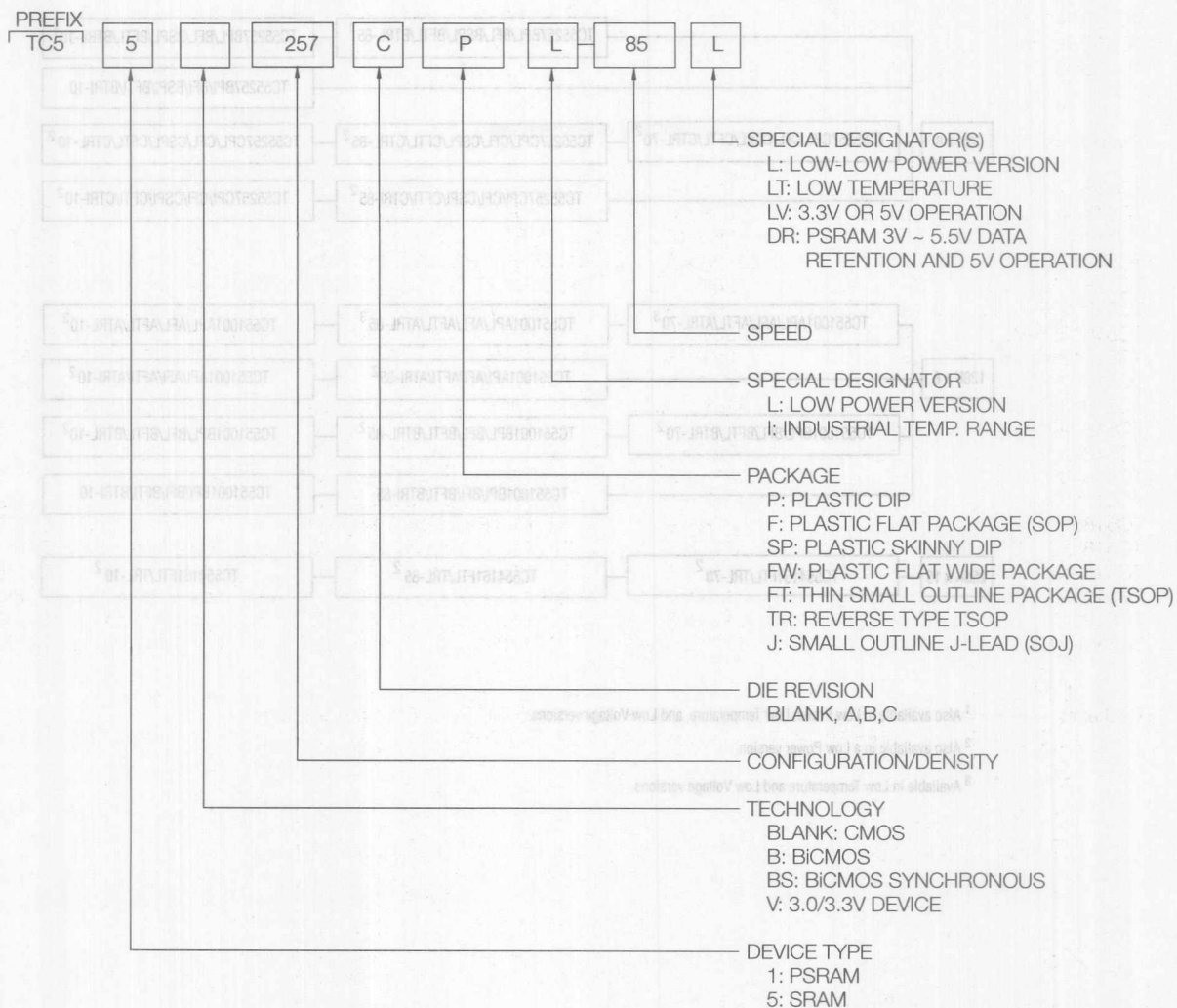
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Pseudo Static RAM

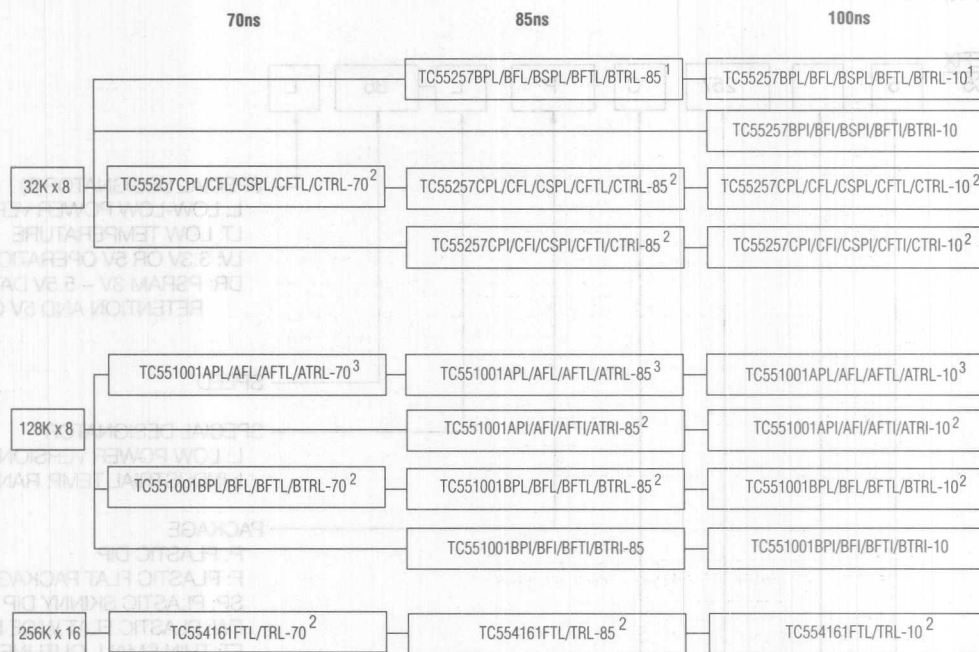
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TC51V8512A	4M	512K x 8	F, FT, TR	120, 150	3V Operation	D-205

Package: P = Plastic DIP, F = Flat package (SOP), SP = Slim Plastic DIP, FW = Flat Wide package
FT = Forward bend TSOP, TR = Reverse bend TSOP, J = SOJ

SRAM/PSRAM PART NUMBER GUIDE



Standard Static RAM



¹ Also available in Low Power, Low Temperature, and Low Voltage versions.

² Also available in a Low Power version.

³ Available in Low Temperature and Low Voltage versions.

High Speed Static RAM

		10ns/12ns	15ns	20ns	25ns	30ns/35ns
CMOS	8K x 8		TC5588P/J-15	TC5588P/J-20	TC5588P/J-25	TC5588P/J-35
	8K x 9		TC5589P/J-15	TC5589P/J-20	TC5589P/J-25	TC5589P/J-35
	64K x 4		TC55464AP/AJ-15	TC55464AP/AJ-20	TC55464AP/AJ-25	TC55464AP/AJ-35
			TC55465AP/AJ-15	TC55465AP/AJ-20	TC55465AP/AJ-25	TC55465AP/AJ-35
	32K x 8		TC55328AP/AJ-15	TC55328AP/AJ-20	TC55328AP/AJ-25	TC55328AP/AJ-35
				TC55V328J-20	TC55V328J-25	TC55V328J-35
	32K x 9		TC55329AP/AJ-15	TC55329AP/AJ-20	TC55329AP/AJ-25	TC55329AP/AJ-35
	32K x 16			TC551632J-20	TC551632J-25	TC551632J-35
	64K x 16		TC551664J-15	TC551664J-20	TC551664J-25	
		TC55V1664J/FT-10/12	TC55V1664J/FT-15			
	64K x 18	TC55V1864J/FT-10/12	TC55V1864J/FT-15			
	4M x 1/ 1M x 4			TC551402J-20	TC551402J-25	TC551402J-30
	1M x 4			TC554101J-20	TC554101J-25	TC554101J-30
BiCMOS	8K x 8	TC55B88P/J-10/12				
	64K x 4	TC55B464P/J-10/12				
		TC55B465P/J-10/12				
	32K x 8	TC55B328P/J-10/12				
	32K x 9	TC55B329P/J-10/12				
	256K x 4	TC55B4256J-12	TC55B4256J-15	TC55B4256J-20		
		TC55B4257J-12	TC55B4257J-15	TC55B4257J-20		
		TC55BS4258J-10/12				
	128K x 8	TC55B8128P/J-12	TC55B8128P/J-15	TC55B8128P/J-20		
		TC55BS8125J-10/12				
		TC55BS8128J-10/12				

Pseudo Static RAM

	70ns	80ns/85ns	100ns	120/150ns
32K x 8	TC51832AP/AF/ASP-70 TC51832APL/AF/ASPL-70	TC51832AP/AF/ASP-85 TC51832APL/AF/ASPL-85	TC51832AP/AF/ASP-10 TC51832APL/AF/ASPL-10	
64K x 8		TC51864PL/FL-85	TC51864PL/FL-10	
32K x 16	TC511632FL/FTL-70	TC511632FL/FTL-85	TC511632FL/FTL-10	
		TC518128AP/AF/ASP/AFW-80 ¹ TC518128APL/AF/ASPL/AFWL/AFTL-80 ¹	TC518128AP/AF/ASP/AFW-10 ¹ TC518128APL/AF/ASPL/AFWL/AFTL-10 ¹	TC518128AP/AF/ASP/AFW-12 ¹ TC518128APL/AF/ASPL/AFWL/AFTL-12 ¹
	TC518128BPL/BFL/BSPL/BFWL/BFTL-70 ¹ TC518128BPL/BFL/BSPL/BFWL/BFTL-70L	TC518128BPL/BFL/BSPL/BFWL/BFTL-80 ¹ TC518128BPL/BFL/BSPL/BFWL/BFTL-80L	TC518128BPL/BFL/BSPL/BFWL/BFTL-10 ¹ TC518128BPL/BFL/BSPL/BFWL/BFTL-10L	
	TC518128CPL/CFL/CSPL/CFWL/CFTL-70 TC518128CPL/CFL/CSPL/CFWL/CFTL-70L	TC518128CPL/CFL/CSPL/CFWL/CFTL-80 TC518128CPL/CFL/CSPL/CFWL/CFTL-80L	TC518128CPL/CFL/CSPL/CFWL/CFTL-10 TC518128CPL/CFL/CSPL/CFWL/CFTL-10L	
128K x 8		TC518129AP/AF/ASP/AFW-80 ¹ TC518129APL/AF/ASPL/AFWL/AFTL-80 ¹	TC518129AP/AF/ASP/AFW-10 ¹ TC518129APL/AF/ASPL/AFWL/AFTL-10 ¹	TC518129AP/AF/ASP/AFW-12 ¹ TC518129APL/AF/ASPL/AFWL/AFTL-12 ¹
		TC518129AFWI-10		
	TC518129BPL/BFL/BSPL/BFWL/BFTL-70 ¹ TC518129BPL/BFL/BSPL/BFWL/BFTL-70L	TC518129BPL/BFL/BSPL/BFWL/BFTL-80 ¹ TC518129BPL/BFL/BSPL/BFWL/BFTL-80L	TC518129BPL/BFL/BSPL/BFWL/BFTL-10 ¹ TC518129BPL/BFL/BSPL/BFWL/BFTL-10L	
	TC518129CPL/CFL/CSPL/CFWL/CFTL-70 TC518129CPL/CFL/CSPL/CFWL/CFTL-70L	TC518129CPL/CFL/CSPL/CFWL/CFTL-80 TC518129CPL/CFL/CSPL/CFWL/CFTL-80L	TC518129CPL/CFL/CSPL/CFWL/CFTL-10 TC518129CPL/CFL/CSPL/CFWL/CFTL-10L	
	TC518512PL/FL/FTL/TRL-70 ²	TC518512PL/FL/FTL/TRL-80 ²	TC518512PL/FL/FTL/TRL-10 ²	
512K x 8		TC518512PI/FI-80	TC518512PI/FI-10	
				TC51V8512AF/AFT/ATR-12/15

¹ Also available in Low Voltage version.

² Also available in Low Temperature, Data Retention, and Low Voltage versions.

Standard Static RAM (256K)

ORGANIZATION	32K x 8, 28-pin				
PACKAGE WIDTH	0.6 INCH DIP	0.45 INCH SOP	0.3 INCH DIP	8 x 13.4mm TYPE I TSOP (Forward)	8 x 13.4mm TYPE I TSOP (Reverse)
TOSHIBA	TC55257CP	TC55257CF	TC55257CSP	TC55257CFT	TC55257CTR
Cypress					
Fujitsu	MB84256A-P	MB84256A-PF	MB84256A-PSK	MB84256A-PFTN	MB84256A-PFTR
Hitachi	HM62256AP	HM62256AFP	HM62256ASP		
Micron					
Mitsubishi	M5M5256CP	M5M5256CFP	M5M5256CKP	M5M5256CVP	M5M5256CRV
Motorola					
NEC	μ PD43256BCZ	μ PD43256BGU			
Samsung	KM62256BLP	KM62256BLG	KM62256BLS	KM62256BLTG	KM62256BLRG
Sharp	LH52B256 LH51256L	LH52B256N LH51256LN	LH52B256D	LH52B256T	LH52B256TR
Sony	CXK58257AP	CXK58257AM	CXK58257ASP	CXK58257ATM	CXK58257AYM

Standard Static RAM (1M)

ORGANIZATION	128K x 8, 32-pin			
PACKAGE WIDTH	0.6 INCH DIP	0.525 INCH SOP	8 x 20mm TYPE I TSOP (Forward)	8 x 20mm TYPE I TSOP (Reverse)
TOSHIBA	TC551001BP	TC551001BF	TC551001BFT	TC551001BTR
Cypress				
Fujitsu	MB841000-P	MB841000-PF		
Hitachi	HM628128ALP	HM628128ALFP	HM628128ALT	HM628128ALR
Micron				
Mitsubishi	M5M51008AP	M5M51008AFP	M5M51008AVP	M5M51008ARV
Motorola				
NEC	μ PD431000ACZ	μ PD431000AGW	μ PD431000AGZ	μ PD431000AGZM
Samsung	KM681000BLP	KM681000BLG	KM681000BLT	KM681000BLR
Sharp				
Sony	CXK581000P	CXK581000M	CXK581000TM	CXK581000YM

High Speed CMOS/BiCMOS Static RAM (64K)

ORGANIZATION	8K x 8, 28-pin			
PACKAGE WIDTH	0.3 INCH DIP	0.3 INCH SOJ	0.3 INCH DIP	0.3 INCH SOJ
TOSHIBA	TC5588P	TC5588J	TC55B88P	TC55B88J
Cypress	CY7B185-PC CY7C185-PC	CY7B185-VC CY7C185-VC	CY7B185-PC CY7C185-PC	CY7B185-VC CY7C185-VC
Fujitsu	MB81C78A-PSK	MB81C78A-PJ		
Hitachi				
Micron	MT5C6408	MT5C6408DJ	MT5C6408	MT5C6408DJ
Mitsubishi	M5M5178BP	M5M5178BJ		
Motorola	MCM6264CP	MCM6264CJ	MCM6264CP	MCM6264CJ
NEC	μ PD4368CR	μ PD4368LA		
Samsung	KM6865BP	KM6865BJ	KM6865BP	KM6865BJ
Sharp				
Sony	CXK5866P CXK5863BP	CXK5866J CXK5863BJ		

High Speed CMOS Static RAM (72K)

ORGANIZATION	8K x 9, 28-pin	
PACKAGE WIDTH	0.3 INCH DIP	0.3 INCH SOJ
TOSHIBA	TC5589P	TC5589J
Cypress	CY7C182-PC	CY7C182-VC
Fujitsu	MB81C79A-PSK	MB81C79A-PJ
Hitachi		
Micron		
Mitsubishi	M5M5179BP	M5M5179BJ
Motorola	MCM6265CP	MCM6265CJ
NEC	μ PD4369CR	μ PD4369LA
Samsung		
Sharp		
Sony	CXK5972P CXK5971AP	CXK5972J CXK5971AJ

High Speed CMOS/BiCMOS Static RAM (256K)

ORGANIZATION	64K x 4, 24-pin			
PACKAGE WIDTH	0.3 INCH DIP	0.3 INCH SOJ	0.3 INCH DIP	0.3 INCH SOJ
TOSHIBA	TC55464AP	TC55464AJ	TC55B464P	TC55B464J
Cypress	CY7B194-PC CY7C194-PC	CY7C194-VC	CY7B194-PC CY7C194-PC	CY7C194-VC
Fujitsu	MB81C84A-PSK	MB81C84A-PJ		
Hitachi	HM6208HP	HM6208HJP		HM6708SHJP
Micron	MT5C2564	MT5C2564DJ	MT5C2564	MT5C2564DJ
Mitsubishi	M5M5258CP	M5M5258CJ		
Motorola	MCM6208CP	MCM6208CJ	MCM6208CP	MCM6708AJ MCM6208CJ
NEC	μ PD43254BCR	μ PD43254BLA		
Samsung				
Sharp	LH52252AD	LH52252AK		
Sony				

High Speed CMOS/BiCMOS Static RAM (256K)

ORGANIZATION	64K x 4, 28-pin (OE)			
PACKAGE WIDTH	0.3 INCH DIP	0.3 INCH SOJ	0.3 INCH DIP	0.3 INCH SOJ
TOSHIBA	TC55465AP	TC55465AJ	TC55B465P	TC55B465J
Cypress	CY7B195-PC CY7C195-PC	CY7B195-VC CY7C195-VC	CY7B195-PC CY7C195-PC	CY7B195-VC CY7C195-VC
Fujitsu	MB82B85-PSK	MB82B85-PJ		
Hitachi				HM6709SHJP
Micron	MT5C2565	MT5C2565DJ	MT5C2565	MT5C2565DJ
Mitsubishi	M5M5259CP	M5M5259CJ		
Motorola	MCM6209CP	MCM6209CJ	MCM6209CP	MCM6709AJ MCM6209CJ
NEC	μ PD43253BCR	μ PD43253BLA		
Samsung	KM64258BP	KM64258BJ		KM64B258AJ
Sharp	LH52253D	LH52253K		
Sony				

High Speed CMOS/BiCMOS Static RAM (256K)

ORGANIZATION	32K x 8, 28-pin				
PACKAGE WIDTH	0.3 INCH DIP	0.3 INCH SOJ	0.3 INCH DIP	0.3 INCH SOJ	0.3 INCH SOJ (3.3V)
TOSHIBA	TC55328AP	TC55328AJ	TC55B328P	TC55B328J	TC55V328J
Cypress	CY7B199-PC CY7C199-PC	CY7B199-VC CY7C199-VC	CY7B199-PC CY7C199-PC	CY7B199-VC CY7C199-VC	CY7C1399-VC
Fujitsu	MB8298-PSK	MB8298-PJ			
Hitachi	HM62832UHP	HM62832UHJP		HM67832SHJP	HM62W832
Micron	MT5C2568	MT5C2568DJ	MT5C2568	MT5C2568DJ	MT5LC2568DJ
Mitsubishi	M5M5278CP	M5M5278CJ		M5M52B78AJ	
Motorola	MCM6206DP	MCM6206DJ	MCM6206DP	MCM6706AJ MCM6206DJ	MCM62V06DJ
NEC	μ PD43258ACR	μ PD43258ALA			
Samsung	KM68257BP	KM68257BJ		KM68B257AJ	KM68V257J
Sharp	LH52258AD	LH52258AK			
Sony	CXK58258BP	CXK58258BJ			

High Speed CMOS/BiCMOS Static RAM (288K)

ORGANIZATION	32K x 9, 32-pin			
PACKAGE WIDTH	0.3 INCH DIP	0.3 INCH SOJ	0.3 INCH DIP	0.3 INCH SOJ
TOSHIBA	TC55329AP	TC55329AJ	TC55B329P	TC55B329J
Cypress	CY7C188-PC	CY7C188-VC	CY7C188-PC	CY7C188-VC
Fujitsu	MB8299-PSK	MB8299-PJ		
Hitachi				
Micron				
Mitsubishi	M5M5279P	M5M5279J		M5M52B79J
Motorola		MCM6205DJ		MCM6705AJ
NEC	μ PD43259ACR	μ PD43259ALA		
Samsung				KM69B257AJ
Sharp				
Sony	CXK59288P	CXK59288J		

High Speed CMOS Static RAM (512K)

ORGANIZATION	32K x 16, 40-pin
PACKAGE WIDTH	0.4 INCH SOJ
TOSHIBA	TC551632J
Cypress	
Fujitsu	
Hitachi	
Micron	
Mitsubishi	
Motorola	
NEC	
Samsung	KM616513J
Sharp	
Sony	

High Speed BiCMOS Static RAM (1M)

ORGANIZATION	256K x 4, 28-pin	256K x 4, 32-pin (OE)
PACKAGE WIDTH	0.4 INCH SOJ	0.4 INCH SOJ
TOSHIBA	TC55B4256J	TC55B4257J
Cypress		
Fujitsu		
Hitachi		HM674256UHJ
Micron		MT5C256K4A1DJ
Mitsubishi		
Motorola	MCM6728AWJ	MCM6729AWJ
NEC		
Samsung		KM64B1003J KM641003J
Sharp		
Sony		

High Speed BiCMOS Static RAM (1M)

ORGANIZATION	128K x 8, 32-pin
PACKAGE WIDTH	0.4 INCH SOJ
TOSHIBA	TC55B8128J
Cypress	
Fujitsu	
Hitachi	HM678127UHJ HM628127HJP
Micron	MT5C128K8A1DJ
Mitsubishi	
Motorola	MCM6726AWJ
NEC	μ PD431008LE
Samsung	KM68B1002J KM681002J
Sharp	
Sony	CXK581120J

High Speed CMOS Static RAM (1M)

ORGANIZATION	256K x 4, 28-pin	256K x 4, 32-pin (OE)
PACKAGE WIDTH	0.4 INCH SOJ	0.4 INCH SOJ
TOSHIBA	TC55V1664J	TC55V1664J
Cypress		
Fujitsu		
Hitachi		HM651664HLP
Micron	MT5C64K16A1DJ	MT5C64K16A1DJ
Mitsubishi		
Motorola	M6M5V16016J	M6M5V16016J
NEC		μ PD431016LE
Samsung		KM64B1002J
Sharp		
Sony		

High Speed CMOS Static RAM (1.25M)

ORGANIZATION	256K x 4, 28-pin	256K x 4, 32-pin (OE)
PACKAGE WIDTH	0.4 INCH SOJ	0.4 INCH SOJ
TOSHIBA	TC55V1664J	TC55V1664J
Cypress		
Fujitsu		
Hitachi		
Micron		
Mitsubishi	M6M5V16016J	M6M5V16016J
Motorola		
NEC		
Samsung		
Sharp		
Sony		

High Speed CMOS Static RAM (1M)

ORGANIZATION	256K x 4, 28-pin	256K x 4, 32-pin (OE)
PACKAGE WIDTH	0.4 INCH SOJ	0.4 INCH SOJ
TOSHIBA	TC55V1664J	TC55V1664J
Cypress		
Fujitsu		
Hitachi		HM651664HLP
Micron	MT5C64K16A1DJ	MT5C64K16A1DJ
Mitsubishi		
Motorola	M6M5V16016J	M6M5V16016J
NEC		μ PD431016LE
Samsung		KM64B1002J
Sharp		
Sony		

High Speed CMOS Static RAM (1M)

ORGANIZATION	64K x 16, 44-pin		
PACKAGE WIDTH	0.4 INCH SOJ	0.4 INCH SOJ (3.3V)	TYPE II TSOP (Forward) (3.3V)
TOSHIBA	TC551664J	TC55V1664J	TC55V1664FT
Cypress			
Fujitsu			
Hitachi	HM621664HJP		
Micron	MT5C64K16A1DJ	MT5LC64K16D4DJ	MT5LC64K16D4TG
Mitsubishi		M5M5V1B016J	M5M5V1B016TP
Motorola			
NEC	μ PD431016LE		
Samsung	KM6161002J		
Sharp			
Sony			

High Speed CMOS Static RAM (1.125M)

ORGANIZATION	64K x 18, 44-pin	
PACKAGE WIDTH	0.4 INCH SOJ (3.3V)	TYPE II TSOP (Forward) (3.3V)
TOSHIBA	TC55V1864J	TC55V1864FT
Cypress		
Fujitsu		
Hitachi		
Micron		
Mitsubishi	M5M5V1B018J	M5M5V1B018TP
Motorola		
NEC		
Samsung		
Sharp		
Sony		

High Speed CMOS Static RAM (4M)

ORGANIZATION	4M x 1, 32-pin	1M x 4, 32-pin
PACKAGE WIDTH	0.4 INCH SOJ	0.4 INCH SOJ
TOSHIBA	TC551402J	TC551402J
Cypress		
Fujitsu	MB82B201-PJ	MB82B201-PJ
Hitachi		HM674100HJP
Micron		MT5C1M4B2DJ
Mitsubishi		
Motorola		MCM6249WJ
NEC	μ PD434001LE	μ PD434004LE
Samsung		KM644002J
Sharp		
Sony		

High Speed Synchronous Static RAM (1M)

ORGANIZATION	256K x 4, 36-pin
PACKAGE WIDTH	0.4 INCH SOJ
TOSHIBA	TC55BS4258J
Cypress	
Fujitsu	
Hitachi	HM67A4257JP
Micron	
Mitsubishi	
Motorola	MCM67Q804WJ
NEC	
Samsung	KM741006J
Sharp	
Sony	CXK77410J

Pseudo Static RAM (256K)

ORGANIZATION	256K x 8, 36-pin
PACKAGE WIDTH	0.4 INCH DIP
TOSHIBA	TC51832AP
Cypress	
Fujitsu	
Hitachi	HM6256BP
Micron	
Mitsubishi	
Motorola	
NEC	
Samsung	
Sharp	LH5P832
Sony	

Pseudo Static RAM (1M)

ORGANIZATION	128K x 8, 36-pin
PACKAGE WIDTH	0.4 INCH DIP
TOSHIBA	TC518128CP
Cypress	
Fujitsu	
Hitachi	
Micron	
Mitsubishi	
Motorola	
NEC	
Samsung	
Sharp	LH5P8128
Sony	

Pseudo Static RAM (1M)

ORGANIZATION	128K x 8, 36-pin (CE28)
PACKAGE WIDTH	0.4 INCH DIP
TOSHIBA	TC518128CP
Cypress	
Fujitsu	
Hitachi	HM68128ALP
Micron	
Mitsubishi	
Motorola	
NEC	
Samsung	KM68128P
Sharp	LH5P8128
Sony	

Pseudo Static RAM (256K)

ORGANIZATION	32K x 8, 28-pin		
PACKAGE WIDTH	0.6 INCH DIP	0.45 INCH SOP	0.3 INCH DIP
TOSHIBA	TC51832AP	TC51832AF	TC51832ASP
Cypress			
Fujitsu			
Hitachi	HM65256BP	HM65256BFP	HM65256BSP
Micron			
Mitsubishi			
Motorola			
NEC			
Samsung			
Sharp	LH5P832	LH5P832N	LH5P832D
Sony			

Pseudo Static RAM (1M)

ORGANIZATION	128K x 8, 32-pin		
PACKAGE WIDTH	0.6 INCH DIP	0.525 INCH SOP	8 x 20mm TYPE I TSOP (Forward)
TOSHIBA	TC518128CP	TC518128CFW	TC518128CFT
Cypress			
Fujitsu			
Hitachi			
Micron			
Mitsubishi			
Motorola			
NEC			
Samsung			
Sharp	LH5P8128	LH5P8128N	LH5P8128T
Sony			

Pseudo Static RAM (1M)

ORGANIZATION	128K x 8, 32-pin (CE/CS)			
PACKAGE WIDTH	0.6 INCH DIP	0.45 INCH SOP	0.525 INCH SOP	8 x 20mm TYPE I TSOP (Forward)
TOSHIBA	TC518129CP	TC518129BF	TC518129CFW	TC518129CFT
Cypress				
Fujitsu				
Hitachi	HM658128ALP		HM658128ALFP	HM658128ALT
Micron				
Mitsubishi				
Motorola				
NEC				
Samsung	KM658128P	KM658128G	KM658128G	
Sharp	LH5P8129		LH5P8129N	LH5P8129T
Sony				

Pseudo Static RAM (4M)

ORGANIZATION	512K x 8, 32-pin			
PACKAGE WIDTH	0.6 INCH DIP	0.525 INCH SOP	0.4 INCH TYPE II TSOP (Forward)	0.4 INCH TYPE II TSOP (Reverse)
TOSHIBA	TC518512P	TC518512F	TC518512FT	TC518512TR
Cypress				
Fujitsu				
Hitachi	HM658512LP	HM658512LFP	HM658512LTT	HM658512LRR
Micron				
Mitsubishi				
Motorola				
NEC				
Samsung				
Sharp				
Sony				

Pseudo Static RAM (4M)

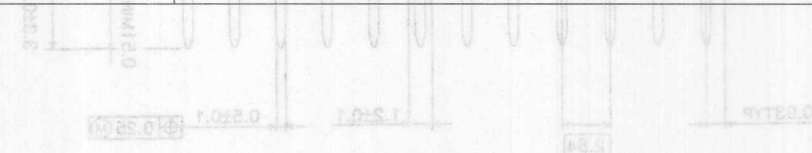
ORGANIZATION	PACKAGE WIDTH	0.8 INCH DIP	0.525 INCH SOP	0.4 INCH TYPE II TSOP (Forward)	0.4 INCH TYPE II TSOP (Reverse)
TOSHIBA	TCS16812P	TCS16812P	TCS16812P	TCS16812PT	TCS16812TR
Cypress					
Fujitsu					
Hitachi	HME65512LP	HME65512LP	HME65512LP	HME65512LTT	HME65512LRR
Mitsumi					
Mitsubishi					
Motrola					
NEC					
Samsung					
Sharp					
Sony					

Package

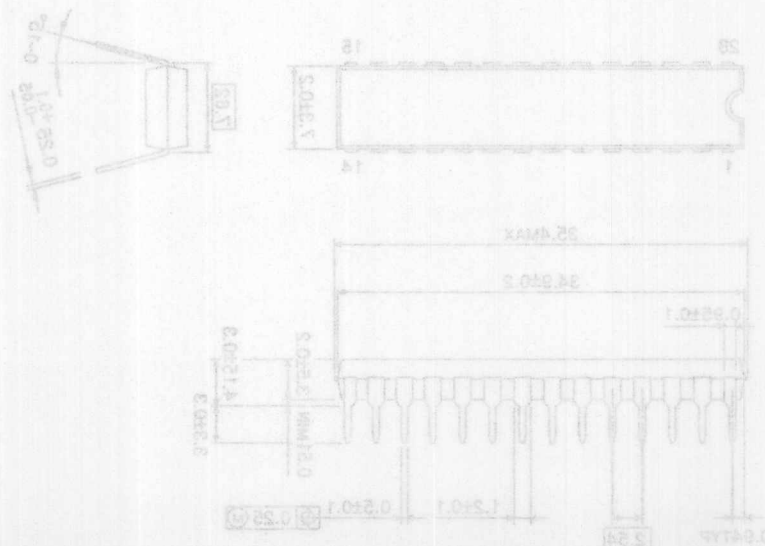
DIP24-P-300B

Dual in-Line Package (DIP)

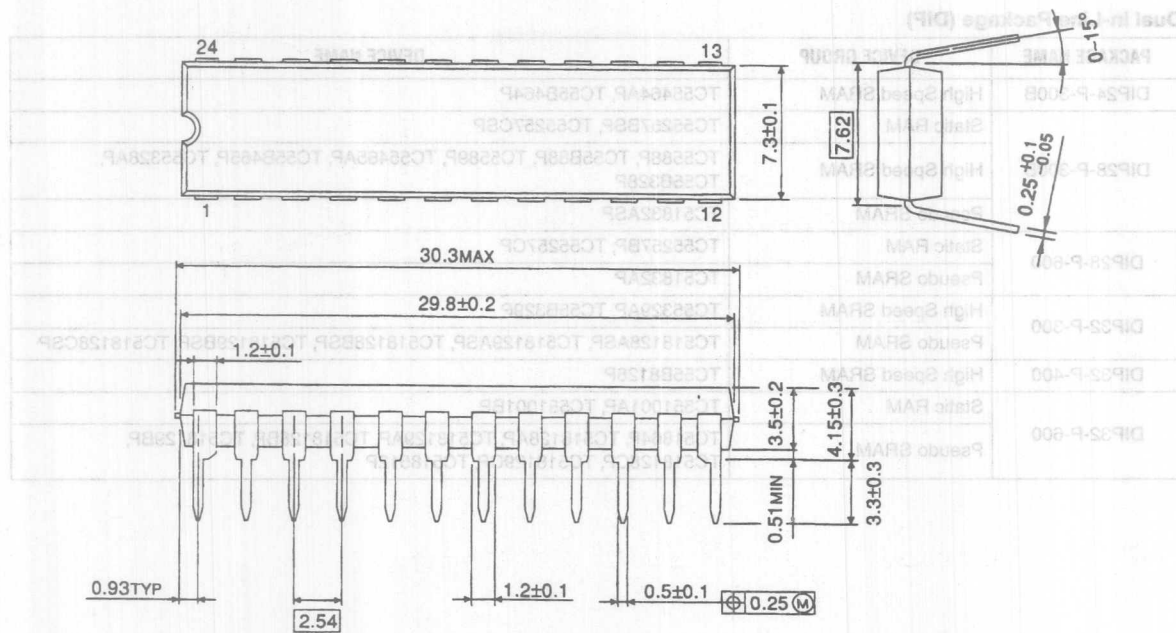
PACKAGE NAME	DEVICE GROUP	DEVICE NAME
DIP24-P-300B	High Speed SRAM	TC55464AP, TC55B464P
DIP28-P-300B	Static RAM	TC55257BSP, TC55257CSP
	High Speed SRAM	TC5588P, TC55B88P, TC5589P, TC55465AP, TC55B465P, TC55328AP, TC55B328P
	Pseudo SRAM	TC51832ASP
DIP28-P-600	Static RAM	TC55257BP, TC55257CP
	Pseudo SRAM	TC51832AP
DIP32-P-300	High Speed SRAM	TC55329AP, TC55B329P
	Pseudo SRAM	TC518128ASP, TC518129ASP, TC518128BSP, TC518129BSP, TC518128CSP
DIP32-P-400	High Speed SRAM	TC55B8128P
DIP32-P-600	Static RAM	TC551001AP, TC551001BP
	Pseudo SRAM	TC51864P, TC518128AP, TC518129AP, TC518128BP, TC518129BP, TC518128CP, TC518129CP, TC518512P



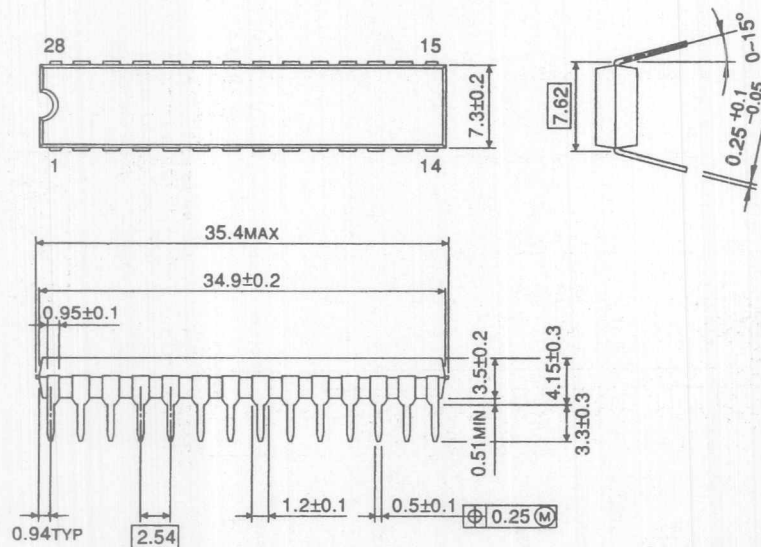
DIP28-P-300B



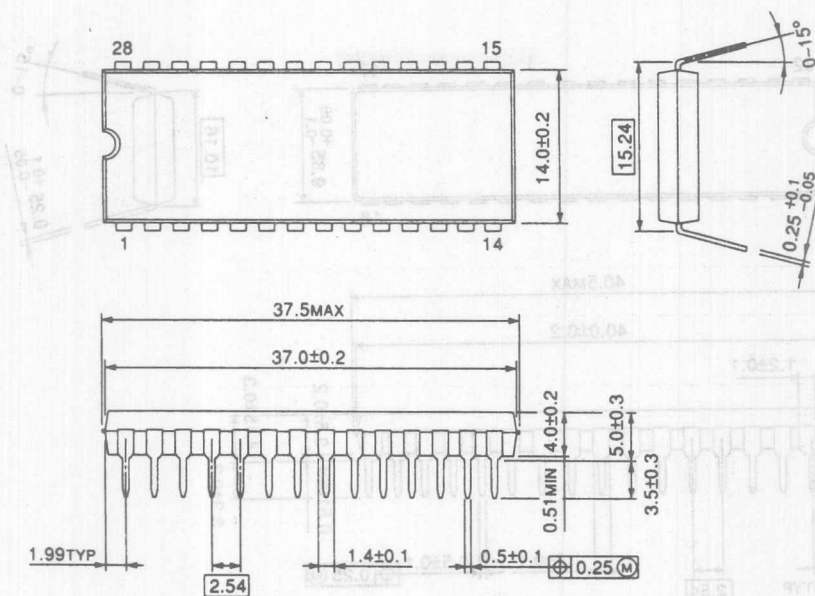
DIP24-P-300B



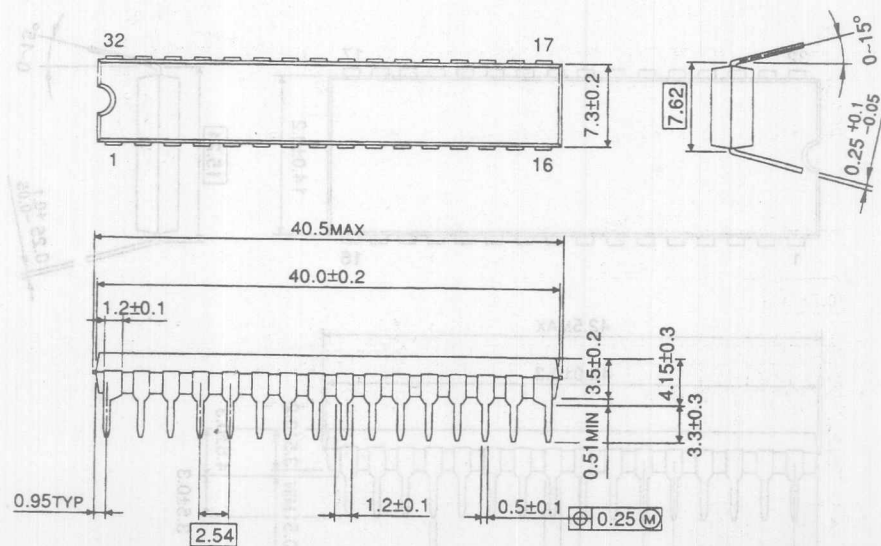
DIP28-P-300B



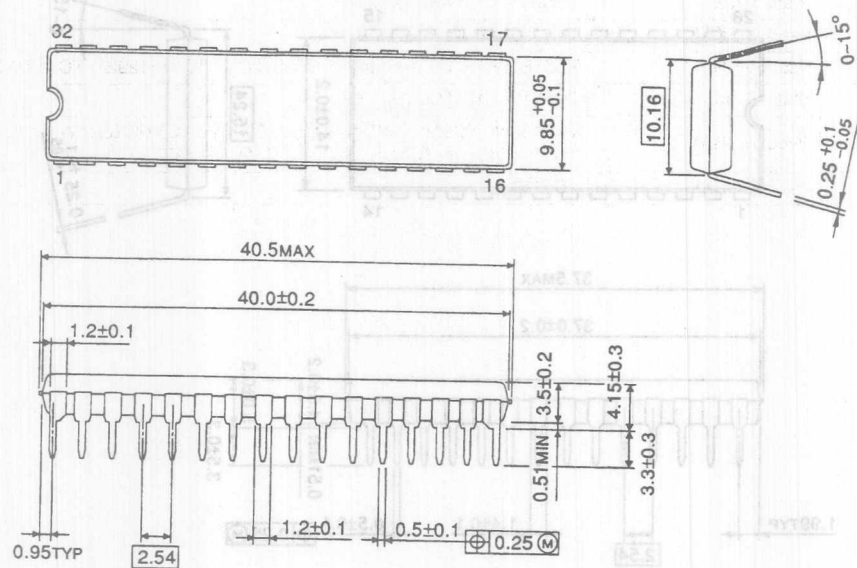
DIP28-P-600



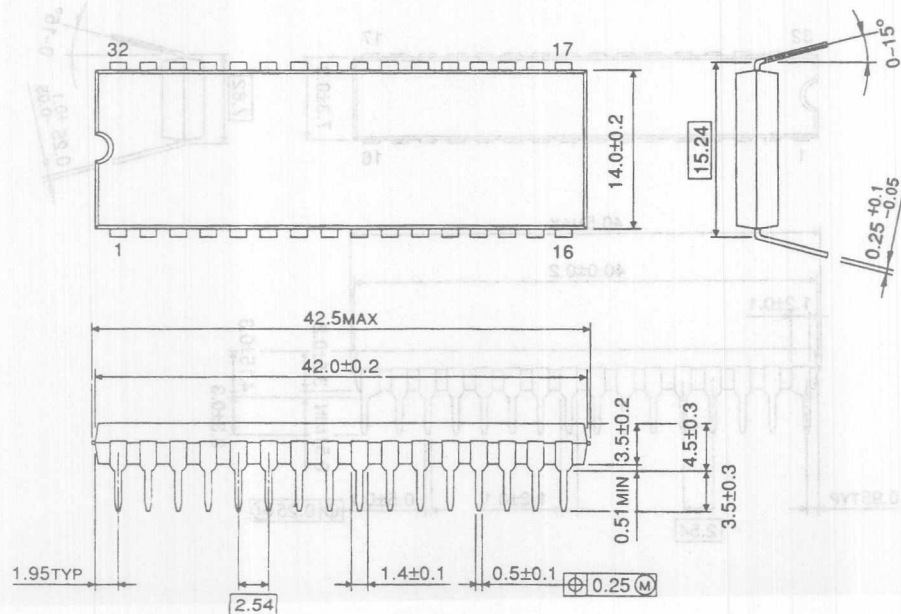
DIP32-P-300



DIP32-P-400

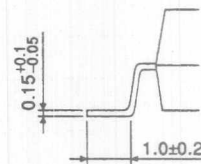
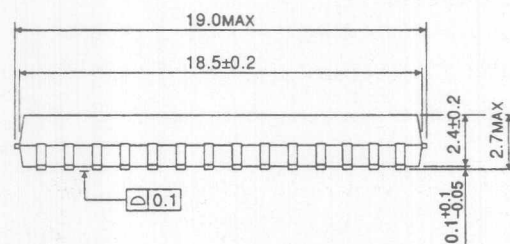
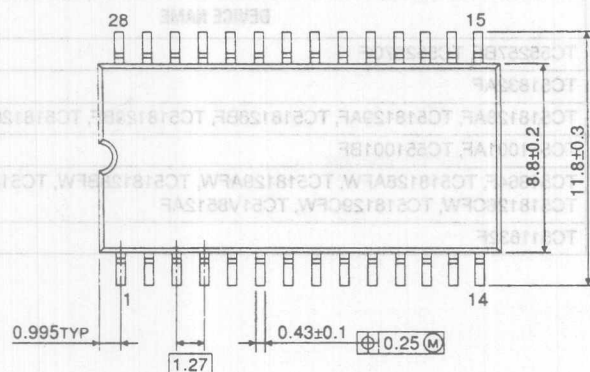


DIP32-P-600

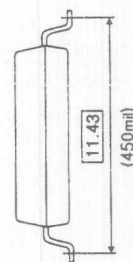
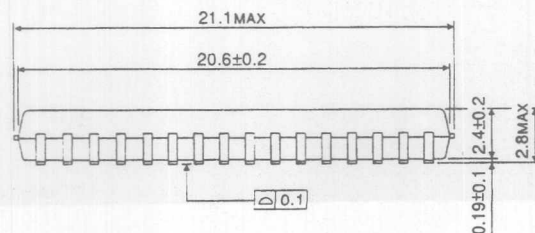
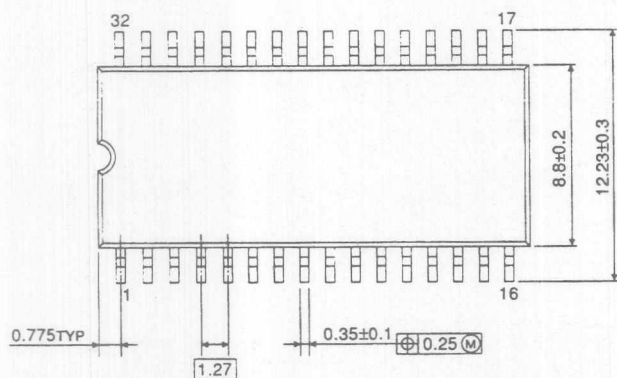


PACKAGE NAME	DEVICE GROUP	DEVICE NAME
SOP28-P-450	Static RAM	TC55257BF, TC55257CF
	Pseudo SRAM	TC51832AF
SOP32-P-450	Pseudo SRAM	TC518128AF, TC518129AF, TC518128BF, TC518129BF, TC518128CF
SOP32-P-525	Static RAM	TC551001AF, TC551001BF
	Pseudo SRAM	TC51864F, TC518128AFW, TC518129AFW, TC518128BFW, TC518129BFW, TC518128CFW, TC518129CFW, TC51V8512AF
SOP40-P-525	Pseudo SRAM	TC511632F

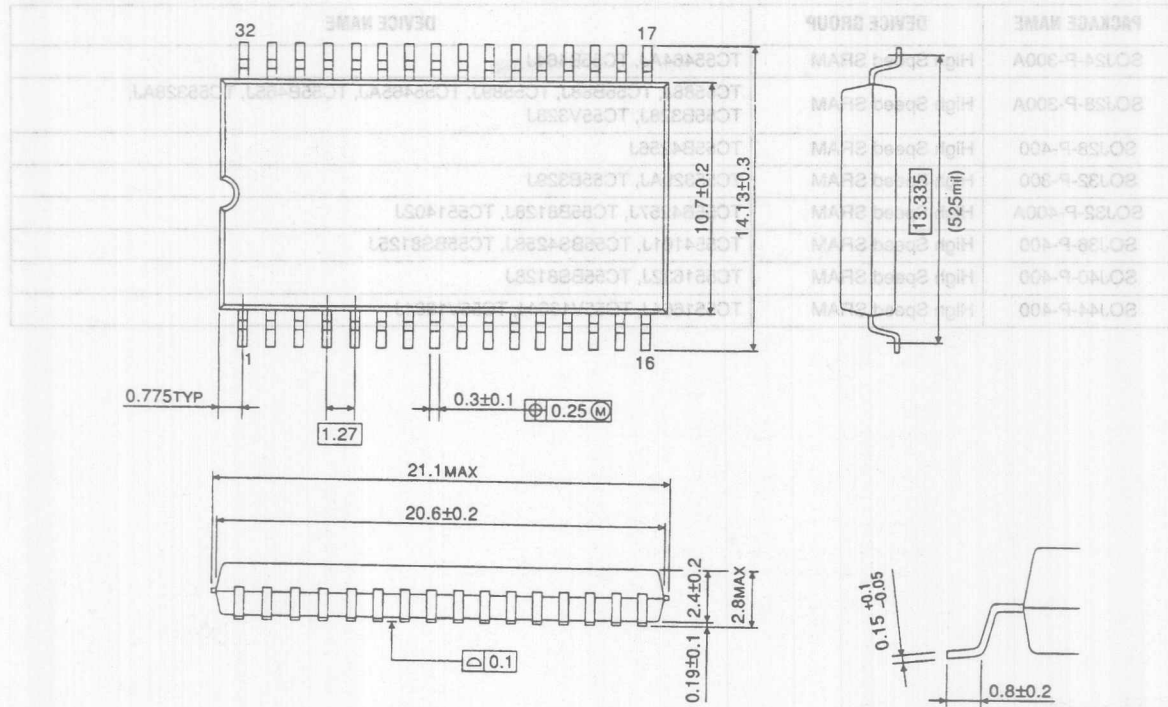
SOP28-P-450



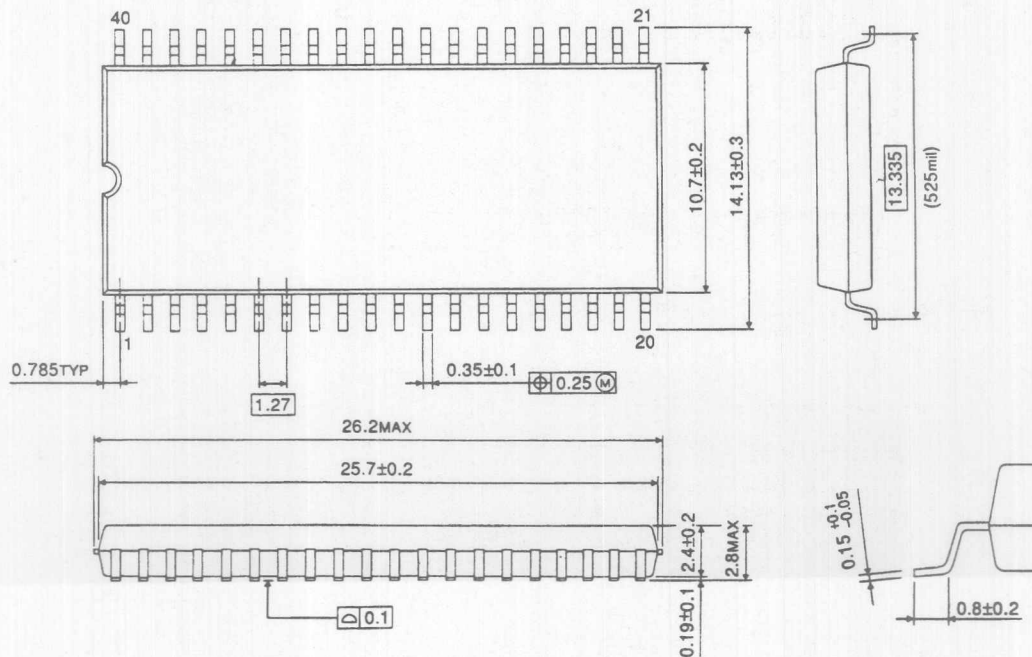
SOP32-P-450



SOP32-P-525



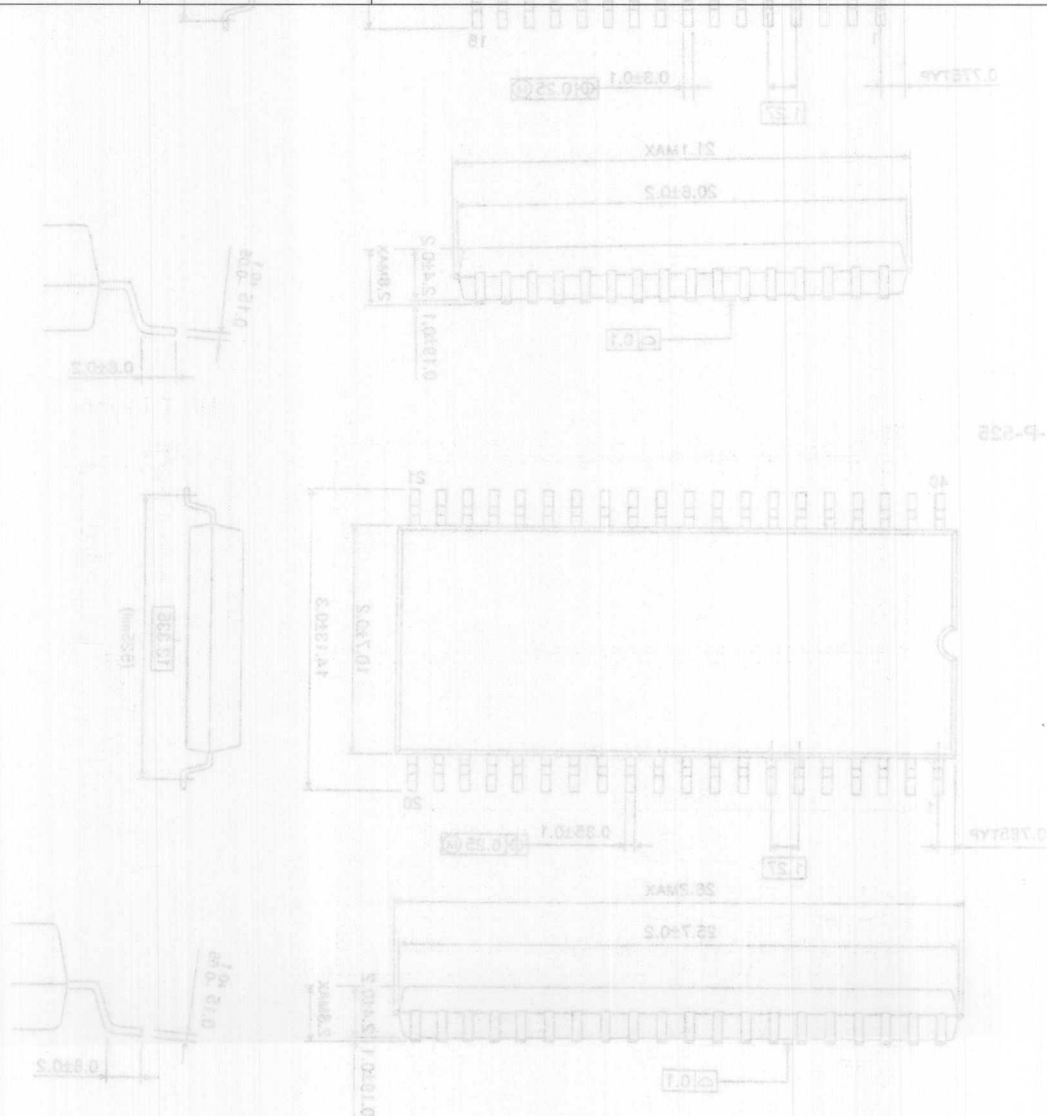
SOP40-P-525



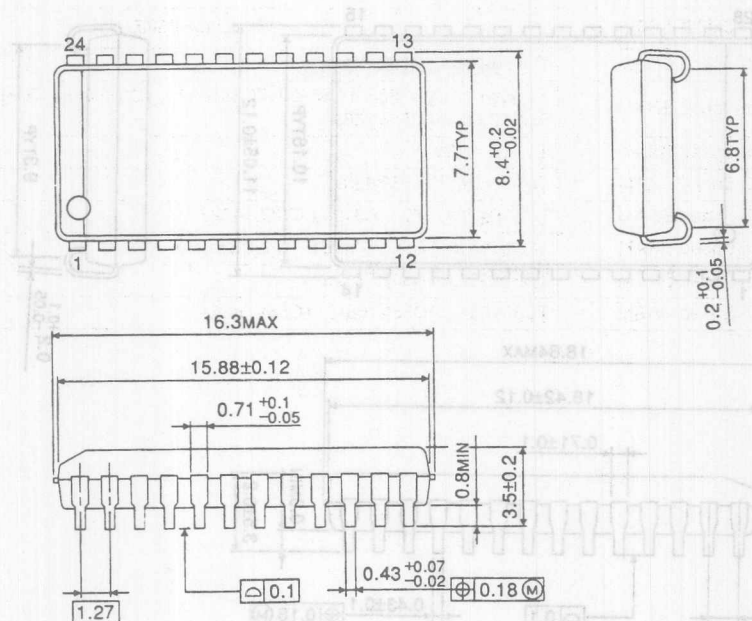
Small Outline J-lead Package (SOJ)

253-9-55908

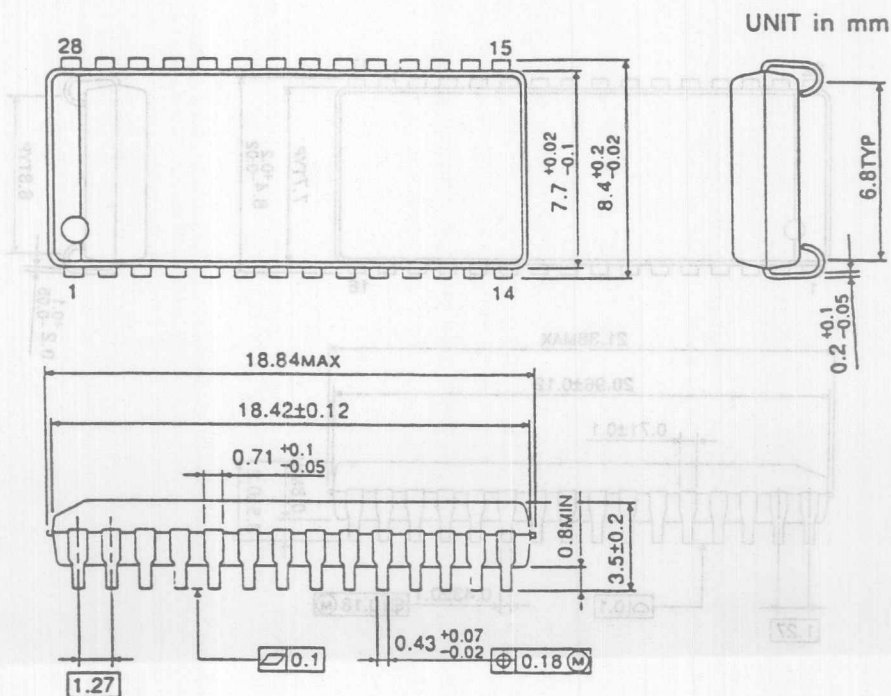
PACKAGE NAME	DEVICE GROUP	DEVICE NAME
SOJ24-P-300A	High Speed SRAM	TC55464AJ, TC55B464J
SOJ28-P-300A	High Speed SRAM	TC5588J, TC55B88J, TC5589J, TC55465AJ, TC55B465J, TC55328AJ, TC55B328J, TC55V328J
SOJ28-P-400	High Speed SRAM	TC55B4256J
SOJ32-P-300	High Speed SRAM	TC55329AJ, TC55B329J
SOJ32-P-400A	High Speed SRAM	TC55B4257J, TC55B8128J, TC551402J
SOJ36-P-400	High Speed SRAM	TC554101J, TC55BS4258J, TC55BS8125J
SOJ40-P-400	High Speed SRAM	TC551632J, TC55BS8128J
SOJ44-P-400	High Speed SRAM	TC551664J, TC55V1664J, TC55V1864J



SOJ24-P-300A

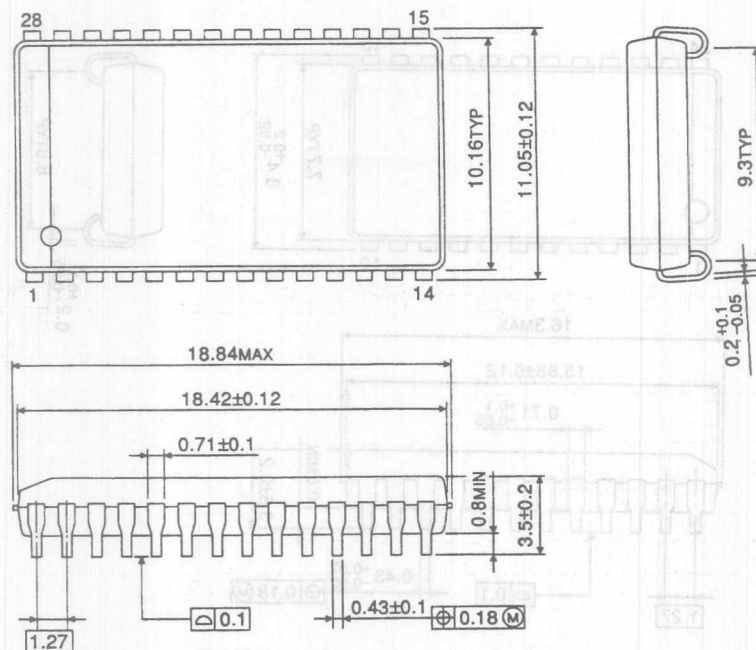


SOJ28-P-300A



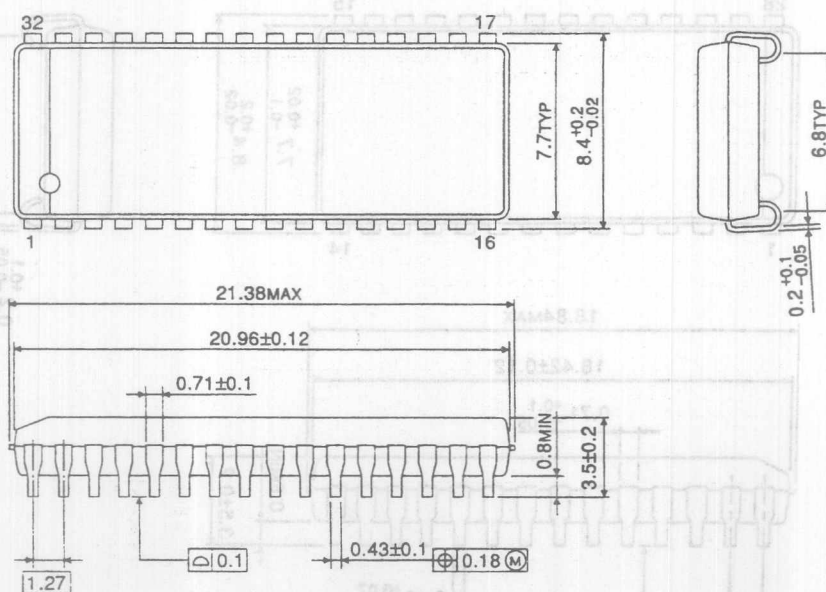
SOJ28-P-400

SOJ28-P-400A



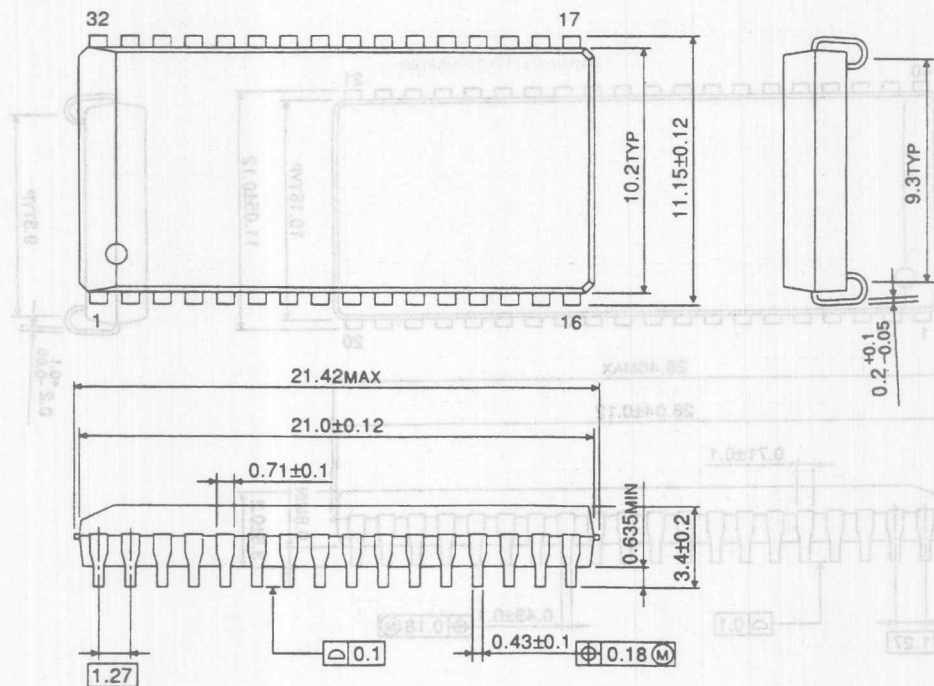
SOJ32-P-300

SOJ32-P-300A



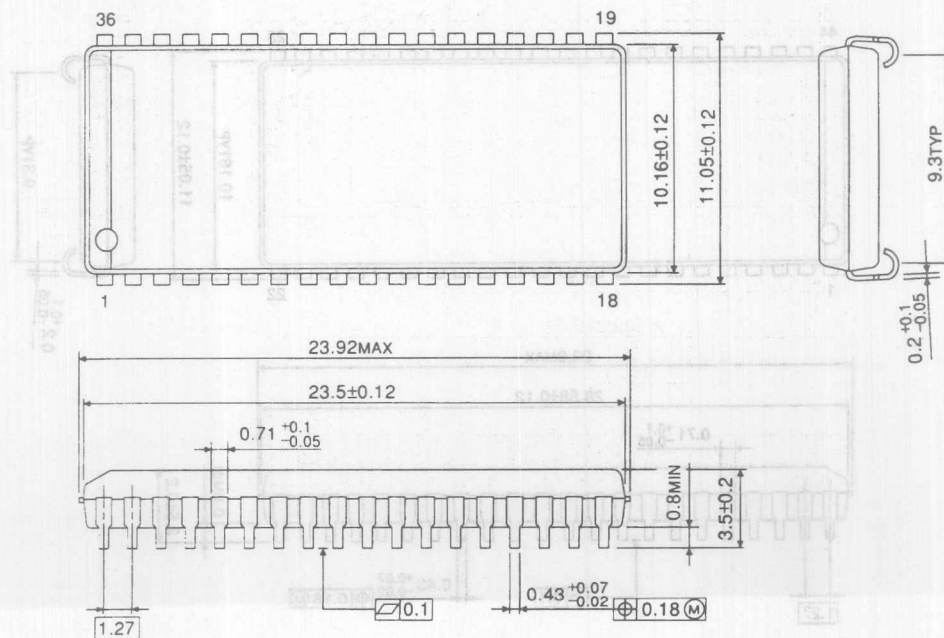
SOJ32-P-400A

SOJ32-P-400A

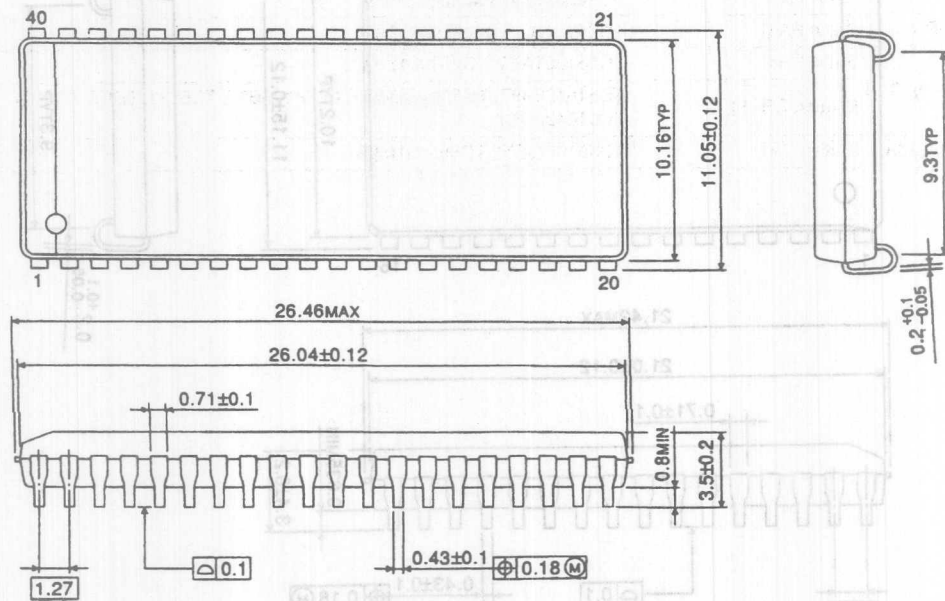


SOJ36-P-400

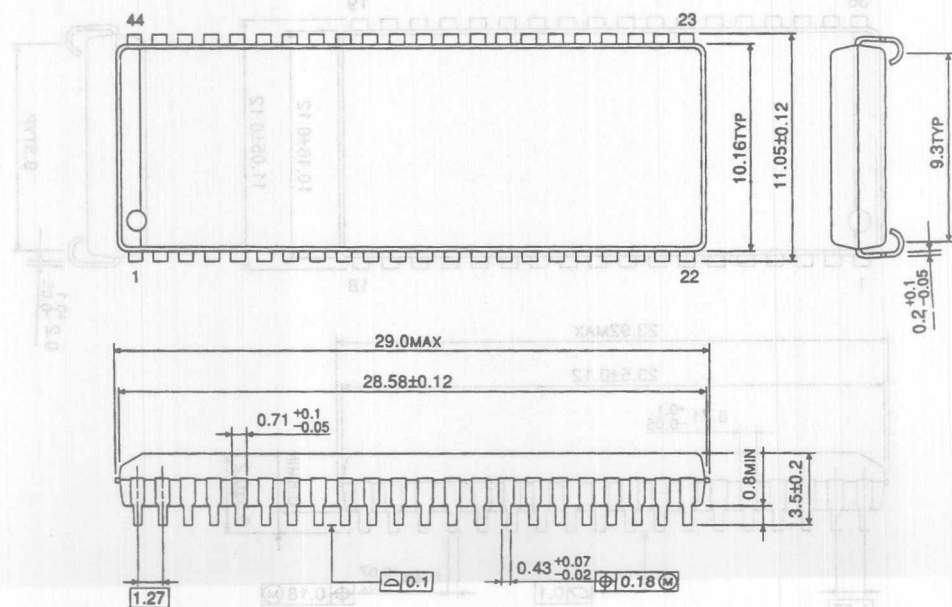
SOJ36-P-400



SOJ40-P-400



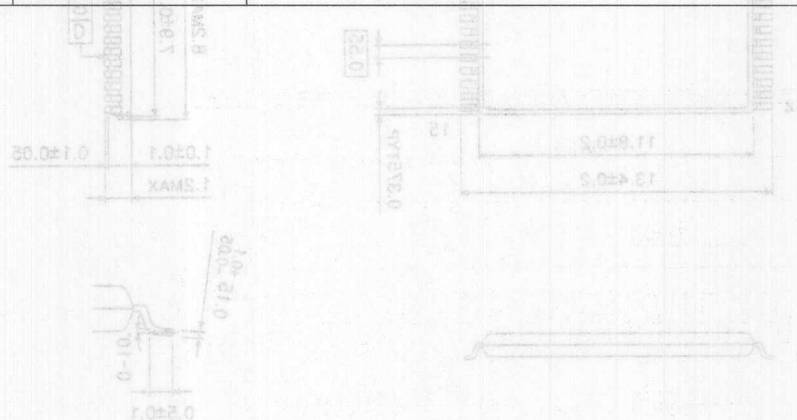
SOJ44-P-400



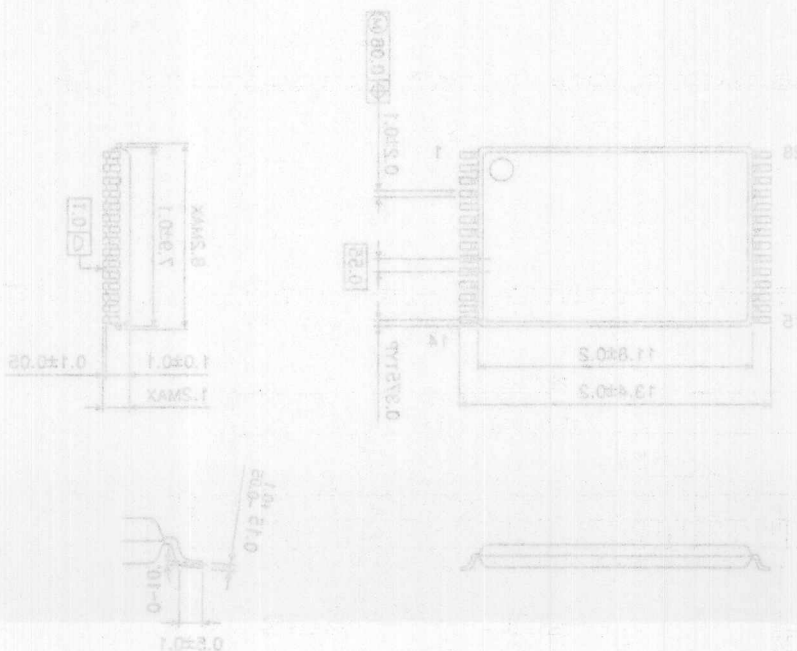
Thin Small Outline L-lead Package (TSOP I)

9-85908T

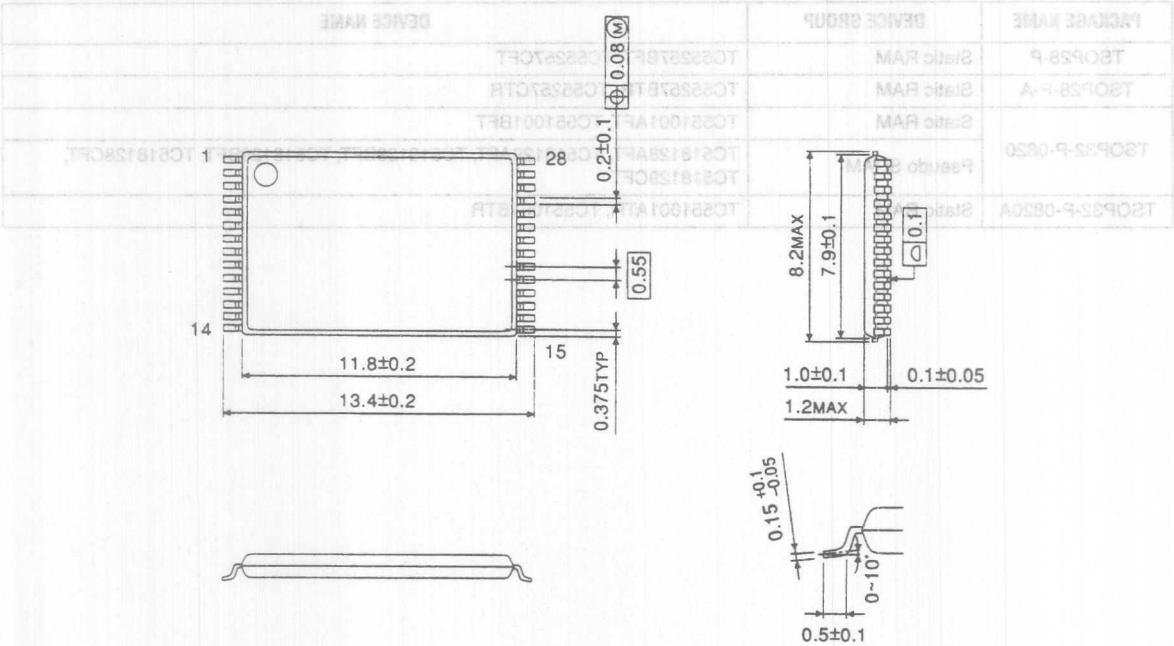
PACKAGE NAME	DEVICE GROUP	DEVICE NAME
TSOP28-P	Static RAM	TC55257BFT, TC55257CFT
TSOP28-P-A	Static RAM	TC55257BTR, TC55257CTR
TSOP32-P-0820	Static RAM	TC551001AFT, TC551001BFT
	Pseudo SRAM	TC518128AFT, TC518129AFT, TC518128BFT, TC518129BFT, TC518128CFT, TC518129CFT
TSOP32-P-0820A	Static RAM	TC551001ATR, TC551001BTR



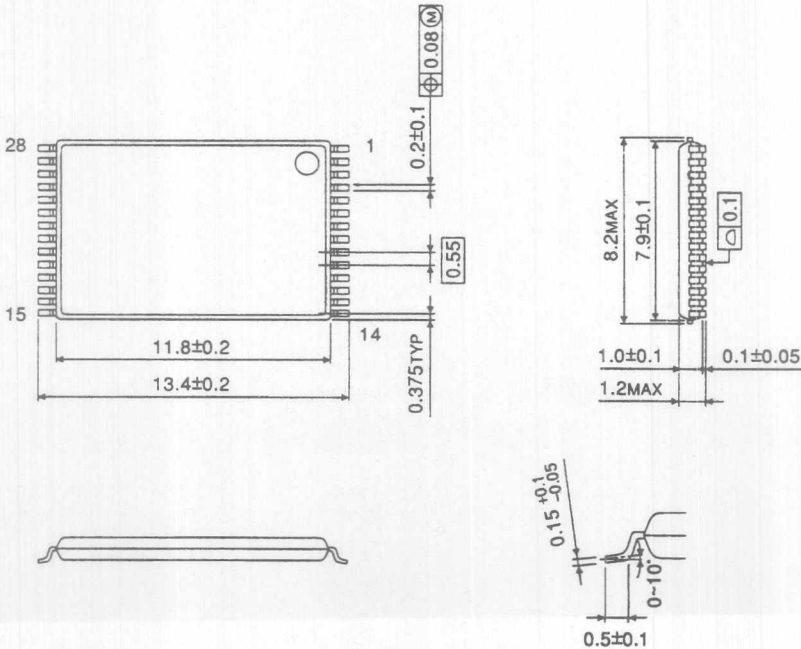
A-9-85908T



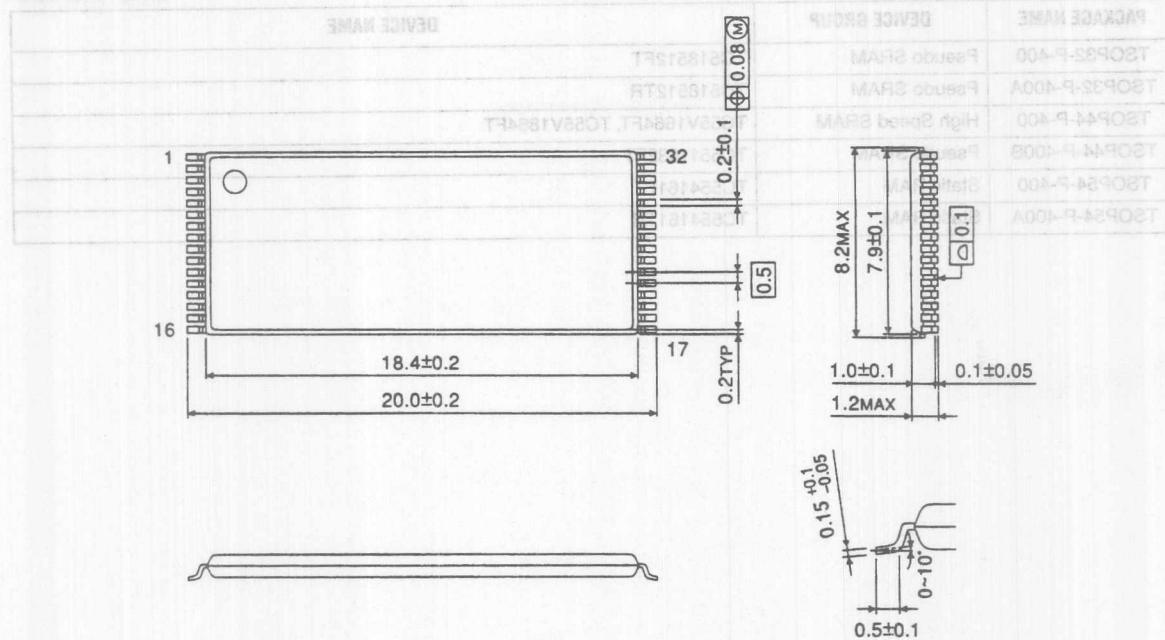
TSOP28-P



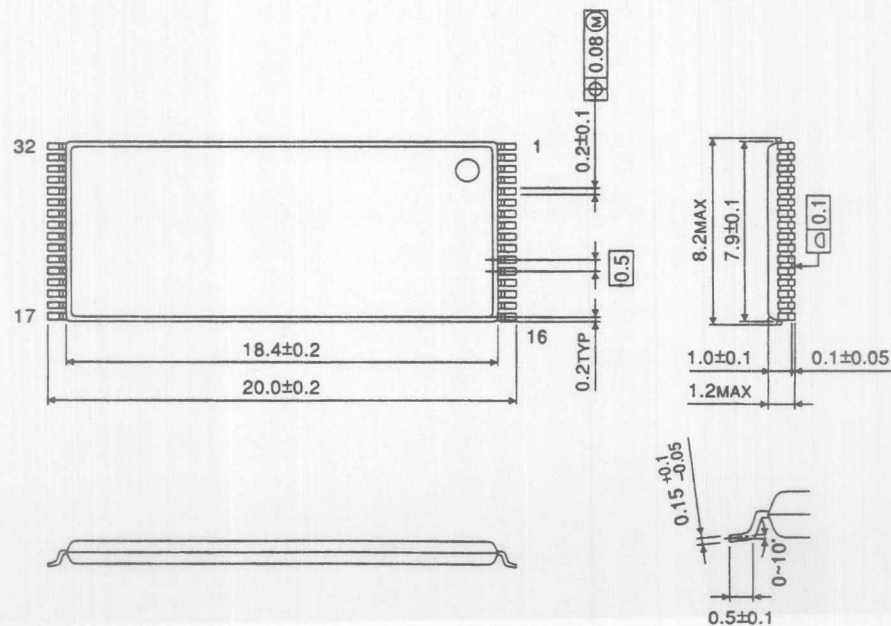
TSOP28-P-A



TSOP32-P-0820



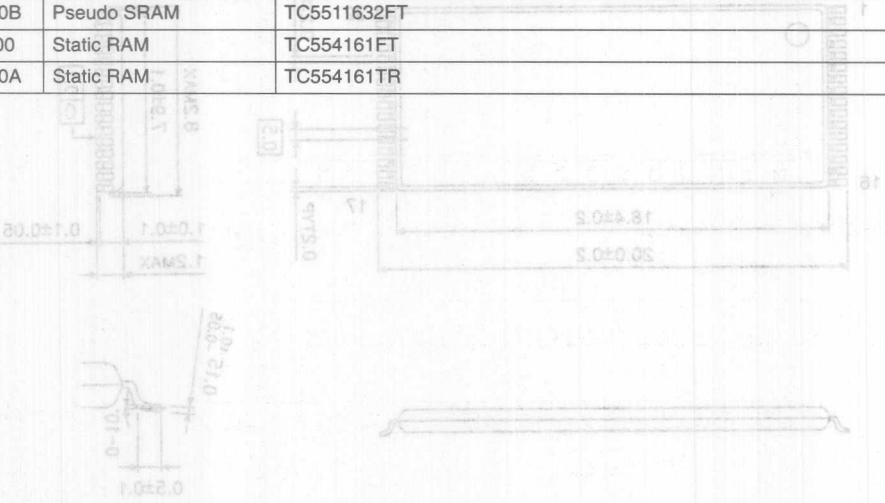
TSOP32-P-0820A



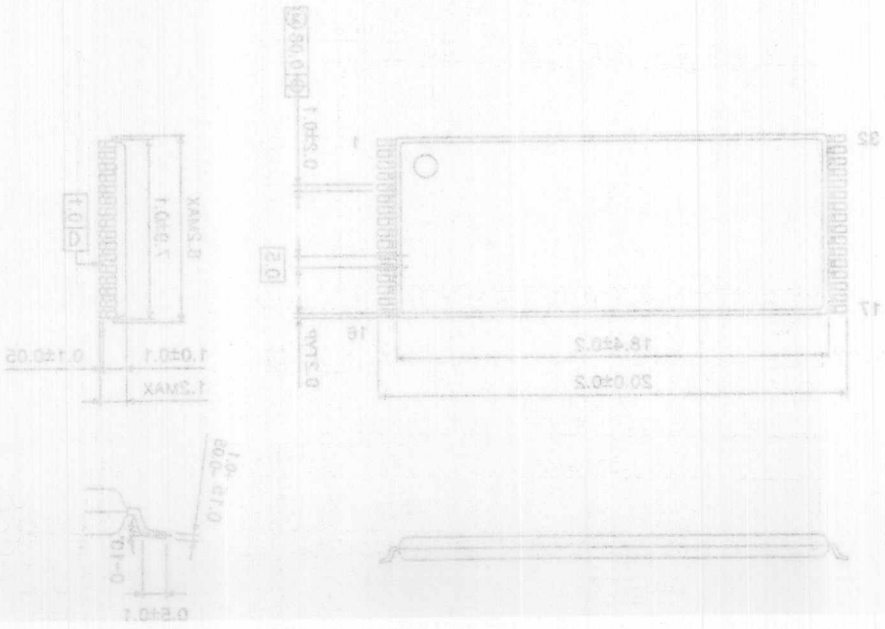
Thin Small Outline L-lead Package (TSOP II)

TSOP32-P-0820

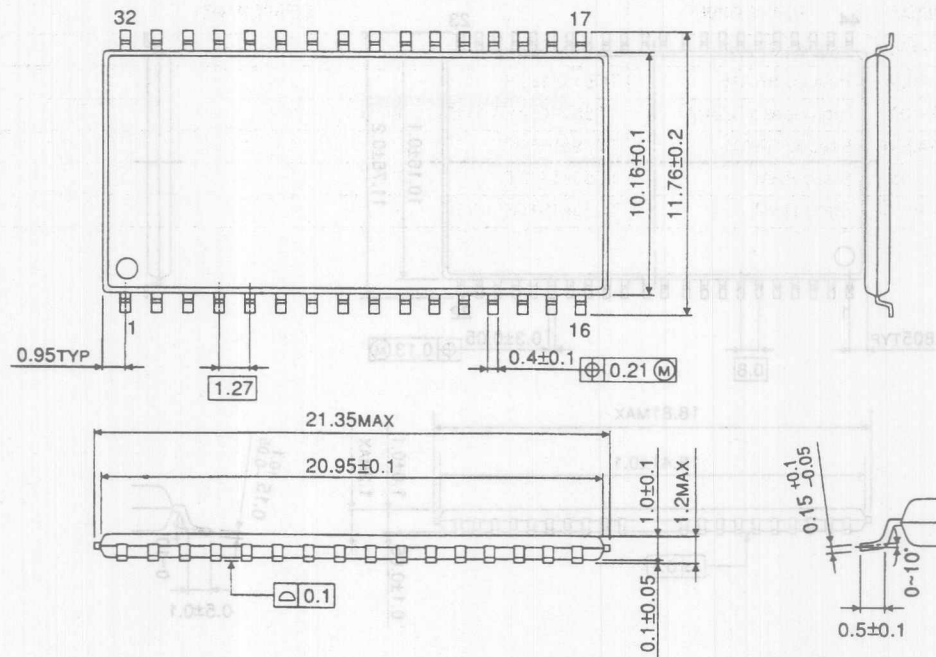
PACKAGE NAME	DEVICE GROUP	DEVICE NAME
TSOP32-P-400	Pseudo SRAM	TC518512FT
TSOP32-P-400A	Pseudo SRAM	TC518512TR
TSOP44-P-400	High Speed SRAM	TC55V1664FT, TC55V1864FT
TSOP44-P-400B	Pseudo SRAM	TC5511632FT
TSOP54-P-400	Static RAM	TC554161FT
TSOP54-P-400A	Static RAM	TC554161TR



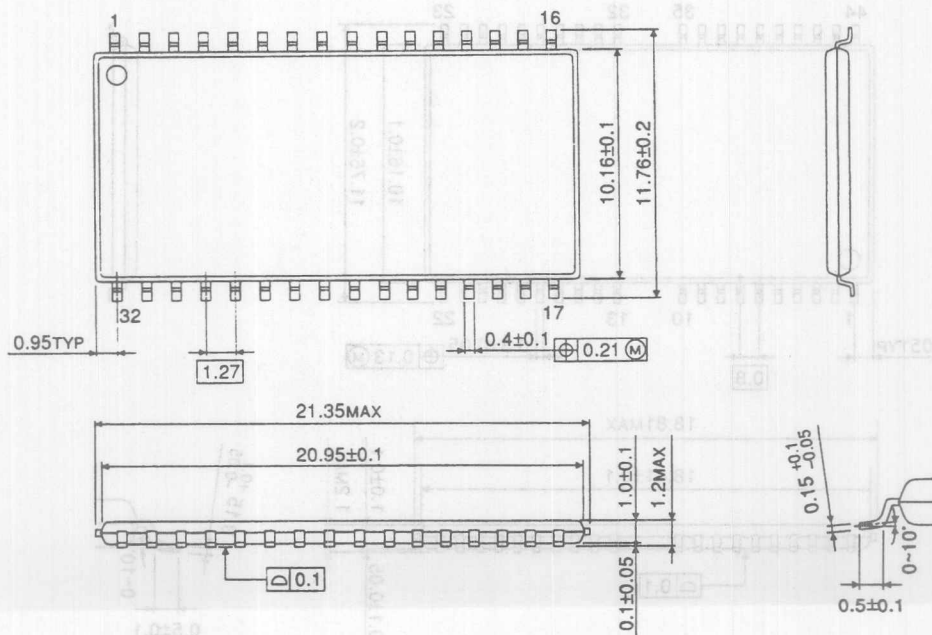
TSOP44-P-0820A



TSOP32-P-400

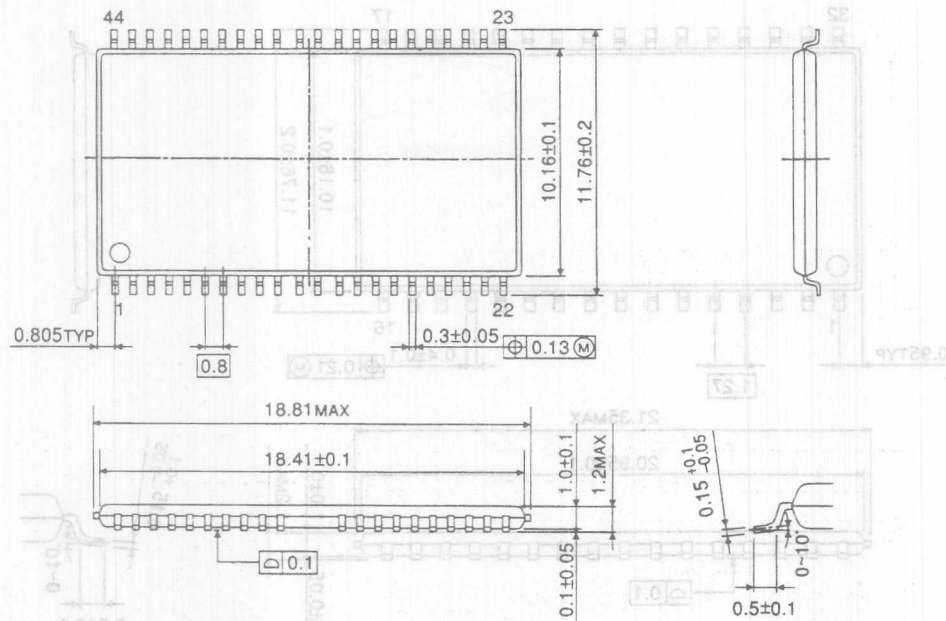


TSOP32-P-400A



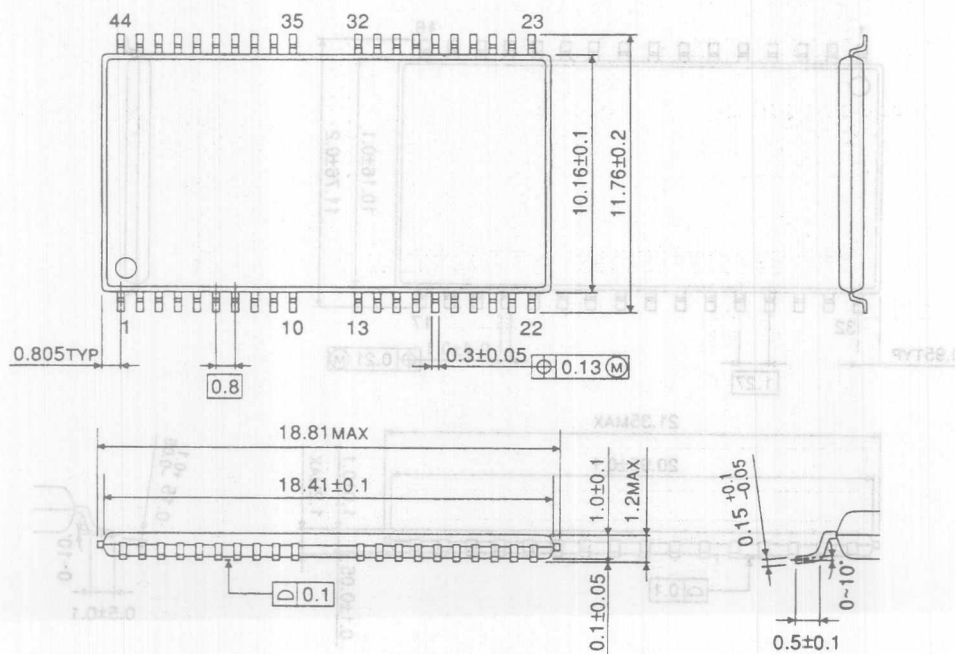
TSOP44-P-400

TSOP44-P-400



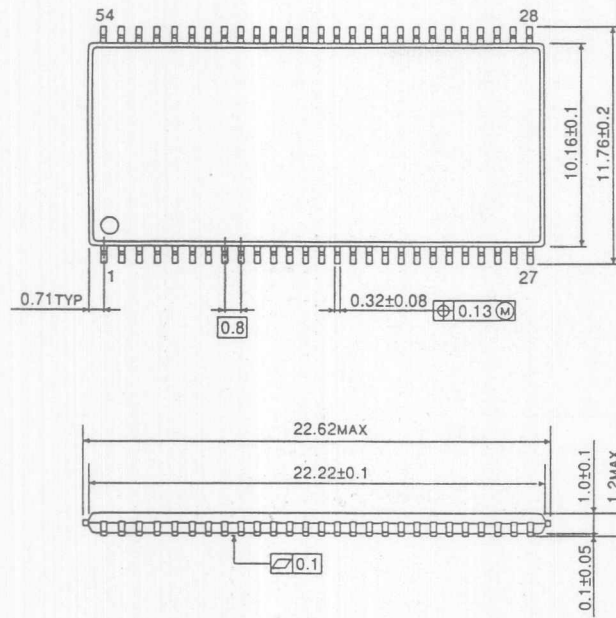
TSOP44-P-400B

TSOP44-P-400B

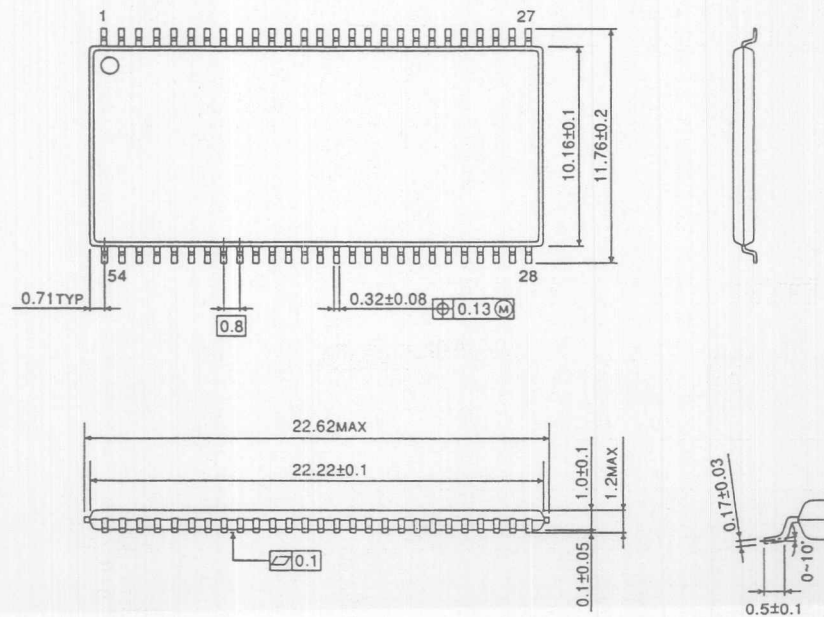


TSOP54-P-400

Notes



TSOP54-P-400A



Notes

Page	Features	Speed (ns)	Package	Organization	Density
A-1		85, 100	R, E, SP, FT, TR	32K x 8	256K
A-9	Low Power	85, 100	R, E, SP, FT, TR	32K x 8	256K
A-17	Low Temp	85, 100	R, E, SP, FT, TR	32K x 8	256K
A-23	Low Power/Low Temp	85, 100	R, E, SP, FT, TR	32K x 8	256K
A-33	Low Power/Low Volt	85, 100	R, E, SP, FT, TR	32K x 8	256K
A-43	Ind Temp/Low Power	85, 100	R, E, SP, FT, TR	32K x 8	256K
A-51		70, 85, 100	R, E, SP, FT, TR	32K x 8	256K
A-59	Low Power	70, 85, 100	R, E, SP, FT, TR	32K x 8	256K
A-67	Industrial Temp	85, 100	R, E, SP, FT, TR	32K x 8	256K
A-75	Ind Temp/Low Power	85, 100	R, E, SP, FT, TR	32K x 8	256K
A-83	Low Temp	70, 85, 100	R, E, SP, FT, TR	32K x 8	256K
A-91	Low Power/Low Temp	70, 85, 100	R, E, SP, FT, TR	32K x 8	256K
A-99	Low Power/Low Volt	70, 85, 100	R, E, SP, FT, TR	32K x 8	256K
A-109	Industrial Temp	85, 100	R, E, SP, FT, TR	128K x 8	1M
A-117	Ind Temp/Low Power	85, 100	R, E, SP, FT, TR	128K x 8	1M
A-125		70, 85, 100	R, E, SP, FT, TR	128K x 8	1M
A-133	Low Power	70, 85, 100	R, E, SP, FT, TR	128K x 8	1M
A-141		70, 85, 100	FT, TR	256K x 16	4M
A-149	Low Power	70, 85, 100	FT, TR	256K x 16	4M

Standard Static RAM

	Density	Organization	Package	Speed (ns)	Features	Page
TC55257B	256K	32K x 8	P, F, SP, FT, TR	85, 100		A-1
TC55257B-L	256K	32K x 8	P, F, SP, FT, TR	85, 100	Low Power	A-9
TC55257B-(LT)	256K	32K x 8	P, F, SP, FT, TR	85, 100	Low Temp.	A-17
TC55257B-L(LT)	256K	32K x 8	P, F, SP, FT, TR	85, 100	Low Power/Low Temp.	A-25
TC55257B-L(LV)	256K	32K x 8	P, F, SP, FT, TR	85, 100	Low Power/Low Volt.	A-33
TC55257BI-L	256K	32K x 8	P, F, SP, FT, TR	100	Ind. Temp./Low Power	A-43
TC55257C	256K	32K x 8	P, F, SP, FT, TR	70, 85, 100		A-51
TC55257C-L	256K	32K x 8	P, F, SP, FT, TR	70, 85, 100	Low Power	A-59
TC55257CI	256K	32K x 8	P, F, SP, FT, TR	85, 100	Industrial Temp.	A-67
TC55257CI-L	256K	32K x 8	P, F, SP, FT, TR	85, 100	Ind. Temp./Low Power	A-75
TC551001A-(LT)	1M	128K x 8	P, F, FT, TR	70, 85, 100	Low Temp.	A-83
TC551001A-L(LT)	1M	128K x 8	P, F, FT, TR	70, 85, 100	Low Power/Low Temp.	A-91
TC551001A-L(LV)	1M	128K x 8	P, F, FT, TR	70, 85, 100	Low Power/Low Volt.	A-99
TC551001AI	1M	128K x 8	P, F, FT, TR	85, 100	Industrial Temp.	A-109
TC551001AI-L	1M	128K x 8	P, F, FT, TR	85, 100	Ind. Temp./Low Power	A-117
TC551001B	1M	128K x 8	P, F, FT, TR	70, 85, 100		A-125
TC551001B-L	1M	128K x 8	P, F, FT, TR	70, 85, 100	Low Power	A-133
TC554161	4M	256K x 16	FT, TR	70, 85, 100		A-141
TC554161-L	4M	256K x 16	FT, TR	70, 85, 100	Low Power	A-149

Package: P = Plastic DIP, F = Flat package (SOP), SP = Slim Plastic DIP, FT = Forward bend TSOP, TR = Reverse bend TSOP

TC55257BPL/BFL/BSPL/BFTL/BTRL-85/10

SILICON GATE CMOS

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257BPL is a 262,144 bit CMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 85ns.

When CE is a logical high, the device is placed in a low power standby mode in which the standby current is 100 μ A. The TC55257BPL has two control inputs. Chip enable (\overline{CE}) allows for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. The TC55257BPL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required.

The TC55257BPL is offered in a standard dual-in-line 28-pin plastic package (0.6/0.3 inch width), a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 100 μ A (max.)
- Single 5V power supply
- Access time (max.)

	TC55257BPL/BFL/BSPL/BFTL/BTRL	
	-85	-10
Access Time	85ns	100ns
Chip Enable Access Time	85ns	100ns
Output Enable Time	45ns	50ns

- Power down feature: \overline{CE}
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package
 - TC55257BPL : DIP28-P-600
 - TC55257BFL : SOP28-P-450
 - TC55257BSPL : DIP28-P-300B
 - TC55257BFTL : TSOP28-P
 - TC55257BTRL : TSOP28-P-A

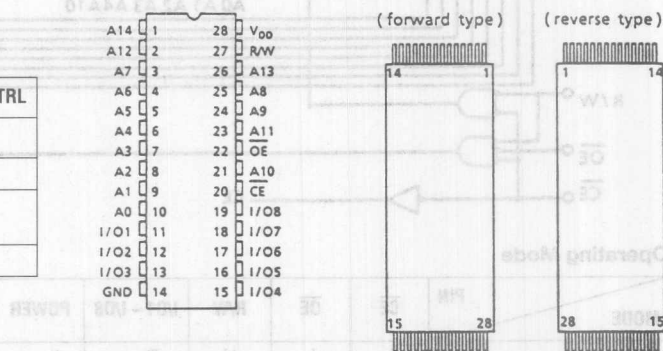
Pin Names

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground

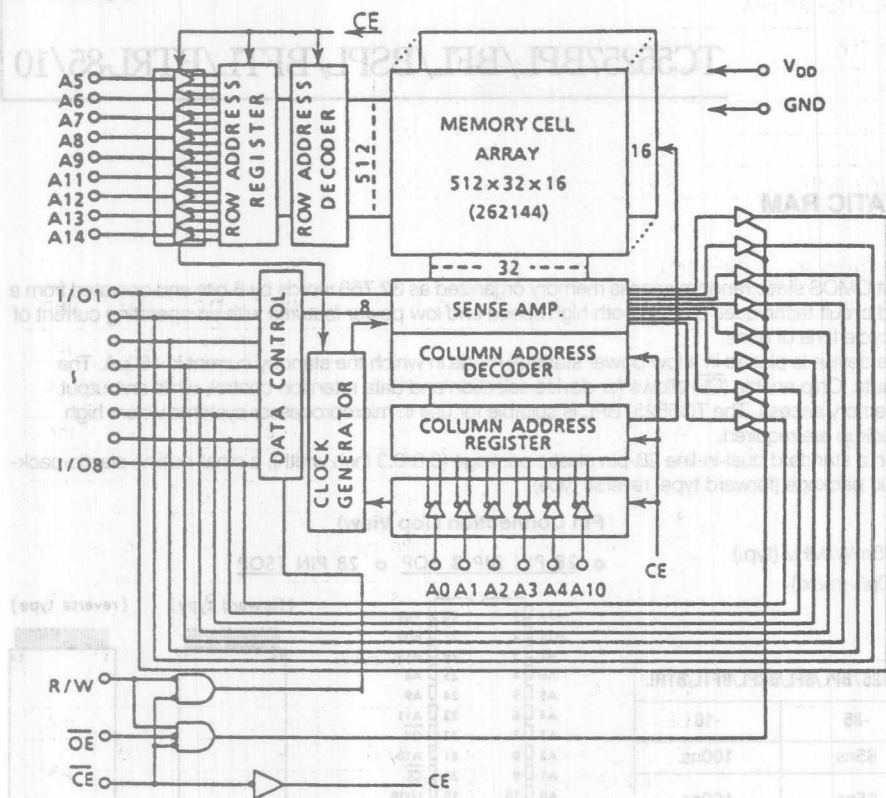
PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	\overline{OE}	A ₁₁	A ₉	A ₈	A ₁₃	R/W	V _{DD}	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀

Pin Connection (Top View)

○ 28 PIN DIP & SOP ○ 28 PIN TSOP



Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	R/W	I/O1 ~ I/O8	POWER
Read		L	L	H	D _{OUT}	I _{DDO}
Write		L	*	L	D _{IN}	I _{DDO}
Output Deselect		L	H	H	High-Z	I _{DDO}
Standby		H	*	*	High-Z	I _{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5* ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.8/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V with a pulse width of 50ns

** Package dependent: 0.6 inch 1.0W, 0.3 inch 0.8W, 0.45 inch 0.6W

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	—	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

* -3.0V with a pulse width of 50ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}		—	—	±1.0	μA
I _{LO}	Output Leakage Current	CE = V _{IH} or R/W = V _{IL} or OE = V _{IH} V _{OUT} = 0 ~ V _{DD}		—	—	±1.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V		-1.0	—	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V		4.0	—	—	mA
I _{DDO1}	Operating Current	CE = V _{IL} R/W = V _{IH} Other Input = V _{IH} /V _{IL} I _{OUT} = 0mA	t _{cycle} = 1μs	—	10	—	mA
			t _{cycle} = Min. cycle	—	—	70	
I _{DDO2}		CE = 0.2V R/W = V _{DD} - 0.2V Other Input = V _{DD} - 0.2V/0.2V I _{OUT} = 0mA	t _{cycle} = 1μs	—	5	—	
			t _{cycle} = Min. cycle	—	—	60	
I _{DDS1}	Standby Current	CE = V _{IH}		—	—	3	mA
I _{DDS2}		CE = V _{DD} - 0.2V V _{DD} = 2.0V ~ 5.5V	Ta = 0 ~ 70°C	—	—	100	μA
			Ta = 25°C	—	2	—	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

Read Cycle						
SYMBOL	PARAMETER	TC55257BPL/BFL/BSPL/BFTL/BTRL				UNIT
		-85		-10		
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	85	—	100	—	ns
t _{ACC}	Address Access Time	—	85	—	100	
t _{CO}	CE Access Time	—	85	—	100	
t _{OE}	Output Enable to Output in Valid	—	45	—	50	
t _{COE}	Chip Enable (CE) to Output in Low-Z	10	—	10	—	
t _{OEE}	Output Enable to Output in Low-Z	5	—	5	—	
t _{OD}	Chip Enable (CE) to Output in High-Z	—	30	—	50	
t _{ODO}	Output Enable to Output in High-Z	—	30	—	40	
t _{OH}	Output Data Hold Time	10	—	10	—	

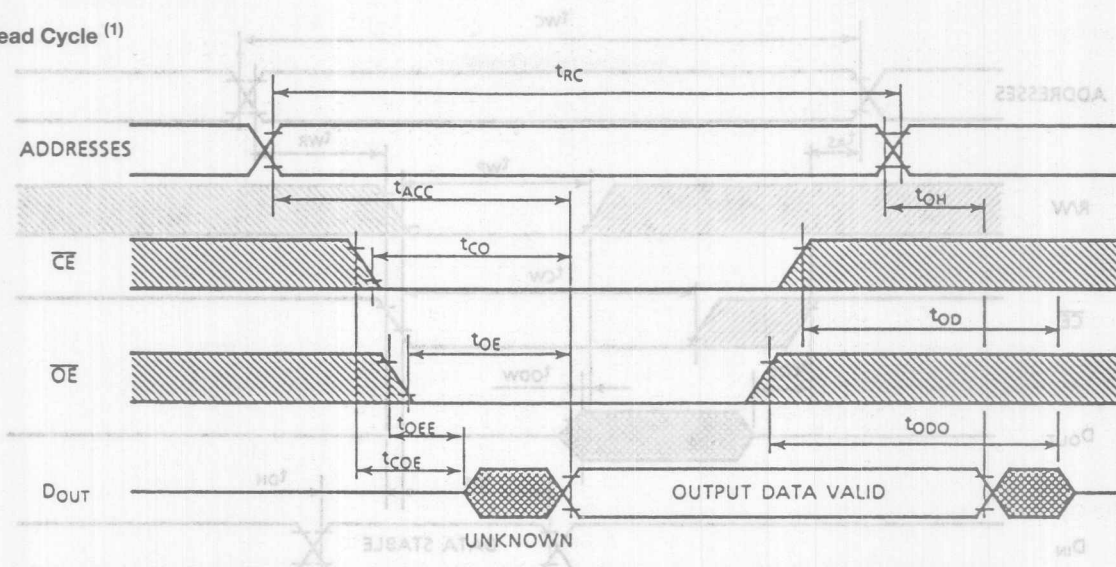
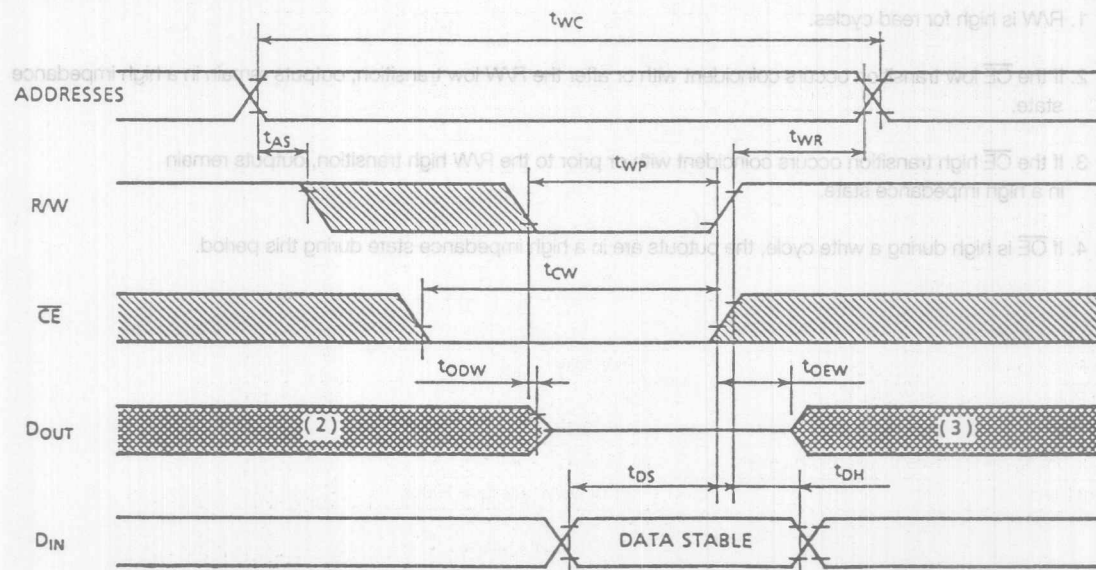
Write Cycle

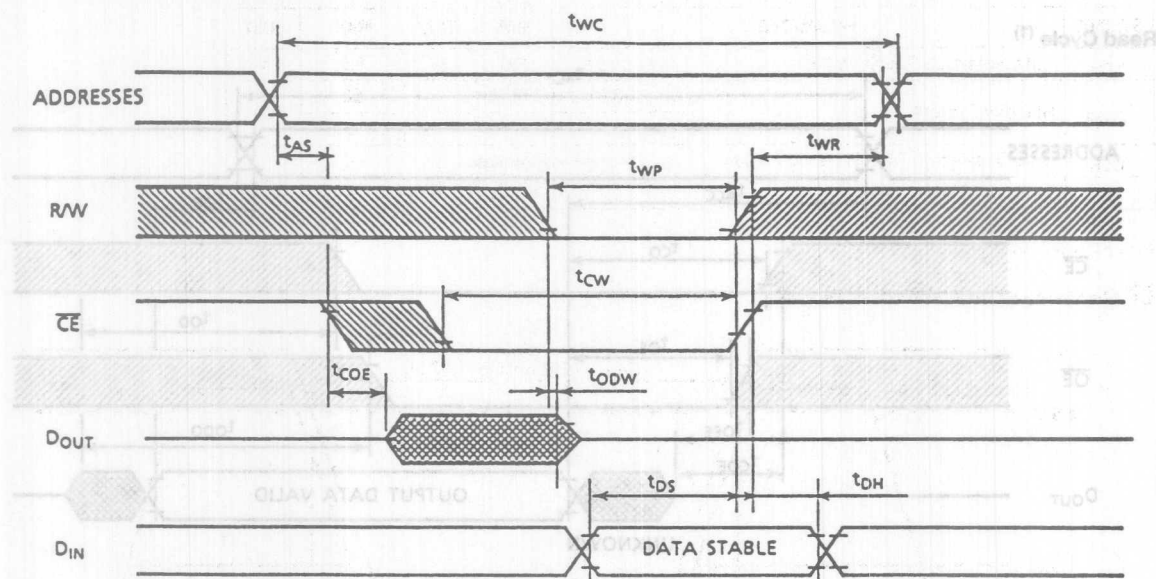
SYMBOL	PARAMETER	TC55257BPL/BFL/BSPL/BFTL/BTRL				UNIT
		-85		-10		
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	85	—	100	—	ns
t _{WP}	Write Pulse Width	60	—	70	—	
t _{CW}	Chip Selection to End of Write	65	—	90	—	
t _{AS}	Address Setup Time	0	—	0	—	
t _{WR}	Write Recovery Time	5	—	5	—	
t _{ODW}	R/W to Output in High-Z	—	30	—	50	
t _{OEW}	R/W to Output in Low-Z	5	—	5	—	
t _{DS}	Data Setup Time	40	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	

AC Test Conditions

Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.2V/0.8V
Output Load	1 TTL Gate and $C_L = 100\text{pF}$

Timing Waveforms

Read Cycle ⁽¹⁾Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)

Write Cycle 2 ⁽⁴⁾ ($\overline{\text{CE}}$ Controlled Write)

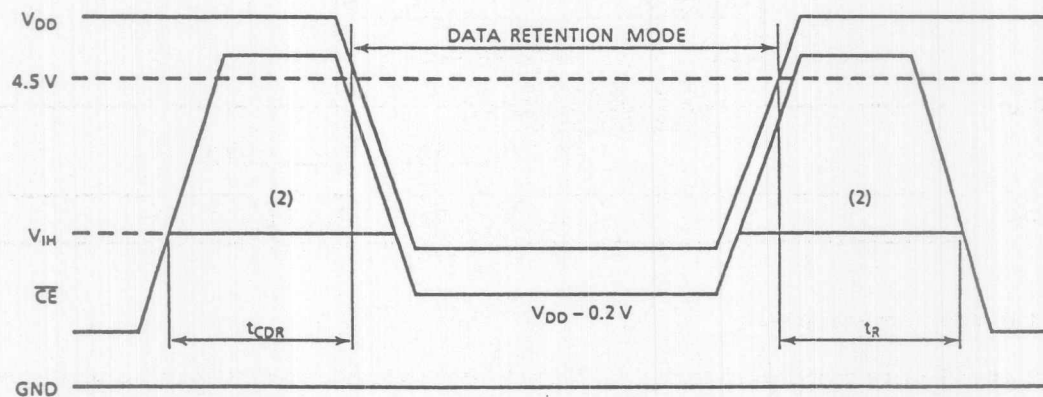
Notes:

1. R/W is high for read cycles.
2. If the $\overline{\text{CE}}$ low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the $\overline{\text{CE}}$ high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If $\overline{\text{OE}}$ is high during a write cycle, the outputs are in a high impedance state during this period.

Data Retention Characteristics ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DDS2}	Standby Current	$V_{DH} = 3.0\text{V}$	—	50	μA
		$V_{DH} = 5.5\text{V}$	—	100	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	μs
t_R	Recovery Time	$t_{RC(1)}$	—	—	

Note (1): Read Cycle Time

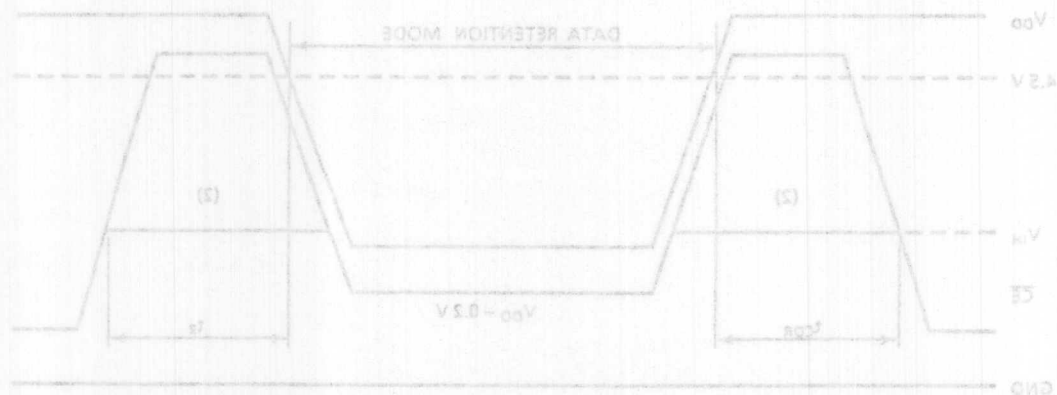
 $\overline{\text{CE}}$ Controlled Data Retention ModeNote (2): If the V_{IH} of $\overline{\text{CE}}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V .

Data Retention Characteristics ($T_s = 0 - 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	2.5	V
I_{DQ}	Standby Current	—	—	—	μA
				50	
				100	
t_{DQ}	Chip Dissipate to Data Retention Mode	0	—	—	μs
t_R	Recovery Time	(100)	—	—	μs

Note (1): Read Cycle Time

OE Controlled Data Retention Mode



Note (2): If the V_{CE} of OE is 2.5V in operation, I_{DQ} current flows during the period that the V_{DD} voltage is going down from 2.5V to 2.0V.

TC55257BPL/BFL/BSPL/BFTL/BTRL-85L/10L

SILICON GATE CMOS

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257BPL is a 262,144 bit CMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 85ns.

When \overline{CE} is a logical high, the device is placed in a low power standby mode in which the standby current is 2 μ A at room temperature. The TC55257BPL has two control inputs. Chip enable (\overline{CE}) allows for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. The TC55257BPL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required.

The TC55257BPL is offered in a standard dual-in-line 28-pin plastic package (0.6/0.3 inch width), a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 2 μ A (max.) at $T_a = 25^\circ\text{C}$
- Single 5V power supply
- Access time (max.)

	TC55257BPL/ BFL/BSPL/BFTL/ BTRL-85L	TC55257BPL/ BFL/BSPL/BFTL/ BTRL-10L
Access Time	85ns	100ns
Chip Enable Access Time	85ns	100ns
Output Enable Time	45ns	50ns

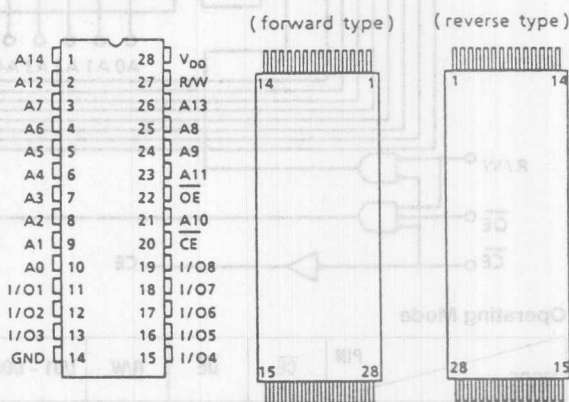
- Power down feature: \overline{CE}
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package
 - TC55257BPL : DIP28-P-600
 - TC55257BFL : SOP28-P-450
 - TC55257BSPL : DIP28-P-300B
 - TC55257BFTL : TSOP28-P
 - TC55257BTRL : TSOP28-P-A

Pin Names

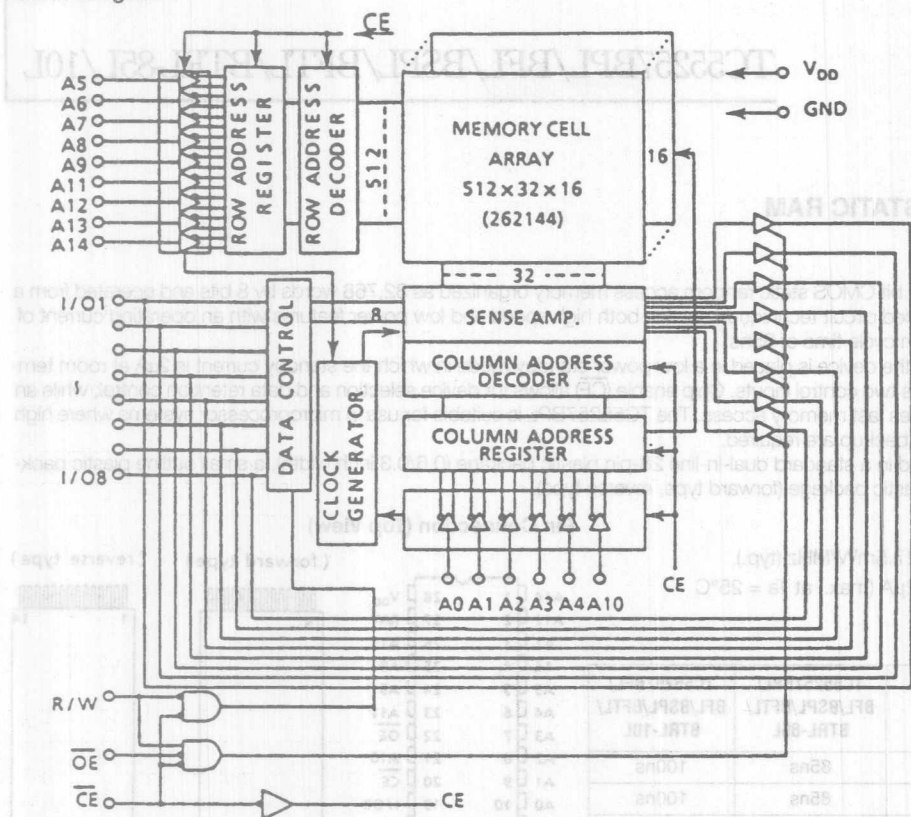
A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	\overline{OE}	A ₁₁	A ₉	A ₈	A ₁₃	R/W	V _{DD}	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	R/W	I/O1 - I/O8	POWER
Read		L	L	H	D _{OUT}	I _{DDO}
Write		L	*	L	D _{IN}	I _{DDO}
Output Deselect		L	H	H	High-Z	I _{DDO}
Standby		H	*	*	High-Z	I _{DS}

* For L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5* ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.8/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V with a pulse width of 50ns

** Package dependent: 0.6 inch 1.0W, 0.3 inch 0.8W, 0.45 inch 0.6W

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	—	V _{DD} + 0.3	
V _{IL}	Input Low Voltage	-0.3*	—	0.8	
V _{DH}	Data Retention Supply Voltage	2.0	—	5.5	

* -3.0V with a pulse width of 50ns

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}		—	—	±1.0	μA
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V _{IL} or $\overline{OE} = V_{IH}$ V _{OUT} = 0 ~ V _{DD}		—	—	±1.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V		-1.0	—	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V		4.0	—	—	mA
I _{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ R/W = V _{IH} Other Input = V _{IH} /V _{IL} I _{OUT} = 0mA	t _{cycle} = 1μs	—	10	—	mA
I _{DDO2}		$\overline{CE} = 0.2V$ R/W = V _{DD} - 0.2V Other Input = V _{DD} - 0.2V/0.2V I _{OUT} = 0mA	t _{cycle} = 1μs	—	5	—	
			t _{cycle} = Min. cycle	—	—	60	
				—	—	—	
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$		—	—	3	mA
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2V$ V _{DD} = 2.0V ~ 5.5V	Ta = 0 ~ 70°C	—	—	30	μA
			Ta = 25°C	—	—	2	

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, VDD = 5V±10%)

Read Cycle

Read Cycle						
SYMBOL	PARAMETER	TC55257BPL/BFL/BSPL/BFTL/BTRL				UNIT
		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	85	—	100	—	ns
t _{ACC}	Address Access Time	—	85	—	100	
t _{CO}	CE Access Time	—	85	—	100	
t _{OE}	Output Enable to Output in Valid	—	45	—	50	
t _{COE}	Chip Enable (CE) to Output in Low-Z	10	—	10	—	
t _{OEE}	Output Enable to Output in Low-Z	5	—	5	—	
t _{OD}	Chip Enable (CE) to Output in High-Z	—	30	—	50	
t _{ODO}	Output Enable to Output in High-Z	—	30	—	40	
t _{OH}	Output Data Hold Time	10	—	10	—	

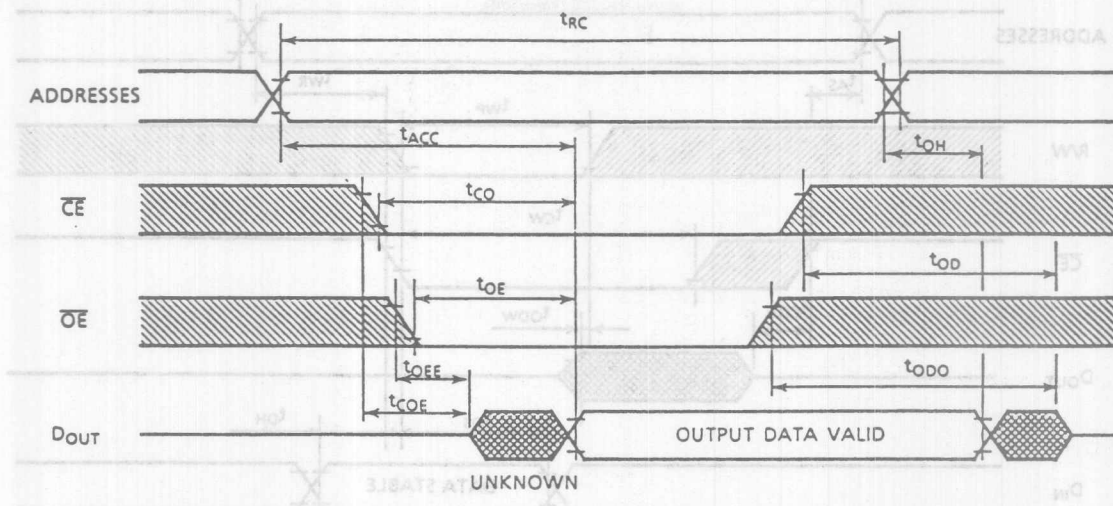
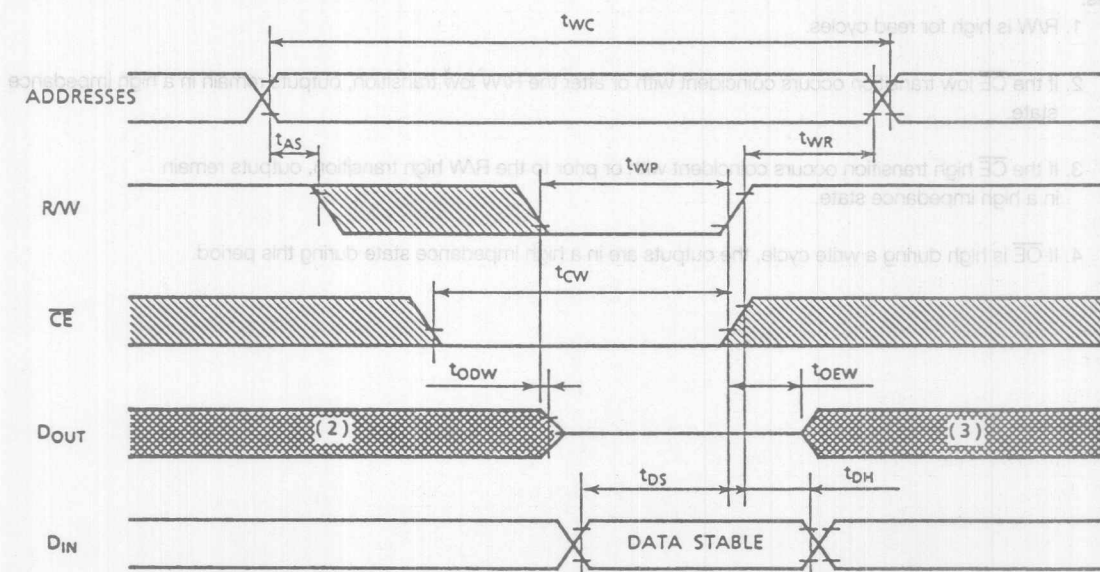
Write Cycle

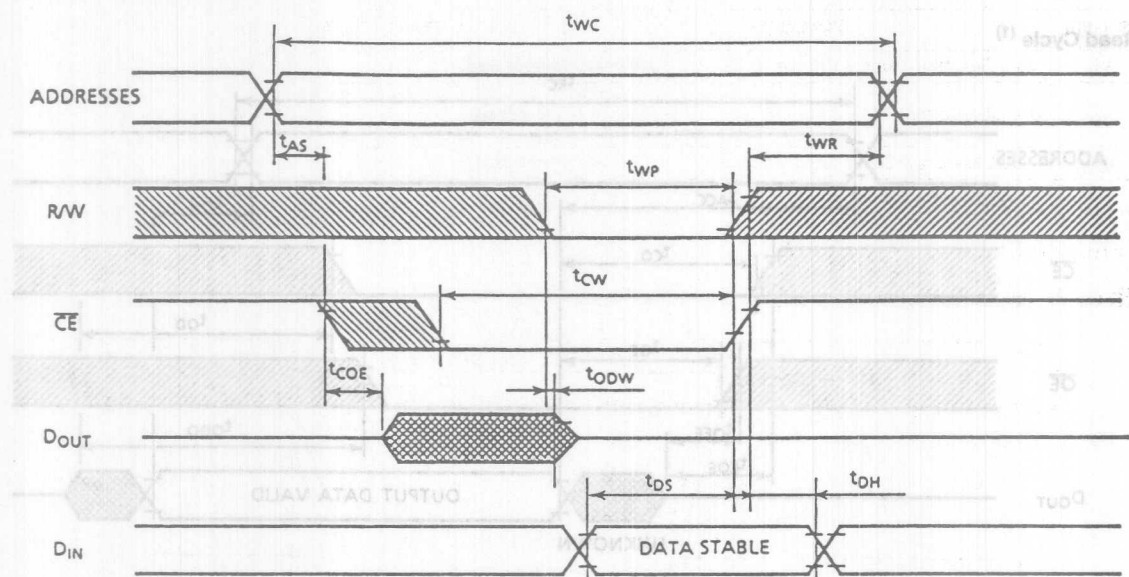
SYMBOL	PARAMETER	TC55257BPL/BFL/BSPL/BFTL/BTRL				UNIT
		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	85	—	100	—	ns
t _{WP}	Write Pulse Width	60	—	70	—	
t _{CW}	Chip Selection to End of Write	65	—	90	—	
t _{AS}	Address Setup Time	0	—	0	—	
t _{WR}	Write Recovery Time	5	—	5	—	
t _{ODW}	R/W to Output in High-Z	—	30	—	50	
t _{OEW}	R/W to Output in Low-Z	5	—	5	—	
t _{DS}	Data Setup Time	40	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	

AC Test Conditions

Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.2V/0.8V
Output Load	1 TTL Gate and C _L = 100pF

Timing Waveforms

Read Cycle ⁽¹⁾Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)

Write Cycle 2 ⁽⁴⁾ ($\overline{\text{CE}}$ Controlled Write)

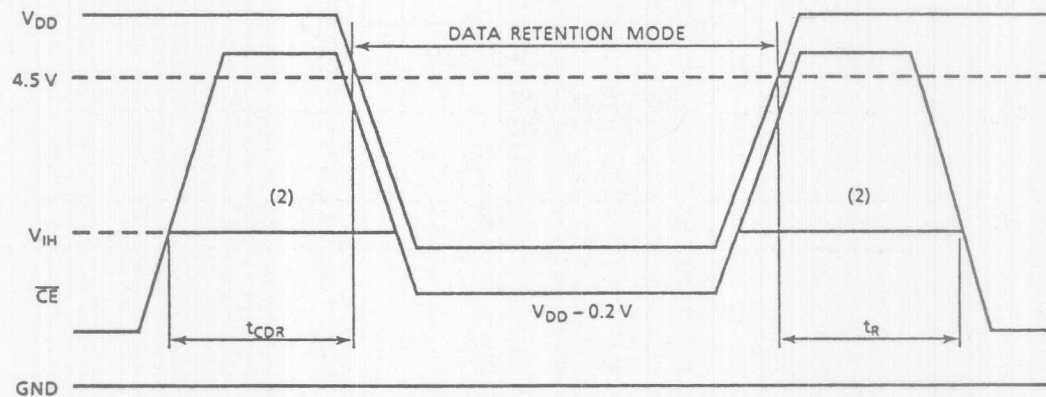
Notes:

1. R/W is high for read cycles.
2. If the $\overline{\text{CE}}$ low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the $\overline{\text{CE}}$ high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If $\overline{\text{OE}}$ is high during a write cycle, the outputs are in a high impedance state during this period.

Data Retention Characteristics ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DPS2}	Standby Current	$V_{DH} = 3.0\text{V}$	—	20	μA
		$V_{DH} = 5.5\text{V}$	—	30	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	μs
t_R	Recovery Time	$t_{RC(1)}$	—	—	

Note (1): Read Cycle Time

 $\overline{\text{CE}}$ Controlled Data Retention ModeNote (2): If the V_{IH} of $\overline{\text{CE}}$ is 2.2V in operation, I_{DPS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

Notes

TC55257BPL/BFL/BSPL/BFTL/BTRL-85/10(LT)

SILICON GATE CMOS

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257BPL is a 262,144 bit CMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 85ns.

When \overline{CE} is a logical high, the device is placed in a low power standby mode in which the standby current is 2 μ A at room temperature. The TC55257BPL has two control inputs. Chip enable (\overline{CE}) allows for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. The TC55257BPL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required. The TC55257BPL-(LT) has an operating temperature range of -20 ~ 70°C so it is suitable for use in low temperature applications.

The TC55257BPL is offered in a standard dual-in-line 28-pin plastic package (0.6/0.3 inch width), a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 100 μ A (max.)
- Single 5V power supply
- Access time (max.)

	TC55257BPL/ BFL/BSPL/BFTL/ BTRL-85(LT)	TC55257BPL/ BFL/BSPL/BFTL/ BTRL-10(LT)
Access Time	85ns	100ns
Chip Enable Access Time	85ns	100ns
Output Enable Time	45ns	50ns

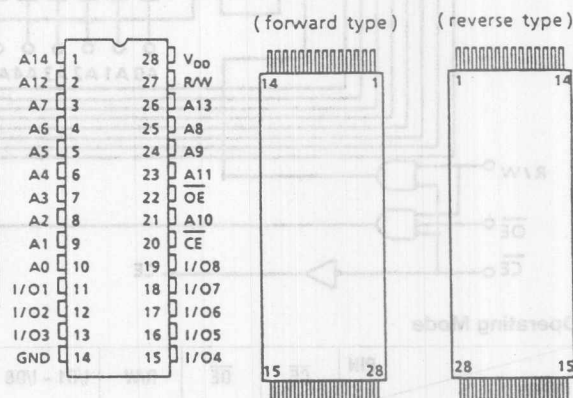
- Power down feature: \overline{CE}
- Data retention supply voltage: 2.0 ~ 5.5V
- Wide operating temperature: -20 ~ 70°C
- Inputs and outputs TTL compatible
- Package
 - TC55257BPL(LT) : DIP28-P-600
 - TC55257BFL(LT) : SOP28-P-450
 - TC55257BSPL(LT) : DIP28-P-300B
 - TC55257BFTL(LT) : TSOP28-P
 - TC55257BTRL(LT) : TSOP28-P-A

Pin Names

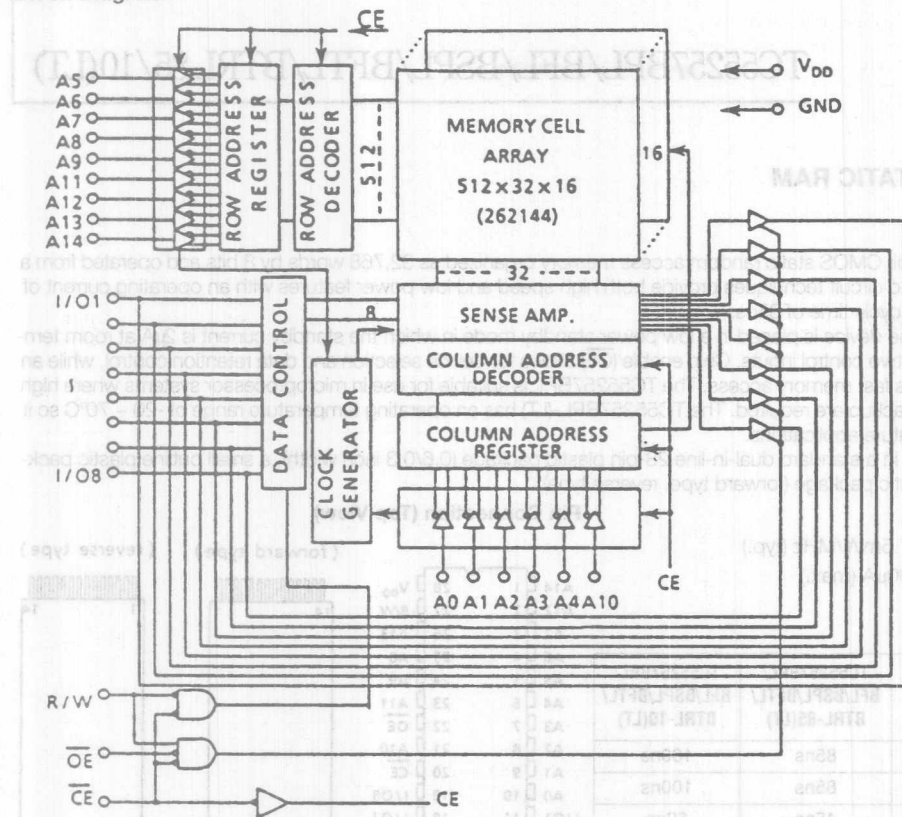
A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	\overline{OE}	A ₁₁	A ₉	A ₈	A ₁₃	R/W	V _{DD}	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A ₂	A ₁	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}		A ₁₀

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	R/W	I/O1 ~ I/O8	POWER
Read		L	L	H	D _{OUT}	I _{DDO}
Write		L	*	L	D _{IN}	I _{DDO}
Output Deselect		L	H	H	High-Z	I _{DDO}
Standby		H	*	*	High-Z	I _{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
V_{IO}	Input and Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0/0.8/0.6**	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	-20 ~ 70	°C

* -3.0V with a pulse width of 50ns

** Package dependent: 0.6 inch 1.0W, 0.3 inch 0.8W, 0.45 inch 0.6W

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	—	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

* -3.0V with a pulse width of 50ns

DC Characteristics ($T_a = -20 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}		—	—	±1.0	μA
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V _{IL} or $\overline{OE} = V_{IH}$ V _{OUT} = 0 ~ V _{DD}		—	—	±1.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V		-1.0	—	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V		4.0	—	—	mA
I _{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ R/W = V _{IH} Other Input = V _{IH} /V _{IL}	t _{cycle} = 1μs	—	10	—	mA
		I _{OUT} = 0mA	t _{cycle} = Min. cycle	—	—	70	
I _{DDO2}		$\overline{CE} = 0.2V$ R/W = V _{DD} - 0.2V Other Input = V _{DD} - 0.2V/0.2V	t _{cycle} = 1μs	—	5	—	
		I _{OUT} = 0mA	t _{cycle} = Min. cycle	—	—	60	
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$		—	—	3	mA
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2V$ V _{DD} = 2.0V ~ 5.5V	Ta = -20 ~ 70°C Ta = 25°C	—	— 2	100 —	μA

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -20 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55257BPL/BFL/BSPL/BFTL/BTRL				UNIT
		-85(LT)		-10(LT)		
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	85	—	100	—	ns
t _{ACC}	Address Access Time	—	85	—	100	
t _{CO}	$\overline{\text{CE}}$ Access Time	—	85	—	100	
t _{OE}	Output Enable to Output in Valid	—	45	—	50	
t _{COE}	Chip Enable ($\overline{\text{CE}}$) to Output in Low-Z	5	—	5	—	
t _{OEE}	Output Enable to Output in Low-Z	0	—	0	—	
t _{OD}	Chip Enable ($\overline{\text{CE}}$) to Output in High-Z	—	30	—	50	
t _{ODO}	Output Enable to Output in High-Z	—	30	—	40	
t _{OH}	Output Data Hold Time	10	—	10	—	

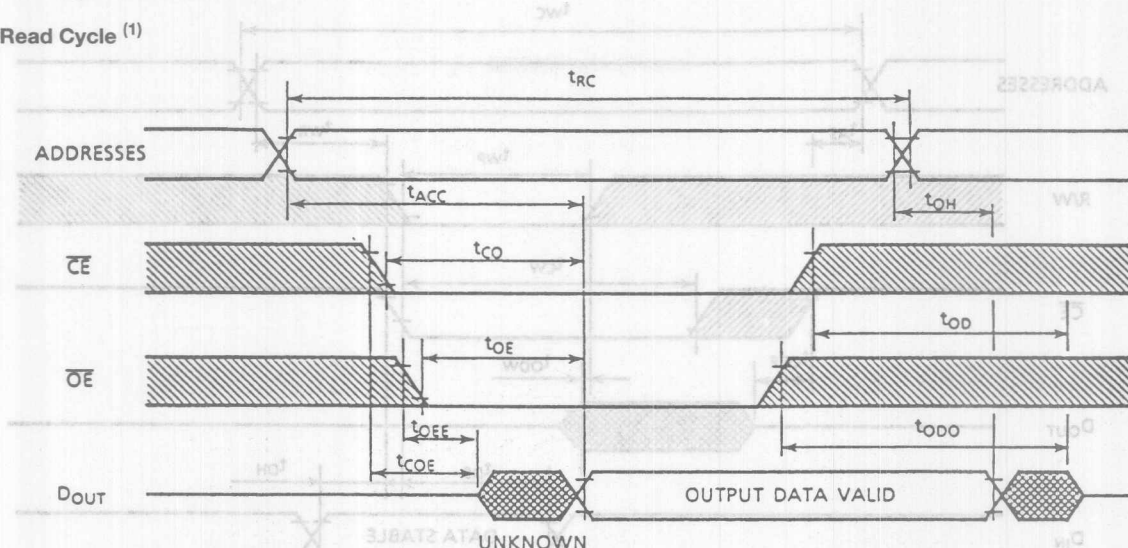
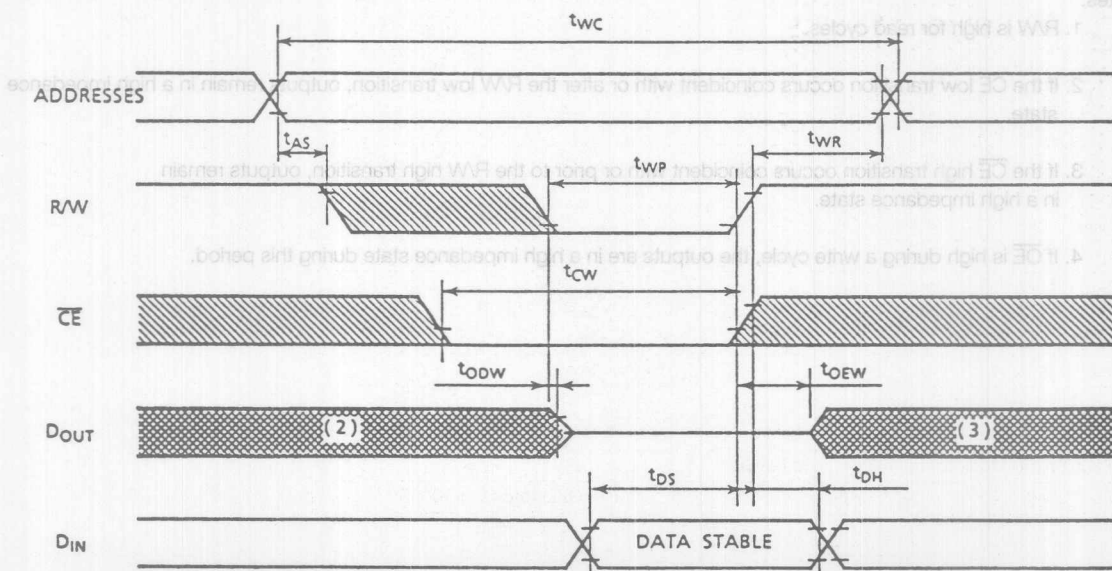
Write Cycle

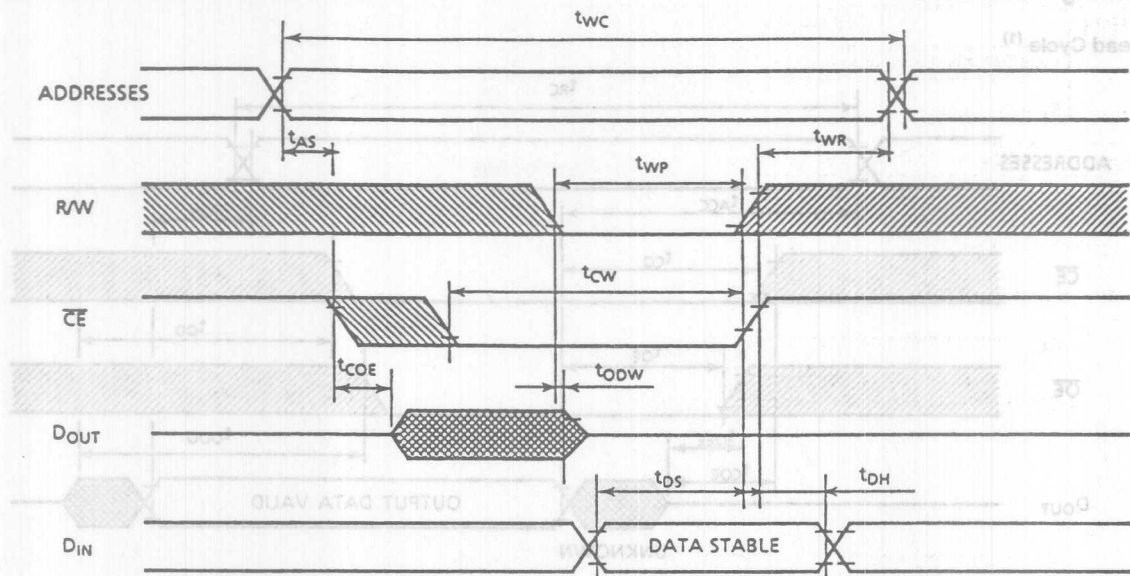
SYMBOL	PARAMETER	TC55257BPL/BFL/BSPL/BFTL/BTRL				UNIT
		-85(LT)		-10(LT)		
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	85	—	100	—	ns
t _{WP}	Write Pulse Width	60	—	70	—	
t _{CW}	Chip Selection to End of Write	65	—	90	—	
t _{AS}	Address Setup Time	0	—	0	—	
t _{WR}	Write Recovery Time	5	—	5	—	
t _{ODW}	R/W to Output in High-Z	—	30	—	50	
t _{OEW}	R/W to Output in Low-Z	0	—	0	—	
t _{DS}	Data Setup Time	40	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	

AC Test Conditions

Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	2.4V/0.6V
Output Timing Measurement Reference Levels	2.2V/0.8V
Output Load	1 TTL Gate and C _L = 100pF

Timing Waveforms

Read Cycle ⁽¹⁾Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)

Write Cycle 2 ⁽⁴⁾ (\overline{CE} Controlled Write)

Notes:

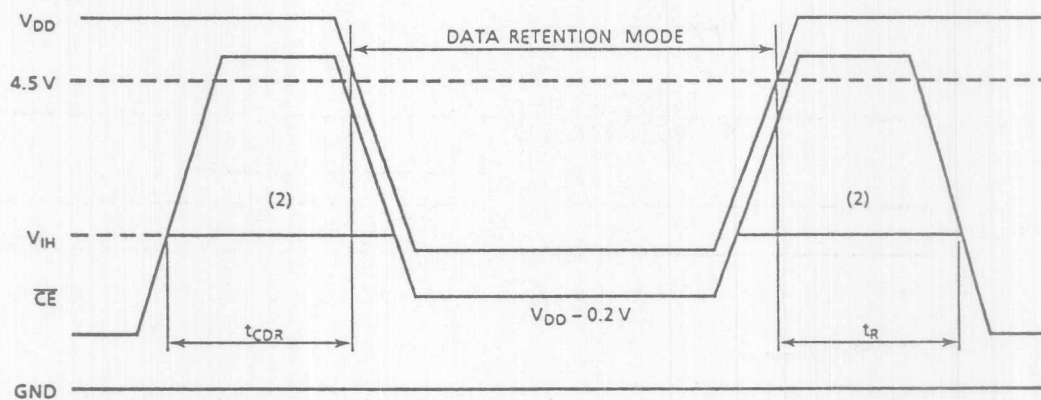
1. R/W is high for read cycles.
2. If the \overline{CE} low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the \overline{CE} high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.

Data Retention Characteristics (Ta = -20 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DDS2}	Standby Current	$V_{DH} = 3.0V$	—	50	μA
		$V_{DH} = 5.5V$	—	100	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	μs
t_R	Recovery Time	$t_{RC(1)}$	—	—	

Note (1): Read Cycle Time

\overline{CE} Controlled Data Retention Mode



Note (2): If the V_{IH} of \overline{CE} is 2.4V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.6V.

Notes

TC55257BPL/BFL/BSPL/BFTL/BTRL-85L/10L(LT)

SILICON GATE CMOS

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257BPL is a 262,144 bit CMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 85ns.

When \overline{CE} is a logical high, the device is placed in a low power standby mode in which the standby current is $2\mu A$ at room temperature. The TC55257BPL has two control inputs. Chip enable (\overline{CE}) allows for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. The TC55257BPL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required. The TC55257BPL-L(LT) has an operating temperature range of $-20 \sim 70^\circ C$ so it is suitable for use in low temperature applications.

The TC55257BPL is offered in a standard dual-in-line 28-pin plastic package (0.6/0.3 inch width), a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: $2\mu A$ at $T_a = 25^\circ C$ (max.)
- Single 5V power supply
- Access time (max.)

	TC55257BPL/BFL/BSPL/BFTL/BTRL	
	-85L(LT)	-10L(LT)
Access Time	85ns	100ns
Chip Enable Access Time	85ns	100ns
Output Enable Time	45ns	50ns

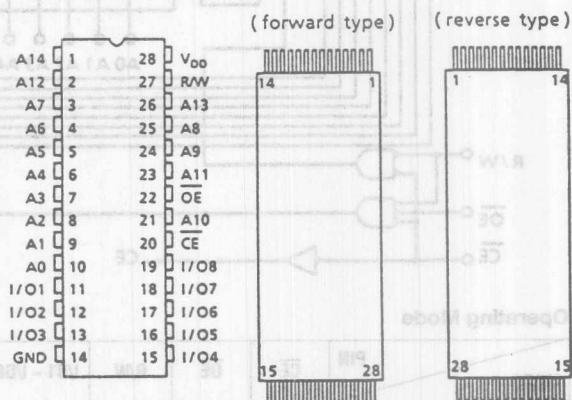
- Power down feature: \overline{CE}
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Wide operating temperature: $-20 \sim 70^\circ C$
- Package
 TC55257BPL-L(LT) : DIP28-P-600
 TC55257BFL-L(LT) : SOP28-P-450
 TC55257BSPL-L(LT) : DIP28-P-300B
 TC55257BFTL-L(LT) : TSOP28-P
 TC55257BTRL-L(LT) : TSOP28-P-A

Pin Names

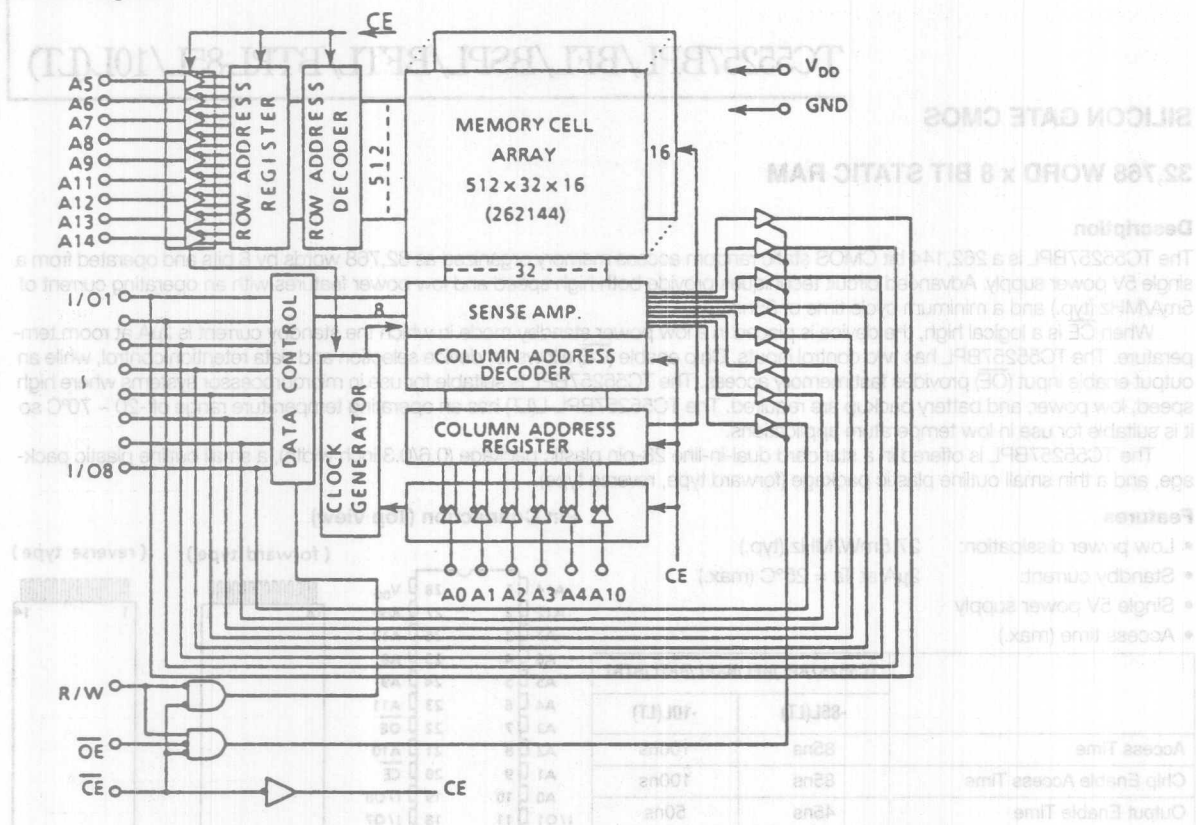
A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	\overline{OE}	A ₁₁	A ₉	A ₈	A ₁₃	R/W	V_{DD}	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE	PIN	CE	OE	R/W	I/O1 ~ I/O8	POWER
Read		L	L	H	D _{OUT}	I _{DDO}
Write		L	*	L	D _{IN}	I _{DDO}
Output Deselect		L	H	H	High-Z	I _{DDO}
Standby		H	*	*	High-Z	I _{DDs}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3 ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.8/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	-20 ~ 70	°C

* -3.0V with a pulse width of 50ns

** Package dependent; 0.6 inch 1.0W, 0.3 inch 0.8W, 0.45 inch 0.6W

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	—	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

* -3.0V with a pulse width of 50ns

DC Characteristics ($T_a = -20 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-1.0	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	4.0	—	—	mA
I_{DDO1}	Operating Current	$\overline{CE} = V_{IL}$, $R/W = V_{DD} - 0.2V$, $I_{OUT} = 0\text{mA}$ Other Input = V_{IH}/V_{IL}	$t_{\text{cycle}} = 1\mu\text{s}$		—	—
			$t_{\text{cycle}} = \text{Min. cycle}$		—	—
					10	—
					70	—
I_{DDO2}	Operating Current	$\overline{CE} = 0.2V$, $R/W = V_{DD} - 0.2V$, $I_{OUT} = 0\text{mA}$ Other Input = $V_{DD} - 0.2V/0.2V$	$t_{\text{cycle}} = 1\mu\text{s}$		—	5
			$t_{\text{cycle}} = \text{Min. cycle}$		—	—
					—	60
					—	—
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	3	mA
		$\overline{CE} = V_{DD} - 0.2V$	—	—	30	—
I_{DDS2}		$V_{DD} = 2.0V \sim 5.5V$	—	—	2	μA

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -20 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55257BPL/BFL/BSPL/BFTL/BTRL				UNIT
		-85L(LT)		-10L(LT)		
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	85	—	100	—	ns
t _{ACC}	Address Access Time	—	85	—	100	
t _{CO}	CE Access Time	—	85	—	100	
t _{OE}	Output Enable to Output in Valid	—	45	—	50	
t _{COE}	Chip Enable (CE) to Output in Low-Z	5	—	5	—	
t _{OEE}	Output Enable to Output in Low-Z	0	—	0	—	
t _{OD}	Chip Enable (CE) to Output in High-Z	—	30	—	50	
t _{ODO}	Output Enable to Output in High-Z	—	30	—	40	
t _{OH}	Output Data Hold Time	10	—	10	—	

Write Cycle

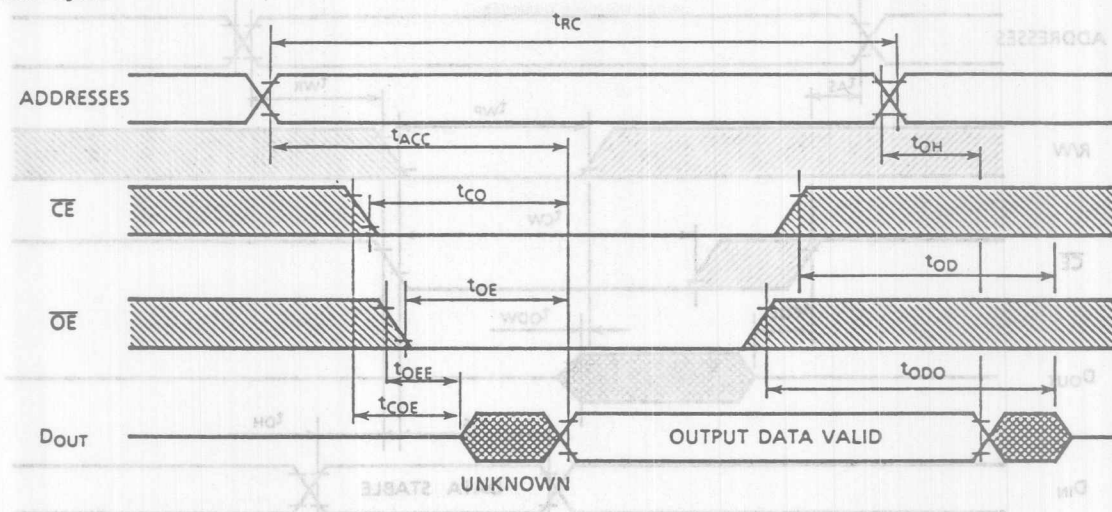
SYMBOL	PARAMETER	TC55257BPL/BFL/BSPL/BFTL/BTRL				UNIT
		-85L(LT)		-10L(LT)		
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	85	—	100	—	ns
t _{WP}	Write Pulse Width	60	—	70	—	
t _{CW}	Chip Selection to End of Write	65	—	90	—	
t _{AS}	Address Setup Time	0	—	0	—	
t _{WR}	Write Recovery Time	5	—	5	—	
t _{ODW}	R/W to Output in High-Z	—	30	—	50	
t _{OEW}	R/W to Output in Low-Z	0	—	0	—	
t _{DS}	Data Setup Time	40	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	

AC Test Conditions

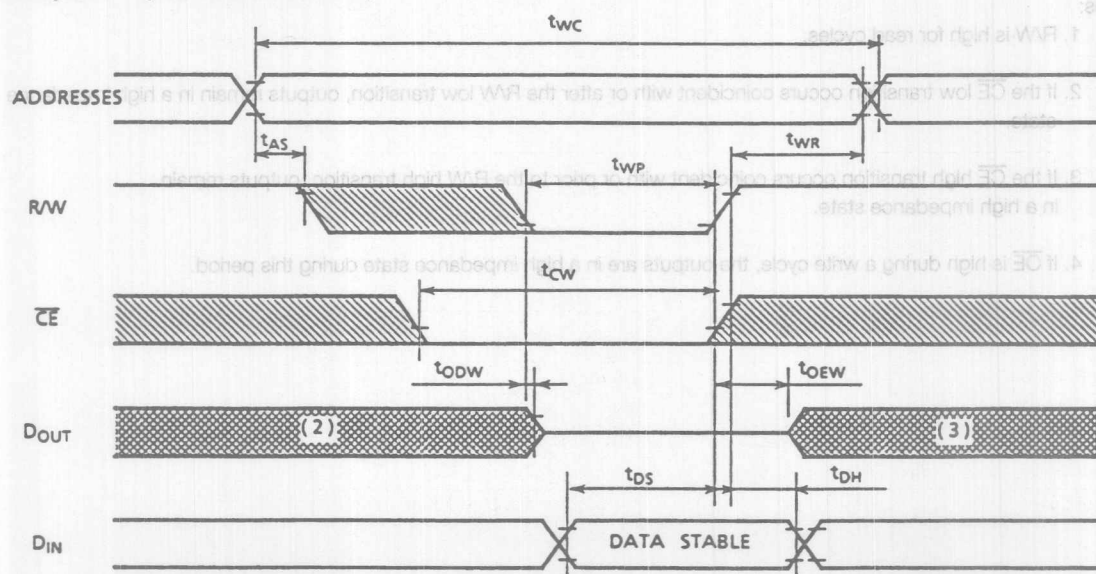
Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	2.4V/0.6V
Output Timing Measurement Reference Levels	2.2V/0.8V
Output Load	1 TTL Gate and C _L = 100pF

Timing Waveforms

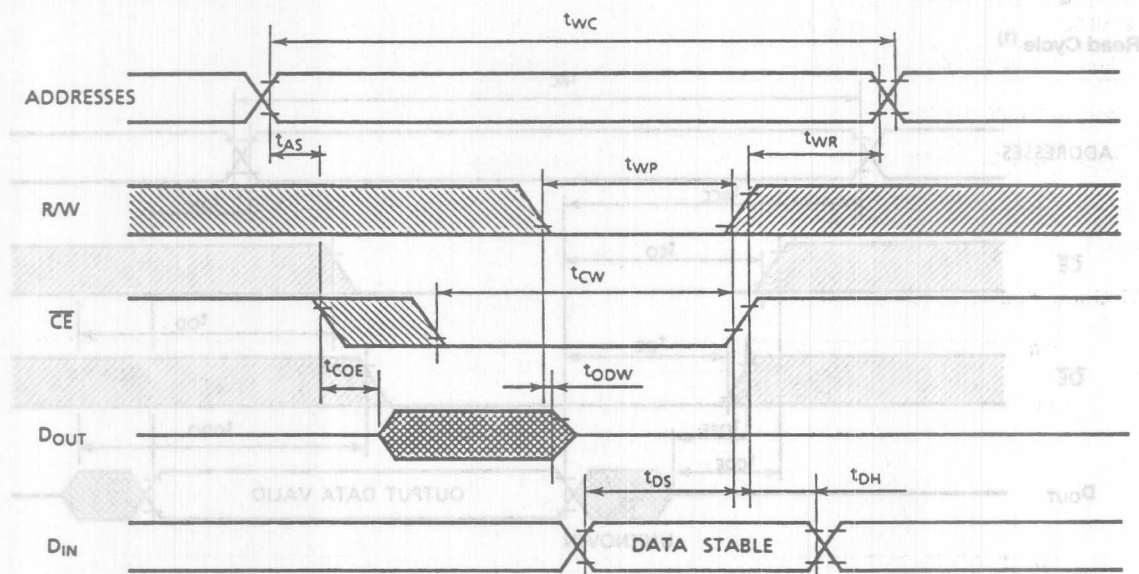
Read Cycle ⁽¹⁾



Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)



Write Cycle 2 ⁽⁴⁾ ($\overline{\text{CE}}$ Controlled Write)



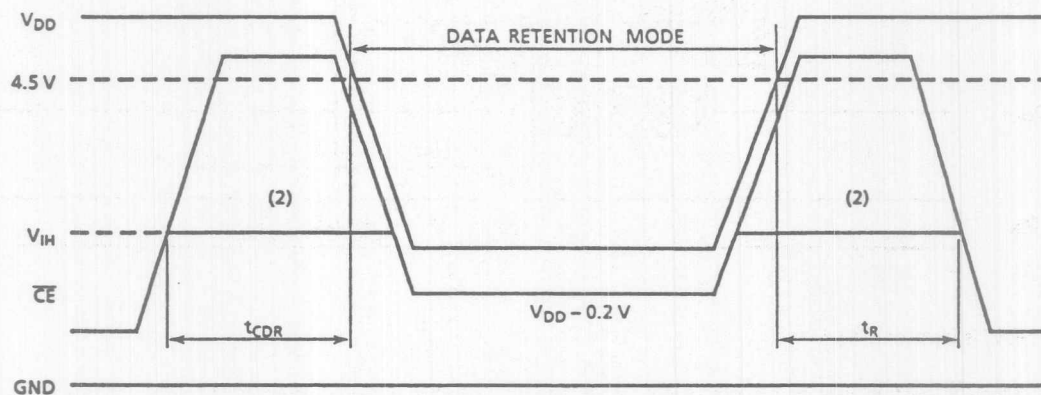
Notes:

1. R/W is high for read cycles.
2. If the $\overline{\text{CE}}$ low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the $\overline{\text{CE}}$ high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If $\overline{\text{OE}}$ is high during a write cycle, the outputs are in a high impedance state during this period.

Data Retention Characteristics (Ta = -20 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DSS2}	Standby Current	$V_{DH} = 3.0V$	—	20	μA
		$V_{DH} = 5.5V$	—	30	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	μs
t_R	Recovery Time	$t_{RC(1)}$	—	—	

Note (1): Read Cycle Time

 \overline{CE} Controlled Data Retention ModeNote (2): If the V_{IH} of \overline{CE} is 2.4V in operation, I_{DSS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.6V.

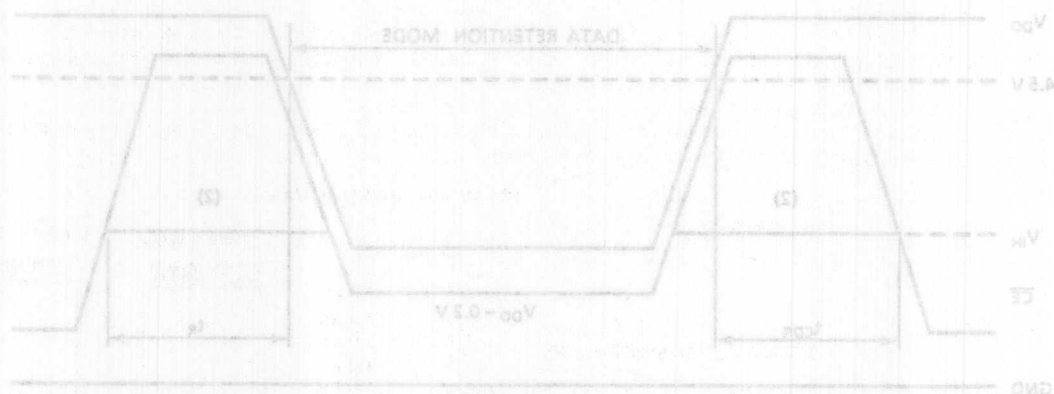
Notes

Data Retention Characteristics ($T_a = -50 - 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Data Retention Supply Voltage	5.0	—	5.5	V
I _{loss}	Standby Current	—	—	20	μA
	$V_{DD} = 3.0\text{V}$	—	—	30	
I _{DD1}	Chip Dissipate to Data Retention Mode	—	—	—	—
t _{RE}	Recovery Time	(sec)	—	—	μs

Note (1): Read Cycle Time

CE Controlled Data Retention Mode

Note (2): If the V_{CE} of CE is 3.0V in operation, I_{loss} current flows during the period that the V_{DD} voltage is going down from 4.5V to 3.0V.

TC55257BPL/BFL/BSPL/BFTL/BTRL-85L/10L(LV)

SILICON GATE CMOS

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257BPL is a 262,144 bit CMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 85ns.

When \overline{CE} is a logical high, the device is placed in a low power standby mode in which the standby current is 2 μ A at room temperature. The TC55257BPL has two control inputs. Chip enable (\overline{CE}) allows for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. The TC55257BPL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required.

The TC55257BPL is offered in a standard dual-in-line 28-pin plastic package (0.6/0.3 inch width), a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 2 μ A (max.) at Ta = 25°C
- Single 5V power supply
- Access time (max.):

	TC55257BPL/BFL/BSPL/BFTL/BTRL	
	-85L(LV)	-10L(LV)
Access Time	85ns	100ns
Chip Enable Access Time	85ns	100ns
Output Enable Time	45ns	50ns

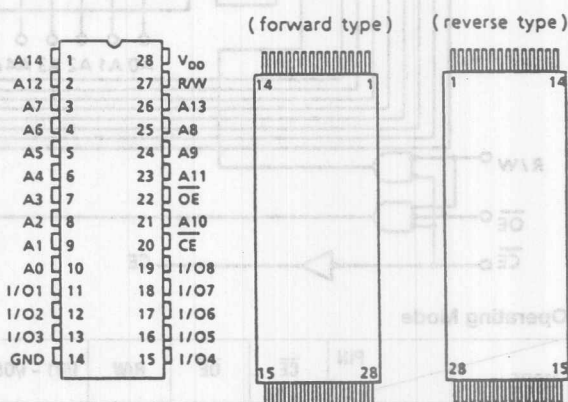
- Power down feature: \overline{CE}
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package
 - TC55257BPL : DIP28-P-600
 - TC55257BFL : SOP28-P-450
 - TC55257BSPL : DIP28-P-300B
 - TC55257BFTL : TSOP28-P
 - TC55257BTRL : TSOP28-P-A

Pin Names

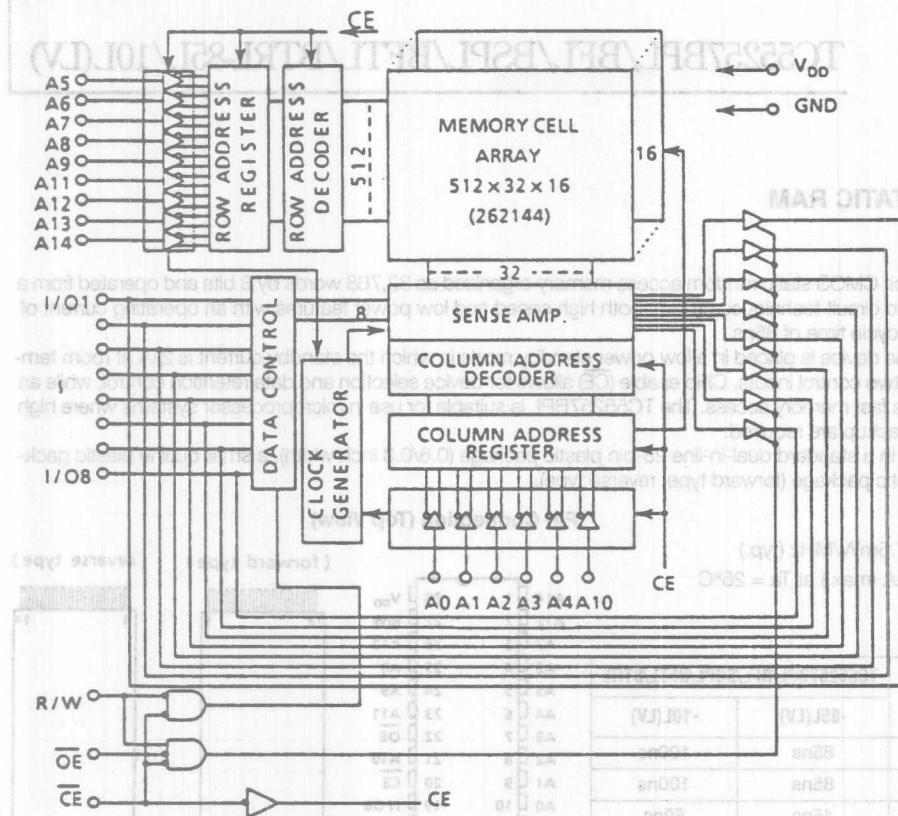
A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	\overline{OE}	A ₁₁	A ₉	A ₈	A ₁₃	R/W	V _{DD}	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	R/W	I/O1 ~ I/O8	POWER
Read		L	L	H	D _{OUT}	I _{DDO}
Write		L	*	L	D _{IN}	I _{DDO}
Output Deselect		L	H	H	High-Z	I _{DDO}
Standby		H	*	*	High-Z	I _{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5* ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.8/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V with a pulse width of 50ns

** Package dependent: 0.6 inch 1.0W, 0.3 inch 0.8W, 0.45 inch 0.6W

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	—	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

* -3.0V with a pulse width of 50ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-1.0	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	4.0	—	—	mA
I_{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ $R/W = V_{IH}$ Other Input = V_{IH}/V_{IL} $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 1\mu\text{s}$	—	10	—
I_{DDO2}		$\overline{CE} = 0.2V$ $R/W = V_{DD} - 0.2V$ Other Input = $V_{DD} - 0.2V/0.2V$ $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 1\mu\text{s}$	—	5	—
			$t_{\text{cycle}} = \text{Min. cycle}$	—	—	70
			$t_{\text{cycle}} = \text{Min. cycle}$	—	—	60
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	3	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2V$ $V_{DD} = 2.0V \sim 5.5V$	$T_a = 0 \sim 70^\circ\text{C}$	—	—	30
			$T_a = 25^\circ\text{C}$	—	—	2

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55257BPL/BFL/BSPL/BFTL/BTRL				UNIT
		-85L(LV)		-10L(LV)		
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	85	—	100	—	ns
t _{ACC}	Address Access Time	—	85	—	100	
t _{CO}	$\overline{\text{CE}}$ Access Time	—	85	—	100	
t _{OE}	Output Enable to Output in Valid	—	45	—	50	
t _{COE}	Chip Enable ($\overline{\text{CE}}$) to Output in Low-Z	10	—	10	—	
t _{OEE}	Output Enable to Output in Low-Z	5	—	5	—	
t _{OD}	Chip Enable ($\overline{\text{CE}}$) to Output in High-Z	—	30	—	50	
t _{ODO}	Output Enable to Output in High-Z	—	30	—	40	
t _{OH}	Output Data Hold Time	10	—	10	—	

Write Cycle

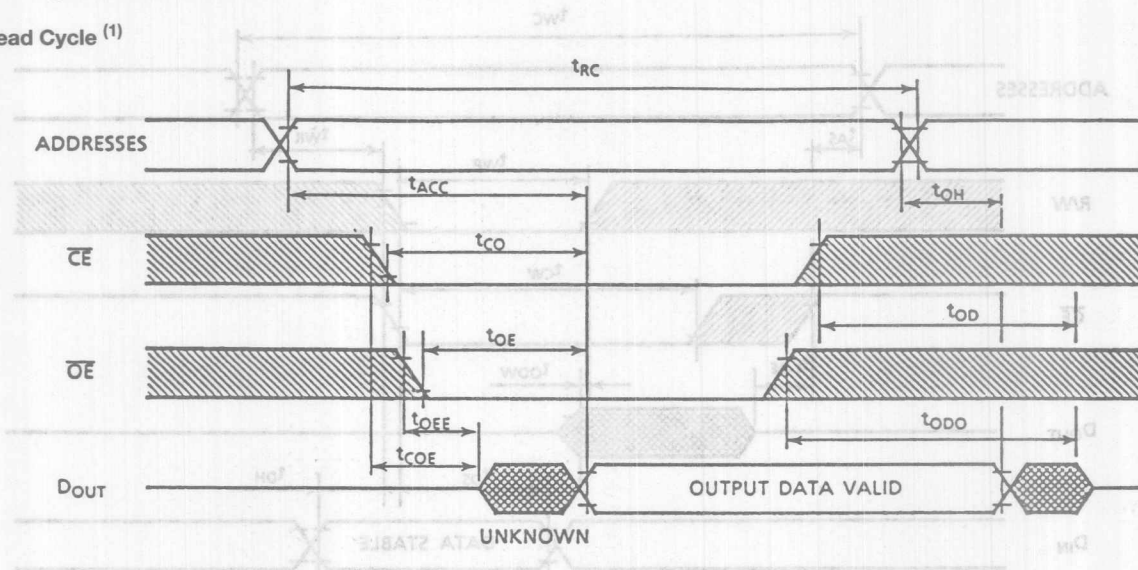
SYMBOL	PARAMETER	TC55257BPL/BFL/BSPL/BFTL/BTRL				UNIT
		-85L(LV)		-10L(LV)		
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	85	—	100	—	ns
t _{WP}	Write Pulse Width	60	—	70	—	
t _{CW}	Chip Selection to End of Write	65	—	90	—	
t _{AS}	Address Setup Time	0	—	0	—	
t _{WR}	Write Recovery Time	5	—	5	—	
t _{ODW}	R/W to Output in High-Z	—	30	—	50	
t _{OEW}	R/W to Output in Low-Z	5	—	5	—	
t _{DS}	Data Setup Time	40	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	

AC Test Conditions

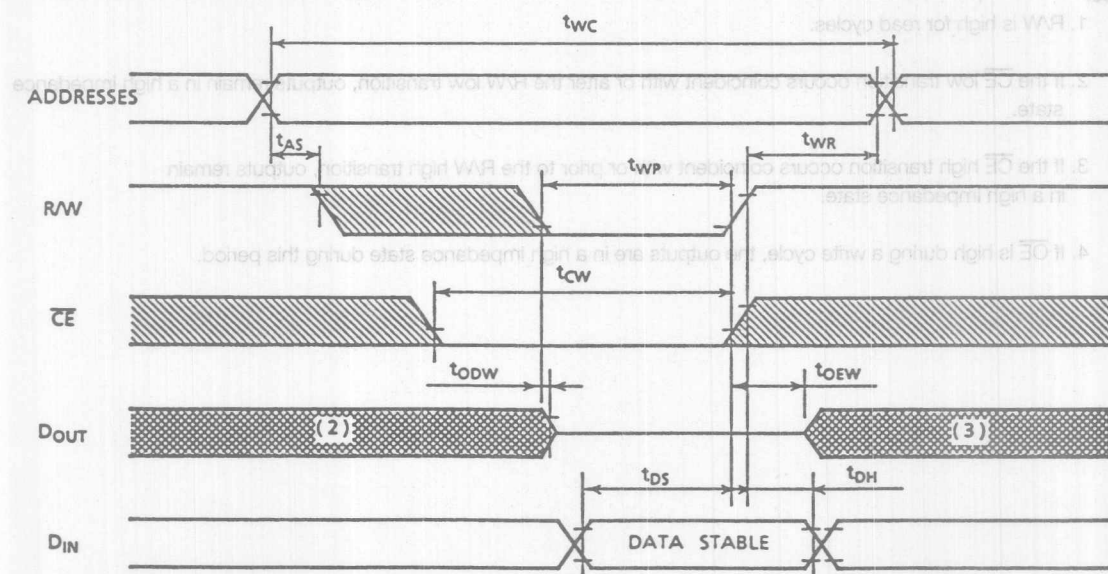
Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.2V/0.8V
Output Load	1 TTL Gate and C _L = 100pF

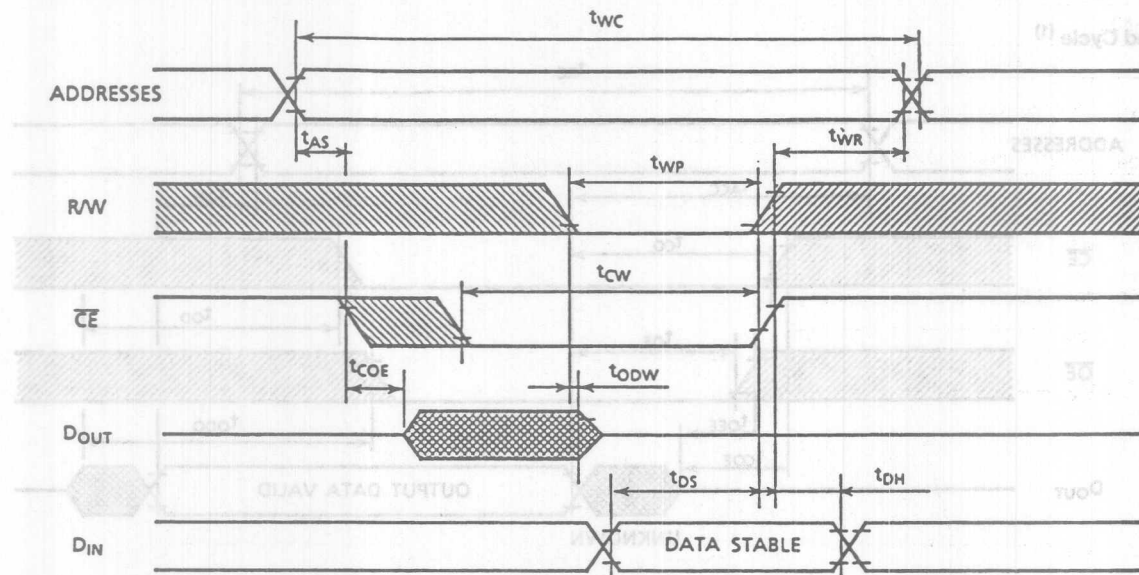
Timing Waveforms

Read Cycle ⁽¹⁾



Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)



Write Cycle 2 ⁽⁴⁾ (\overline{CE} Controlled Write)


Notes:

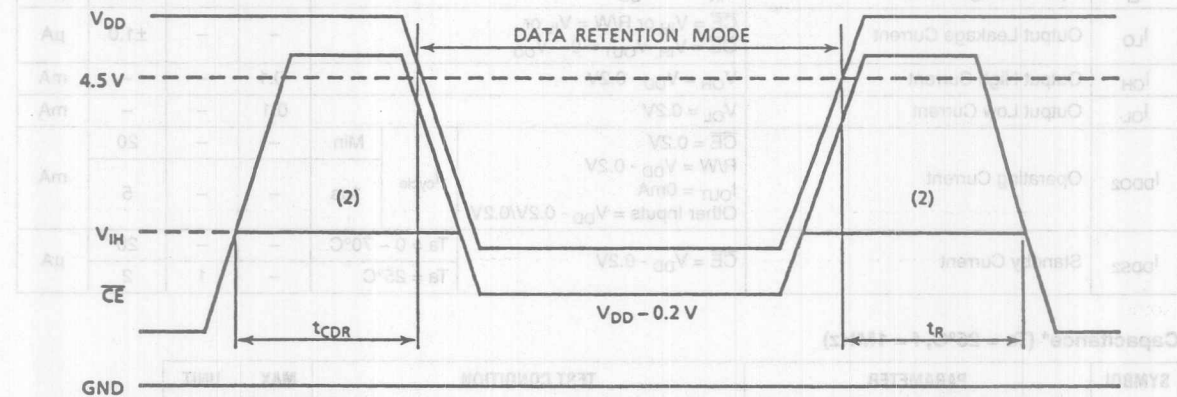
1. R/W is high for read cycles.
2. If the \overline{CE} low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the \overline{CE} high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.

Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DDs2}	Standby Current	$V_{DH} = 3.0V$	—	20	μA
		$V_{DH} = 5.5V$	—	30	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	μs
t_R	Recovery Time	$t_{RC(1)}$	—	—	—

Note (1): Read Cycle Time

\overline{CE} Controlled Data Retention Mode



Note (2): If the V_{IH} of \overline{CE} is 2.2V in operation, I_{DDs1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

3V Operation

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	2.7	3.0	3.3	V
V _{IH}	Input High Voltage	V _{DD} - 0.2	—	V _{DD} + 0.3	
V _{IL}	Input Low Voltage	-0.3	—	0.2	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 3V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}	—	—	±1.0	μA
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V _{IL} or $\overline{OE} = V_{IH}$, V _{OUT} = 0 ~ V _{DD}	—	—	±1.0	μA
I _{OH}	Output High Current	V _{OH} = V _{DD} - 0.2V	-0.1	—	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.2V	0.1	—	—	mA
I _{DDO2}	Operating Current	$\overline{CE} = 0.2V$ R/W = V _{DD} - 0.2V I _{OUT} = 0mA Other Inputs = V _{DD} - 0.2V/0.2V	Min.	—	—	20
			t _{cycle} 1μs	—	—	5
I _{DDS2}	Standby Current	$\overline{CE} = V_{DD} - 0.2V$	Ta = 0 ~ 70°C	—	—	20
			Ta = 25°C	—	1	2

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	10	

*This parameter is periodically sampled and is not 100% tested.

3V Operation

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 3V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	200	—	ns
t_{ACC}	Address Access Time	—	200	
t_{CO}	\overline{CE} Access Time	—	200	
t_{OE}	Output Enable to Output in Valid	—	100	
t_{COE}	Chip Enable (\overline{CE}) to Output in Low-Z	10	—	
t_{OEE}	Output Enable to Output in Low-Z	5	—	
t_{OD}	Chip Enable (\overline{CE}) to Output in High-Z	—	100	
t_{ODO}	Output Enable to Output in High-Z	—	80	
t_{OH}	Output Data Hold Time	10	—	

Write Cycle

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	200	—	ns
t_{WP}	Write Pulse Width	150	—	
t_{CW}	Chip Selection to End of Write	180	—	
t_{AS}	Address Setup Time	0	—	
t_{WR}	Write Recovery Time	5	—	
t_{ODW}	R/W to Output in High-Z	—	100	
t_{OEW}	R/W to Output in Low-Z	5	—	
t_{DS}	Data Setup Time	90	—	
t_{DH}	Data Hold Time	0	—	

AC Test Conditions

Input Pulse Levels	$V_{DD} - 0.2V/0.2V$
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	$C_L = 100\text{pF}$

Notes

TC55257BPI/BFI/BSPI/BFTI/BTRI-10L

SILICON GATE CMOS

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257BPI is a 262,144 bit CMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 100ns.

When \overline{CE} is a logical high, the device is placed in a low power standby mode in which the standby current is 2 μ A at room temperature. The TC55257BPI has two control inputs: Chip enable (\overline{CE}) allows for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. The TC55257BPI is suitable for use in microprocessor systems where high speed, low power, and battery backup are required. The TC55257BPI has an operating temperature range of -40 ~ 85°C so it is suitable for use in wide operating temperature systems.

The TC55257BPI is offered in a standard dual-in-line 28-pin plastic package (0.6/0.3 inch width), a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 2 μ A at $T_a = 25^\circ\text{C}$ (max.)
- Single 5V power supply
- Access time (max.)

	TC55257BPI/BFI/BSPI/BFTI/BTRI-10L
Access Time	100ns
Chip Enable Access Time	100ns
Output Enable Time	50ns

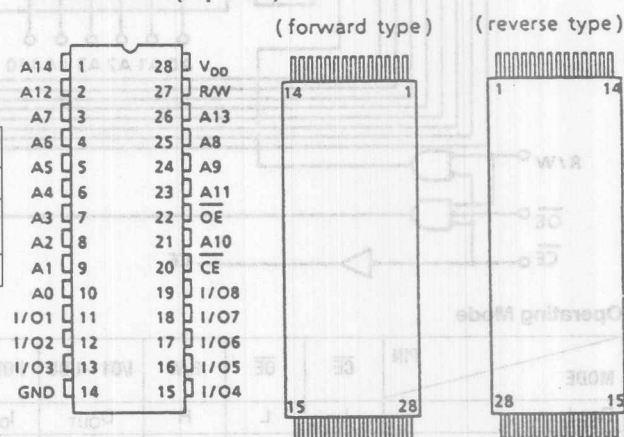
- Power down feature: \overline{CE}
- Data retention supply voltage: 2.0 ~ 5.5V
- Wide operating temperature: -40 ~ 85°C
- Inputs and outputs TTL compatible
- Package
 - TC55257BPI : DIP28-P-600
 - TC55257BFI : SOP28-P-450
 - TC55257BSPI : DIP28-P-300B
 - TC55257BFTI : TSOP28-P
 - TC55257BTRI : TSOP28-P-A

Pin Names

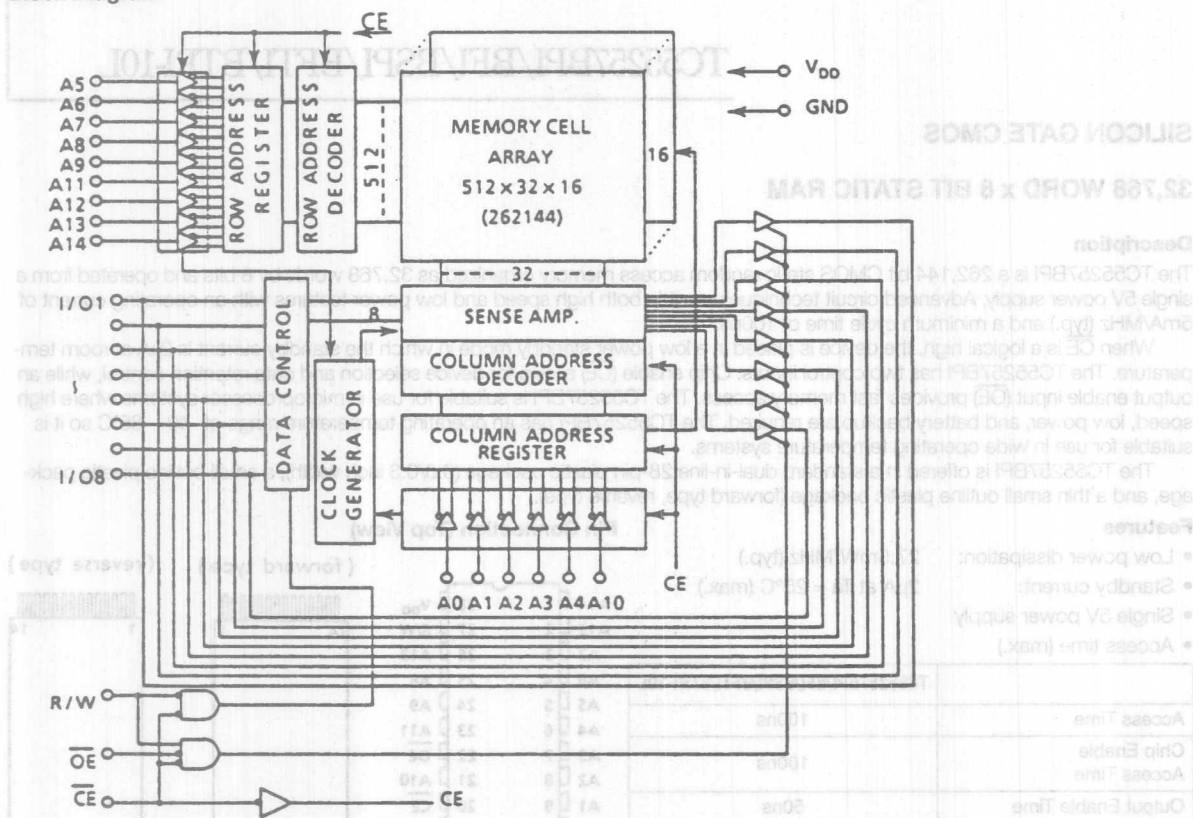
A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	\overline{OE}	A ₁₁	A ₉	A ₈	A ₁₃	R/W	V _{DD}	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	R/W	I/O1 ~ I/O8	POWER
Read		L	L	H	D _{OUT}	I _{DD}
Write		L	*	L	D _{IN}	I _{DD}
Output Deselect		L	H	H	High-Z	I _{DD}
Standby		H	*	*	High-Z	I _{DS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5* ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.8/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	-40 ~ 85	°C

* -3.0V with a pulse width of 50ns

** Package dependent: 0.6 inch 1.0W, 0.3 inch 0.8W, 0.45 inch 0.6W

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	—	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

* -3.0V with a pulse width of 50ns

DC Characteristics ($T_a = -40 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-1.0	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	4.0	—	—	mA
I_{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ $R/W = V_{IH}$ Other Input = V_{IH}/V_{IL} $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 1\mu\text{s}$	—	10	mA
			$t_{\text{cycle}} = \text{Min. cycle}$	—	70	
I_{DDO2}	Operating Current	$\overline{CE} = 0.2V$ $R/W = V_{DD} - 0.2V$ Other Input = $V_{DD} - 0.2V/0.2V$ $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 1\mu\text{s}$	—	5	mA
			$t_{\text{cycle}} = \text{Min. cycle}$	—	60	
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	3	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2V$ $V_{DD} = 2.0V \sim 5.5V$	$T_a = -40 \sim 85^\circ\text{C}$	—	50	μA
			$T_a = 25^\circ\text{C}$	—	2	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -40 ~ 85°C, VDD = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55257BPI/BFI/BSPI/BFTI/BTRI-10L		UNIT
		MIN.	MAX.	
t _{RC}	Read Cycle Time	100	—	
t _{ACC}	Address Access Time	—	100	
t _{CO}	\overline{CE} Access Time	—	100	
t _{OE}	Output Enable to Output in Valid	—	50	
t _{COE}	Chip Enable (\overline{CE}) to Output in Low-Z	5	—	ns
t _{OEE}	Output Enable to Output in Low-Z	0	—	
t _{OD}	Chip Enable (\overline{CE}) to Output in High-Z	—	50	
t _{ODO}	Output Enable to Output in High-Z	—	40	
t _{OH}	Output Data Hold Time	10	—	

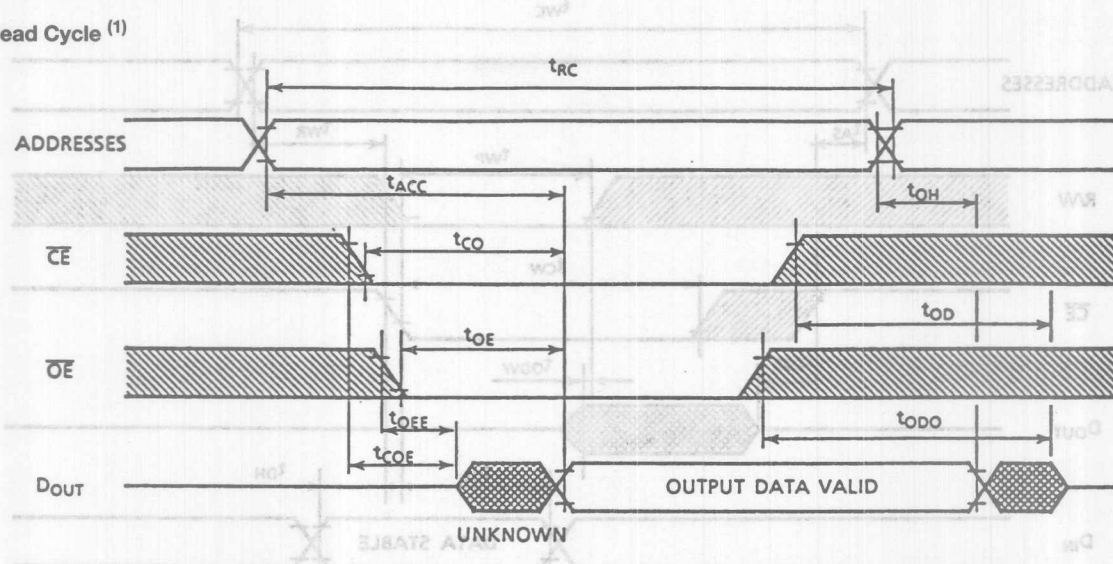
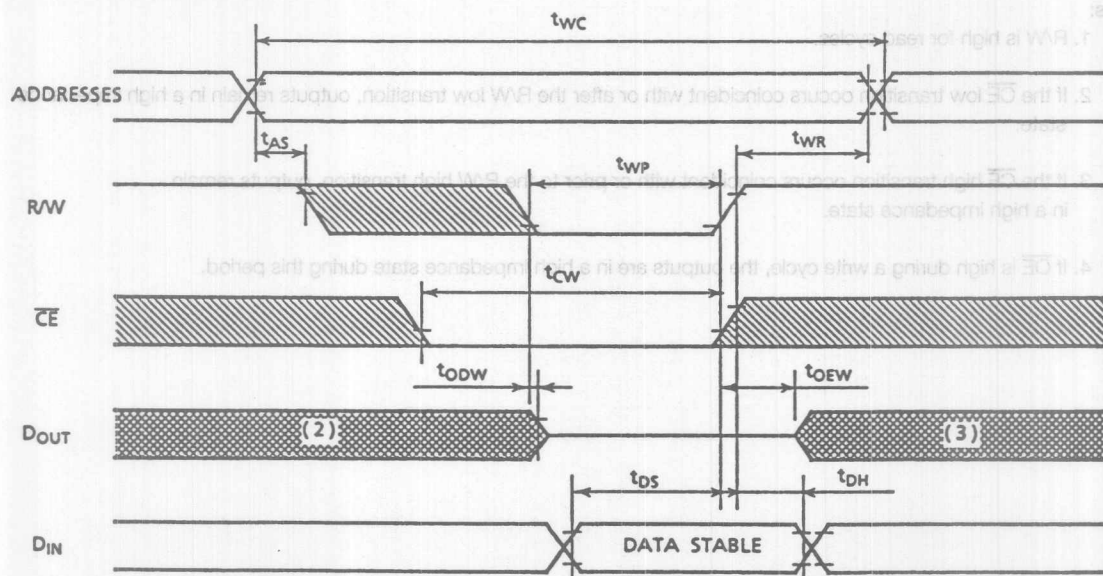
Write Cycle

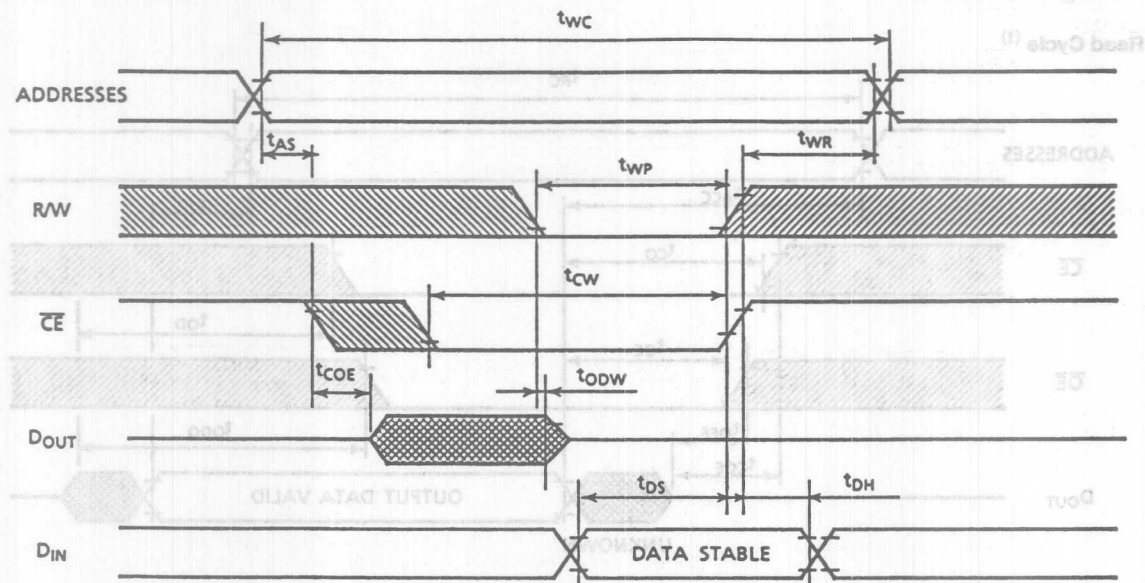
SYMBOL	PARAMETER	TC55257BPI/BFI/BSPI/BFTI/BTRI-10L		UNIT
		MIN.	MAX.	
t _{WC}	Write Cycle Time	100	—	
t _{WP}	Write Pulse Width	70	—	
t _{CW}	Chip Selection to End of Write	90	—	
t _{AS}	Address Setup Time	0	—	
t _{WR}	Write Recovery Time	5	—	ns
t _{ODW}	R/W to Output in High-Z	—	50	
t _{OEW}	R/W to Output in Low-Z	0	—	
t _{DS}	Data Setup Time	40	—	
t _{DH}	Data Hold Time	0	—	

AC Test Conditions

Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	2.4V/0.6V
Output Timing Measurement Reference Levels	2.2V/0.8V
Output Load	1 TTL Gate and C _L = 100pF

Timing Waveforms

Read Cycle ⁽¹⁾Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)

Write Cycle 2 ⁽⁴⁾ (\overline{CE} Controlled Write)

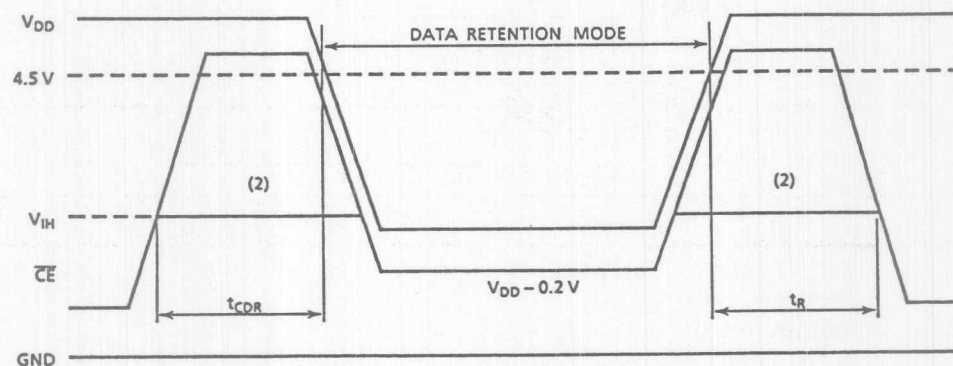
Notes:

1. R/W is high for read cycles.
2. If the \overline{CE} low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the \overline{CE} high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.

Data Retention Characteristics ($T_a = -40 \sim 85^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DDS2}	Standby Current	$V_{DH} = 3.0\text{V}$	—	30	μA
		$V_{DH} = 5.5\text{V}$	—	50	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	μs
t_R	Recovery Time	$t_{RC(1)}$	—	—	

Note (1): Read Cycle Time

 $\overline{\text{CE}}$ Controlled Data Retention Mode

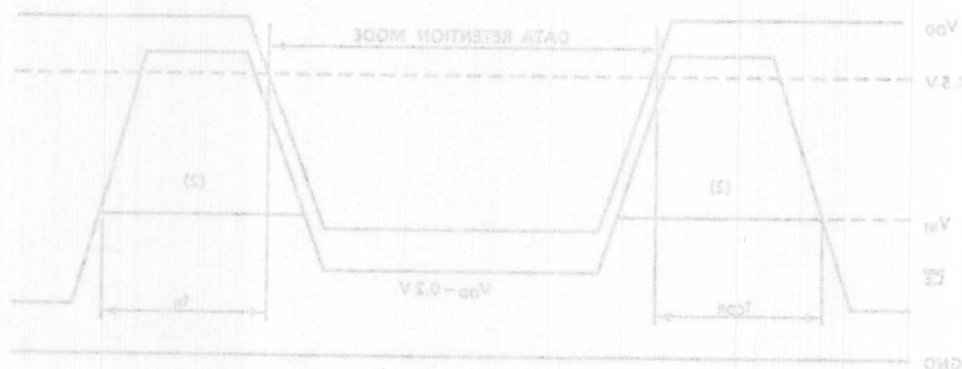
Note (2): If the V_{IH} of $\overline{\text{CE}}$ is 2.4V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.6V.

Notes

Data Retention Characteristics ($T_a = -40 - 85^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{OH}	Data Retention Supply Voltage	2.0	—	2.5	V
I_{OBS}	Standby Current	—	—	30	μA
		—	—	50	
I_{DDR}	Chip Dissipat. to Data Retention Mode	0	—	—	W
		$I_{(DDT)}$	—	—	
t_R	Recovery Time	—	—	—	μs

Note (1): Read Cycle Time

 $\overline{\text{CE}}$ Controlled Data Retention ModeNote (2): If the V_{OH} of $\overline{\text{CE}}$ is 2.4V in operation, I_{OBS} current flows during the period that the V_{DD} voltage is going down from 2.5V to 2.0V.

TC55257CPL/CFL/CSPL/CFTL/CTRL-70/85/10

PRELIMINARY

SILICON GATE CMOS

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257CPL is a 262,144 bit CMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns.

When \overline{CE} is a logical high, the device is placed in a low power standby mode in which the standby current is 2 μ A at room temperature. The TC55257CPL has two control inputs. Chip enable (\overline{CE}) allows for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. The TC55257CPL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required.

The TC55257CPL is offered in a standard dual-in-line 28-pin plastic package (0.6/0.3 inch width), a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 100 μ A (max.)
- Single 5V power supply
- Access time (max.)

	TC55257CPL/CFL/CSPL/CFTL/CTRL		
	-70	-85	-10
Access Time	70ns	85ns	100ns
\overline{CE} Access Time	70ns	85ns	100ns
\overline{OE} Access Time	35ns	45ns	50ns

- Power down feature: \overline{CE}
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package
 - TC55257CPL : DIP28-P-600
 - TC55257CFL : SOP28-P-450
 - TC55257CSPL : DIP28-P-300B
 - TC55257CFTL : TSOP28-P
 - TC55257CTRL : TSOP28-P-A

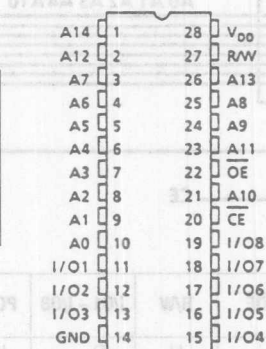
Pin Names

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground

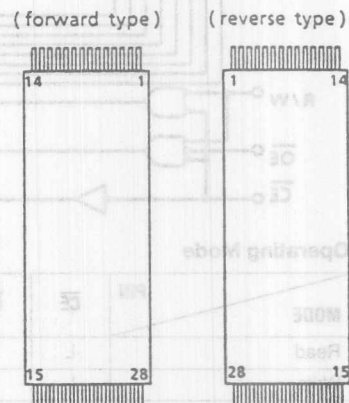
PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	\overline{OE}	A ₁₁	A ₉	A ₈	A ₁₃	R/W	V _{DD}	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀

Pin Connection (Top View)

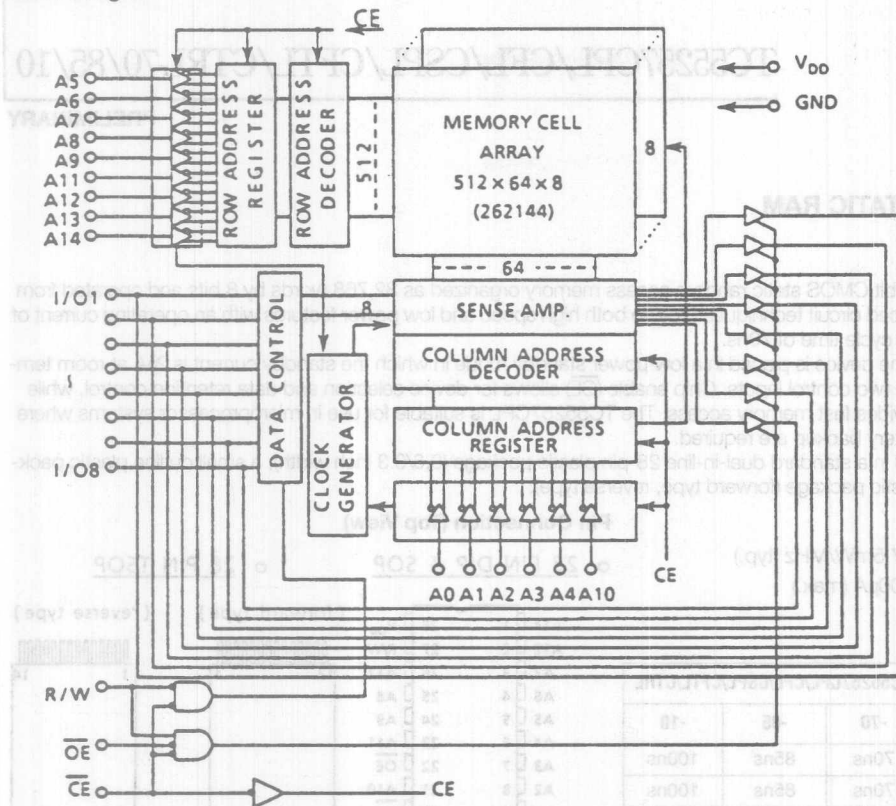
28 PIN DIP & SOP



28 PIN TSOP



Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	R/W	I/O1 ~ I/O8	POWER
Read		L	L	H	D _{OUT}	I _{DD}
Write		L	*	L	D _{IN}	I _{DD}
Output Deselect		L	H	H	High-Z	I _{DD}
Standby		H	*	*	High-Z	I _{DD}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3 ~ 7.0	V
V _{IO}	Input and Output Voltage	-0.5* ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.8/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V with a pulse width of 50ns

** Package dependent: 0.6 inch 1.0W, 0.3 inch 0.8W, 0.45 inch 0.6W

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	—	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

* -3.0V with a pulse width of 50ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-1.0	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	4.0	—	—	mA
I_{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ $R/W = V_{IH}$ Other Input = V_{IH}/V_{IL} $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 1\mu\text{s}$	—	10	—
			$t_{\text{cycle}} = \text{Min. cycle}$	—	—	70
I_{DDO2}	Operating Current	$\overline{CE} = 0.2V$ $R/W = V_{DD} - 0.2V$ Other Input = $V_{DD} - 0.2V/0.2V$ $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 1\mu\text{s}$	—	5	—
			$t_{\text{cycle}} = \text{Min. cycle}$	—	—	60
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	3	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2V$ $V_{DD} = 2.0V \sim 5.5V$	$T_a = 0 \sim 70^\circ\text{C}$	—	100	μA
			$T_a = 25^\circ\text{C}$	—	2	—

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55257CPL/CFL/CSPL/CFTL/CTRL						UNIT
		-70		-85		-10		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	70	—	85	—	100	—	ns
t _{ACC}	Address Access Time	—	70	—	85	—	100	
t _{CO}	CE Access Time	—	70	—	85	—	100	
t _{OE}	Output Enable to Output in Valid	—	35	—	45	—	50	
t _{COE}	Chip Enable (CE) to Output in Low-Z	10	—	10	—	10	—	
t _{OEE}	Output Enable to Output in Low-Z	5	—	5	—	5	—	
t _{OD}	Chip Enable (CE) to Output in High-Z	—	25	—	30	—	50	
t _{ODO}	Output Enable to Output in High-Z	—	25	—	30	—	40	
t _{OH}	Output Data Hold Time	10	—	10	—	10	—	

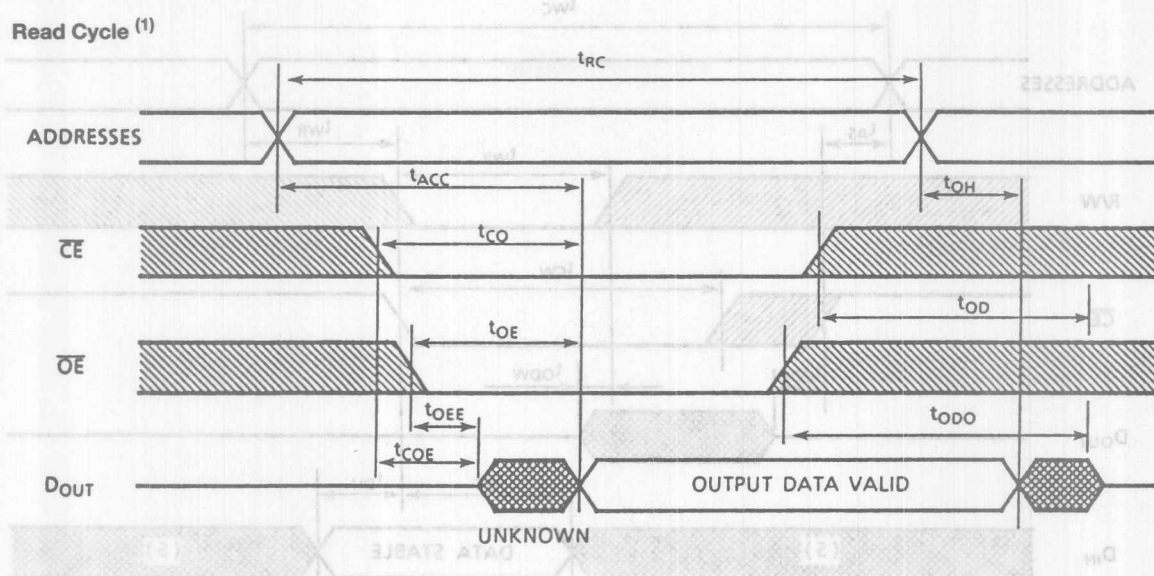
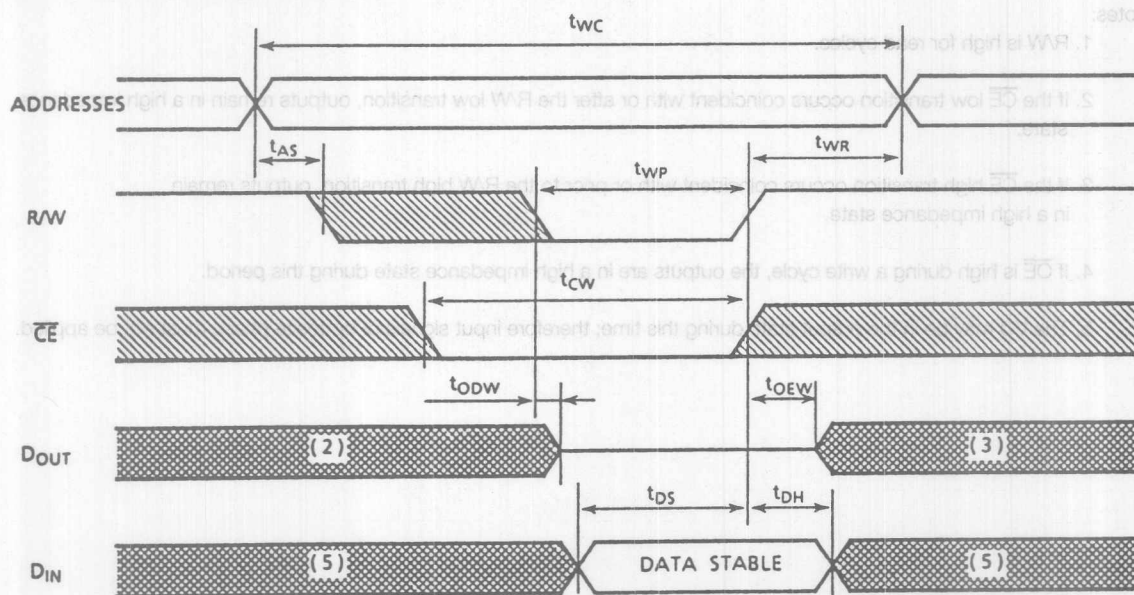
Write Cycle

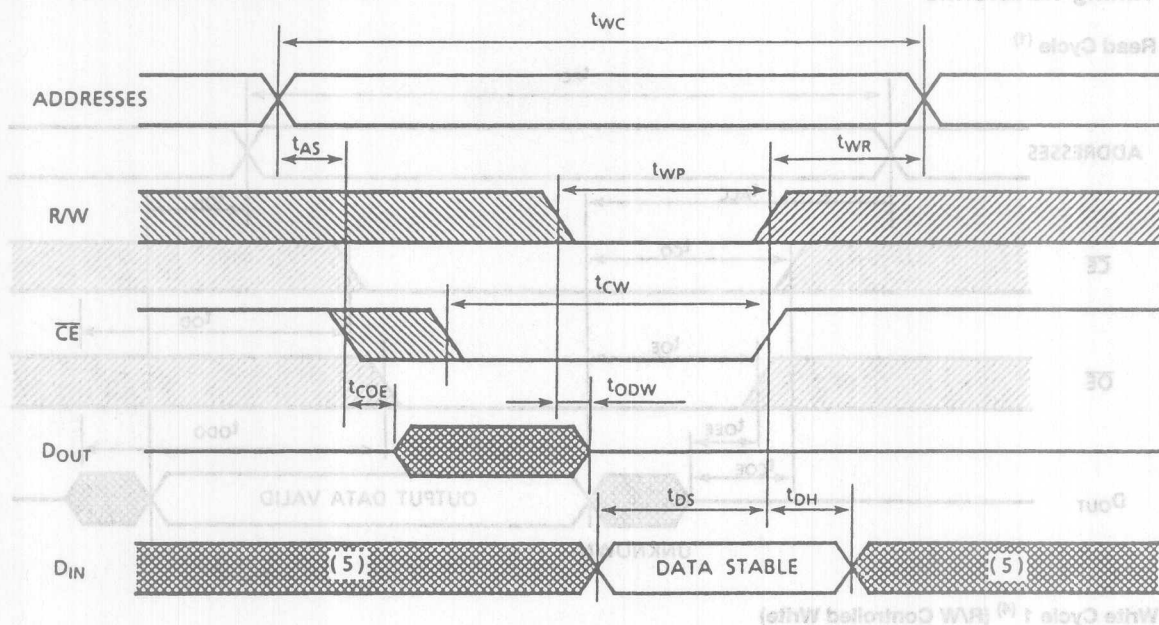
SYMBOL	PARAMETER	TC55257CPL/CFL/CSPL/CFTL/CTRL						UNIT
		-70		-85		-10		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	70	—	85	—	100	—	ns
t _{WP}	Write Pulse Width	50	—	60	—	70	—	
t _{CW}	Chip Selection to End of Write	60	—	65	—	90	—	
t _{AS}	Address Setup Time	0	—	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	
t _{ODW}	R/W to Output in High-Z	—	25	—	30	—	50	
t _{OEW}	R/W to Output in Low-Z	5	—	5	—	5	—	
t _{DS}	Data Setup Time	30	—	40	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	

AC Test Conditions

Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and C _L = 100pF

Timing Waveforms

Read Cycle ⁽¹⁾Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)

Write Cycle 2 ⁽⁴⁾ (\overline{CE} Controlled Write)

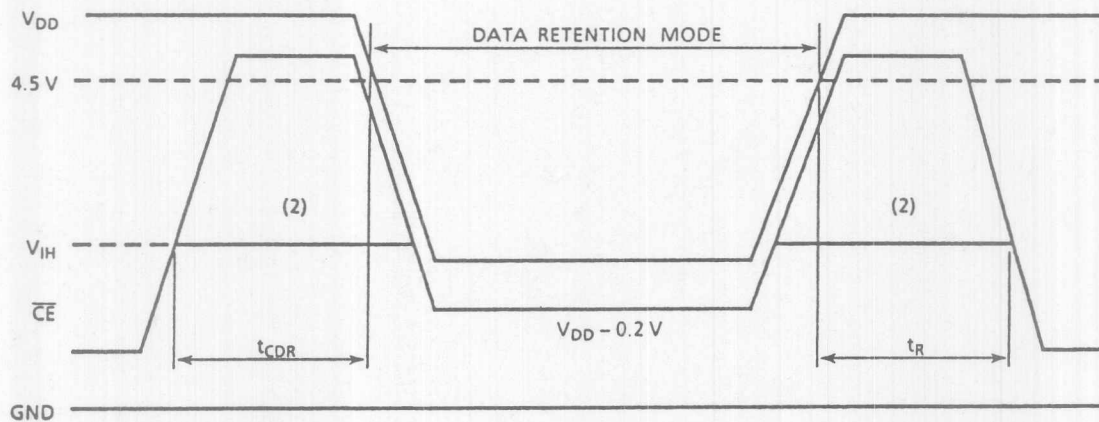
Notes:

1. R/W is high for read cycles.
2. If the \overline{CE} low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the \overline{CE} high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.

Data Retention Characteristics ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DDS2}	Standby Current	$V_{DH} = 3.0\text{V}$	—	50	μA
		$V_{DH} = 5.5\text{V}$	—	100	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	ns
t_R	Recovery Time	$t_{RC(1)}$	—	—	

Note (1): Read Cycle Time

 $\overline{\text{CE}}$ Controlled Data Retention ModeNote (2): If the V_{IH} of $\overline{\text{CE}}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

Notes

TC55257CPL/CFL/CSPL/CFTL/CTRL-70L/85L/10L

PRELIMINARY

SILICON GATE CMOS

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257CPL is a 262,144 bit CMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns.

When \overline{CE} is a logical high, the device is placed in a low power standby mode in which the standby current is 2 μ A at room temperature. The TC55257CPL has two control inputs. Chip enable (\overline{CE}) allows for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. The TC55257CPL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required.

The TC55257CPL is offered in a standard dual-in-line 28-pin plastic package (0.6/0.3 inch width), a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 2 μ A (max.) at $T_a = 25^\circ\text{C}$
- Single 5V power supply
- Access time (max.)

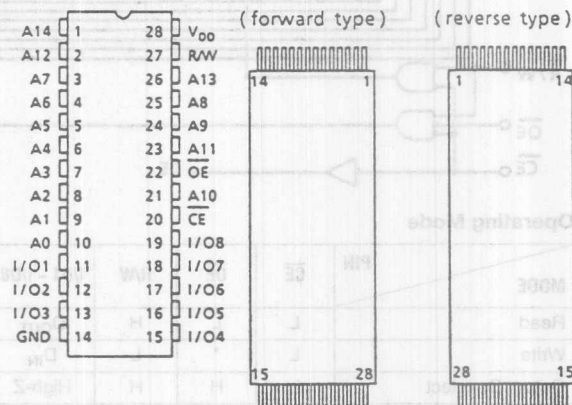
	TC55257CPL/CFL/CSPL/CFTL/CTRL		
	-70L	-85L	-10L
Access Time	70ns	85ns	100ns
\overline{CE} Access Time	70ns	85ns	100ns
\overline{OE} Access Time	35ns	45ns	50ns

- Power down feature: \overline{CE}
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package
 - TC55257CPL : DIP28-P-600
 - TC55257CFL : SOP28-P-450
 - TC55257CSPL : DIP28-P-300B
 - TC55257CFTL : TSOP28-P
 - TC55257CTRL : TSOP28-P-A

Pin Connection (Top View)

○ 28 PIN DIP & SOP

○ 28 PIN TSOP



Pin Names

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground

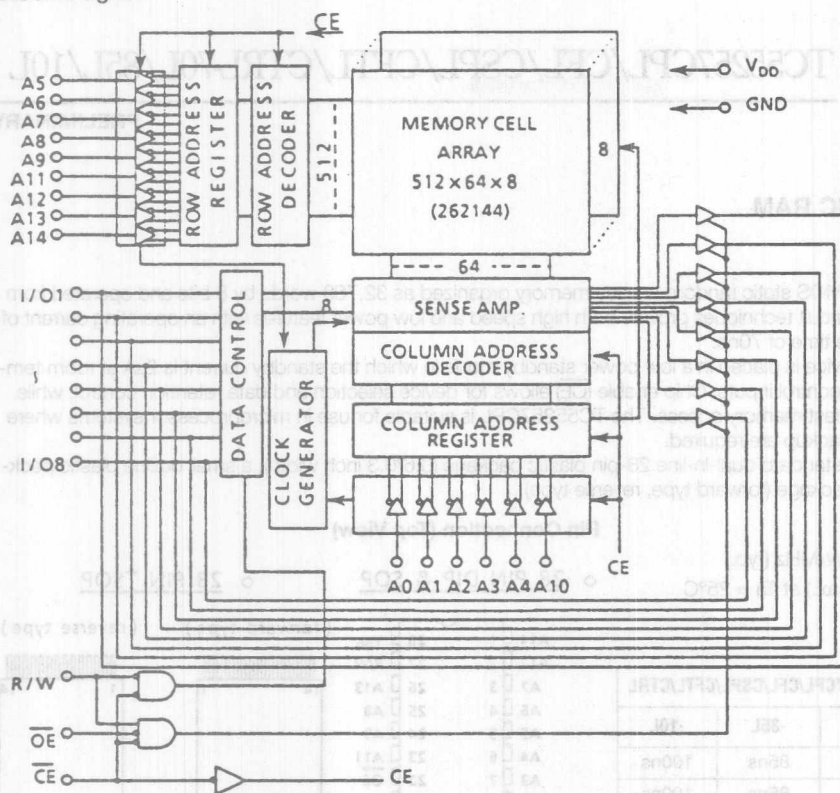
PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	\overline{OE}	A ₁₁	A ₉	A ₈	A ₁₃	R/W	V _{DD}	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀

PRELIMINARY

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

A-59

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	R/W	I/O1 ~ I/O8	POWER
Read		L	L	H	D _{OUT}	I _{DDO}
Write		L	*	L	D _{IN}	I _{DDO}
Output Deselect		L	H	H	High-Z	I _{DDO}
Standby		H	*	*	High-Z	I _{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5* ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.8/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V with a pulse width of 50ns

** Package dependent: 0.6 inch 1.0W, 0.3 inch 0.8W, 0.45 inch 0.6W

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	—	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

* -3.0V with a pulse width of 50ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	-1.0	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	4.0	—	—	mA
I_{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ $R/W = V_{IH}$ Other Input = V_{IH}/V_{IL} $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 1\mu\text{s}$	—	10	—
			$t_{\text{cycle}} = \text{Min. cycle}$	—	—	70
I_{DDO2}	Operating Current	$\overline{CE} = 0.2\text{V}$ $R/W = V_{DD} - 0.2\text{V}$ Other Input = $V_{DD} - 0.2\text{V}/0.2\text{V}$ $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 1\mu\text{s}$	—	5	—
			$t_{\text{cycle}} = \text{Min. cycle}$	—	—	60
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	3	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2\text{V}$ $V_{DD} = 2.0\text{V} \sim 5.5\text{V}$	$T_a = 0 \sim 70^\circ\text{C}$	—	—	20
			$T_a = 25^\circ\text{C}$	—	—	2

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55257CPL/CFL/CSPL/CFTL/CTRL						UNIT
		-70L		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	70	—	85	—	100	—	ns
t _{ACC}	Address Access Time	—	70	—	85	—	100	
t _{CO}	$\overline{\text{CE}}$ Access Time	—	70	—	85	—	100	
t _{OE}	Output Enable to Output in Valid	—	35	—	45	—	50	
t _{COE}	Chip Enable ($\overline{\text{CE}}$) to Output in Low-Z	10	—	10	—	10	—	
t _{OEE}	Output Enable to Output in Low-Z	5	—	5	—	5	—	
t _{OD}	Chip Enable ($\overline{\text{CE}}$) to Output in High-Z	—	25	—	30	—	50	
t _{ODO}	Output Enable to Output in High-Z	—	25	—	30	—	40	
t _{OH}	Output Data Hold Time	10	—	10	—	10	—	

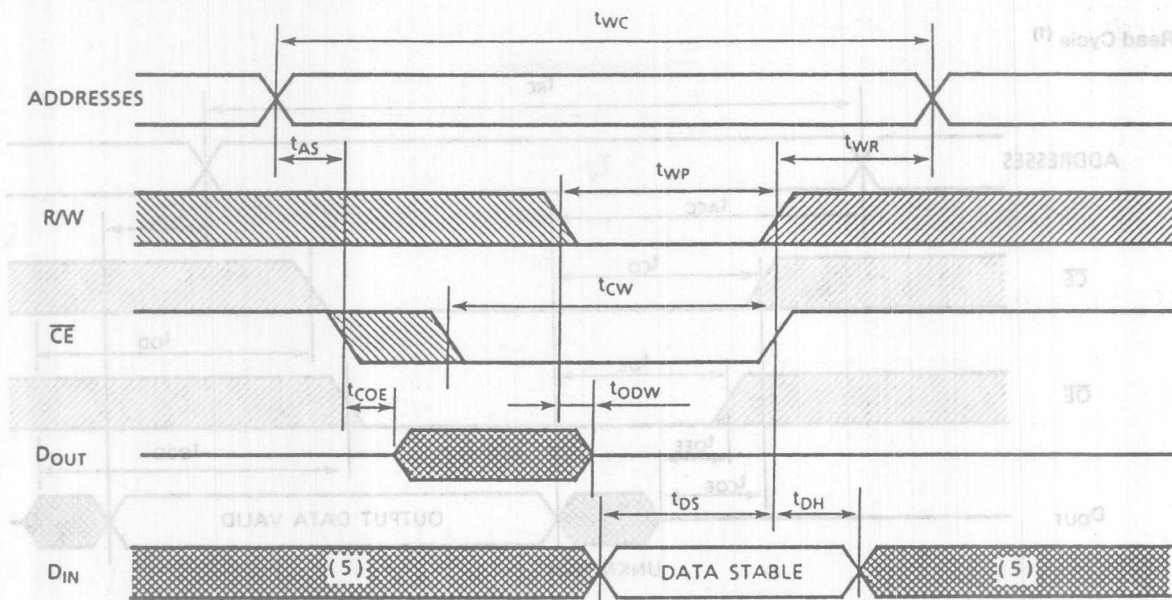
Write Cycle

SYMBOL	PARAMETER	TC55257CPL/CFL/CSPL/CFTL/CTRL						UNIT
		-70L		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	70	—	85	—	100	—	ns
t _{WP}	Write Pulse Width	50	—	60	—	70	—	
t _{CW}	Chip Selection to End of Write	60	—	65	—	90	—	
t _{AS}	Address Setup Time	0	—	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	
t _{ODW}	R/W to Output in High-Z	—	25	—	30	—	50	
t _{OEW}	R/W to Output in Low-Z	5	—	5	—	5	—	
t _{DS}	Data Setup Time	30	—	40	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	

AC Test Conditions

Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and C _L = 100pF

Write Cycle 2 ⁽⁴⁾ ($\overline{\text{CE}}$ Controlled Write)



Notes:

1. R/W is high for read cycles.
2. If the $\overline{\text{CE}}$ low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the $\overline{\text{CE}}$ high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If $\overline{\text{OE}}$ is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.

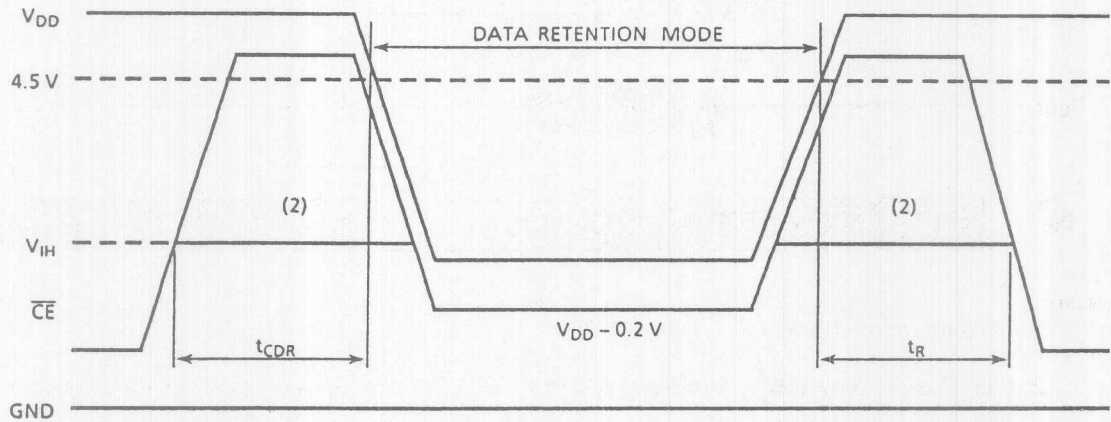
Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V _{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I _{DDS2}	Standby Current	V _{DH} = 3.0V	—	—	10*	μA
		V _{DH} = 5.5V	—	—	20	
t _{CDR}	Chip Deselect to Data Retention Mode		0	—	—	ns
t _R	Recovery Time		t _{RC(1)}	—	—	

Note (1): Read Cycle Time

*2μA (max.) Ta = 0 ~ 40°C

$\overline{\text{CE}}$ Controlled Data Retention Mode



Note (2): If the V_{IH} of $\overline{\text{CE}}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

TC55257CPI/CFI/CSPI/CFTI/CTRI-85/10

SILICON GATE CMOS

PRELIMINARY

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257CPI is a 262,144 bit CMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 85ns.

When \overline{CE} is a logical high, the device is placed in a low power standby mode in which the standby current is 2 μ A at room temperature. The TC55257CPI has two control inputs. Chip enable (\overline{CE}) allows for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. The TC55257CPI is suitable for use in microprocessor systems where high speed, low power, and battery backup are required. The TC55257CPI is guaranteed over an operating temperature range of -40 ~ 85°C so the TC55257CPI is suitable for use in wide operating temperature systems.

The TC55257CPI is offered in a standard dual-in-line 28-pin plastic package (0.6/0.3 inch width), a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 200 μ A (max.)
- Single 5V power supply
- Access time (max.)

	TC55257CPI/CFI/CSPI/CFTI/CTRI	
	-85	-10
Access Time	85ns	100ns
\overline{CE} Access Time	85ns	100ns
\overline{OE} Access Time	45ns	50ns

- Power down feature: \overline{CE}
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Wide operating temperature: -40 ~ 85°C
- Package

TC55257CPI	: DIP28-P-600
TC55257CFI	: SOP28-P-450
TC55257CSPI	: DIP28-P-300B
TC55257CFTI	: TSOP28-P
TC55257CTRI	: TSOP28-P-A

Pin Names

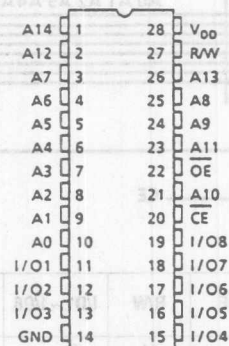
A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	\overline{OE}	A ₁₁	A ₉	A ₈	A ₁₃	R/W	V _{DD}	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀

Pin Connection (Top View)

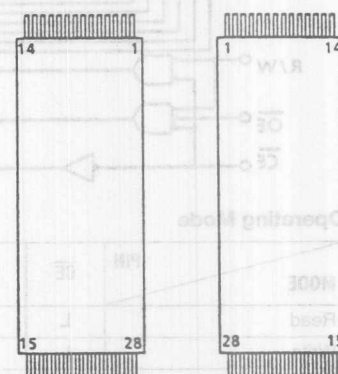
○ 28 PIN DIP & SOP

○ 28 PIN TSOP

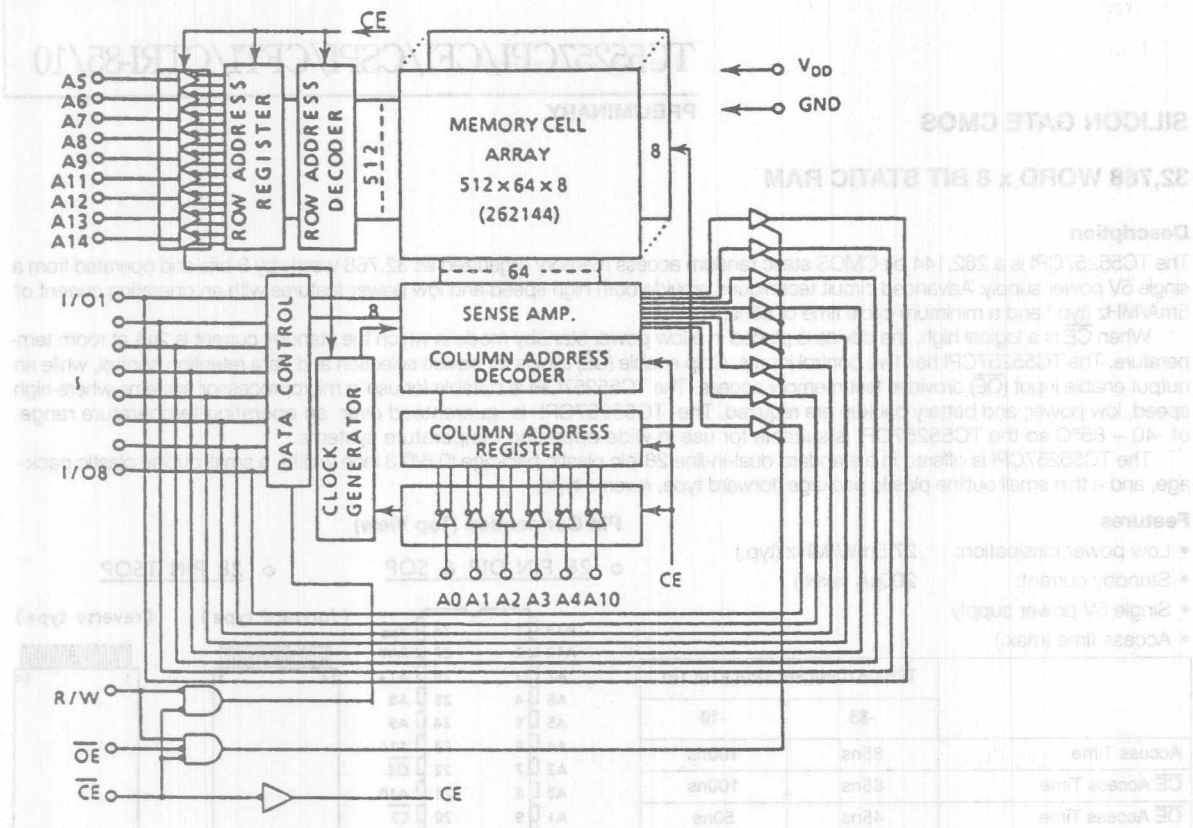


(forward type)

(reverse type)



Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	R/W	I/O1 ~ I/O8	POWER
Read		L	L	H	D _{OUT}	I _{DD}
Write		L	*	L	D _{IN}	I _{DD}
Output Deselect		L	H	H	High-Z	I _{DD}
Standby		H	*	*	High-Z	I _{DS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{IO}	Input and Output Voltage	-0.5* ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.8/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	-40 ~ 85	°C

* -3.0V with a pulse width of 50ns

** Package dependent: 0.6 inch 1.0W, 0.3 inch 0.8W, 0.45 inch 0.6W

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	—	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

* -3.0V with a pulse width of 50ns

DC Characteristics ($T_a = -40 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}		—	—	±1.0	μA
I _{LO}	Output Leakage Current	CE = V _{IH} or R/W = V _{IL} or OE = V _{IH} V _{OUT} = 0 ~ V _{DD}		—	—	±1.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V		-1.0	—	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V		4.0	—	—	mA
I _{DDO1}	Operating Current	CE = V _{IL} R/W = V _{IH} Other Input = V _{IH} /V _{IL} I _{OUT} = 0mA	t _{cycle} = 1μs	—	10	—	mA
			t _{cycle} = Min. cycle	—	—	70	
I _{DDO2}		CE = 0.2V R/W = V _{DD} - 0.2V Other Input = V _{DD} - 0.2V/0.2V I _{OUT} = 0mA	t _{cycle} = 1μs	—	5	—	mA
			t _{cycle} = Min. cycle	—	—	60	
I _{DDS1}	Standby Current	CE = V _{IH}		—	—	3	mA
I _{DDS2}		CE = V _{DD} - 0.2V	Ta = -40 ~ 85°C	—	—	200	μA
		V _{DD} = 2.0V ~ 5.5V	Ta = 25°C	—	2	—	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

* This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55257CPI/CFI/CSPI/CFTI/CTRI				UNIT
		-85		-10		
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	85	—	100	—	ns
t _{ACC}	Address Access Time	—	85	—	100	
t _{CO}	$\overline{\text{CE}}$ Access Time	—	85	—	100	
t _{OE}	Output Enable to Output in Valid	—	45	—	50	
t _{COE}	Chip Enable ($\overline{\text{CE}}$) to Output in Low-Z	5	—	5	—	
t _{OEE}	Output Enable to Output in Low-Z	0	—	0	—	
t _{OD}	Chip Enable ($\overline{\text{CE}}$) to Output in High-Z	—	30	—	50	
t _{ODO}	Output Enable to Output in High-Z	—	30	—	40	
t _{OH}	Output Data Hold Time	10	—	10	—	

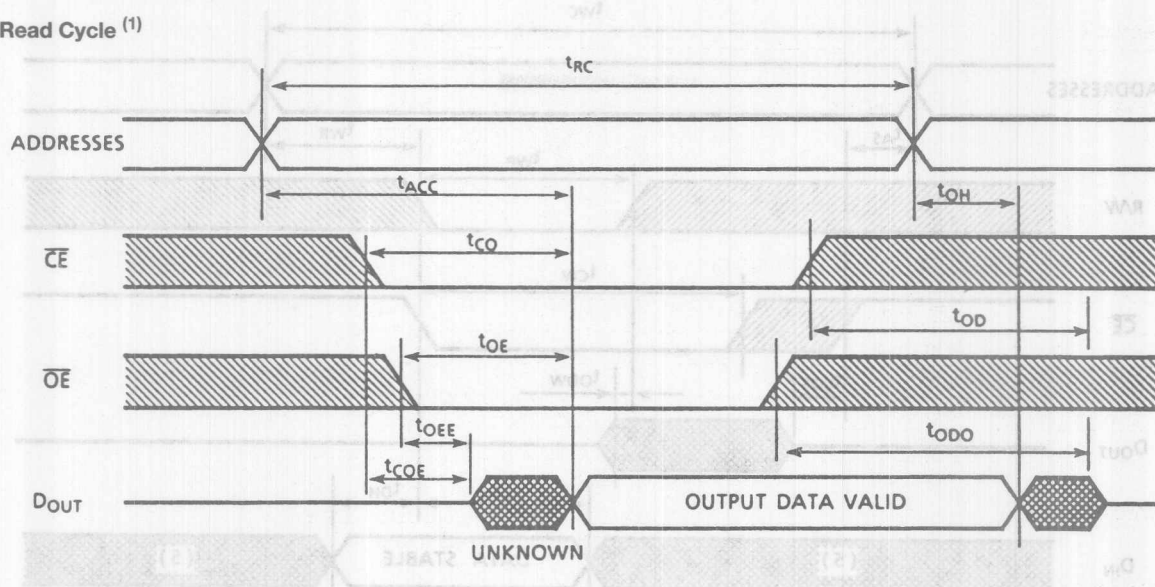
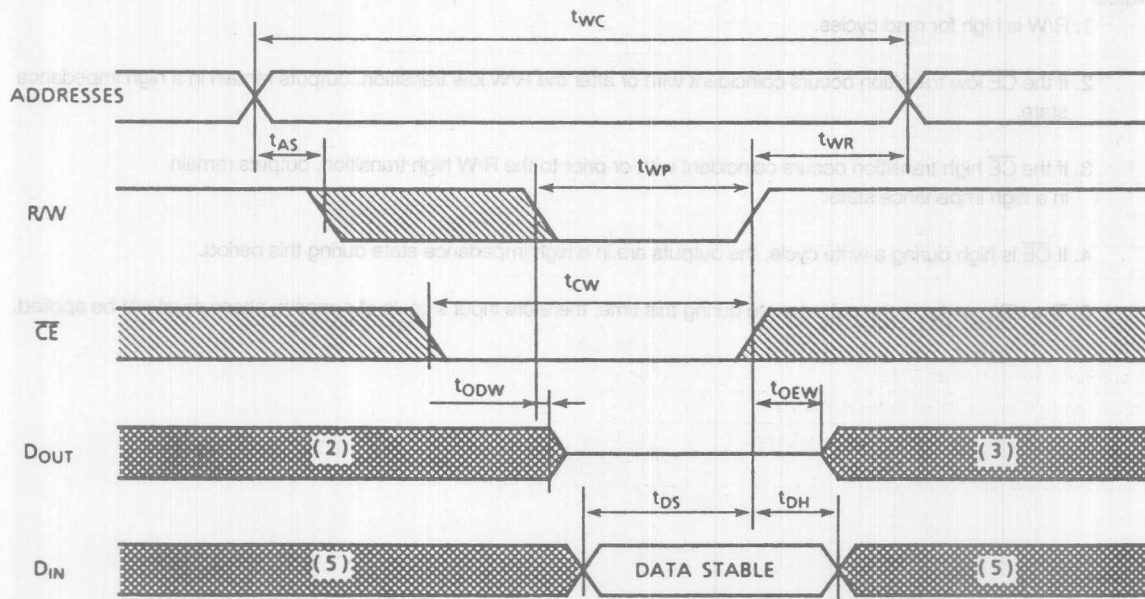
Write Cycle

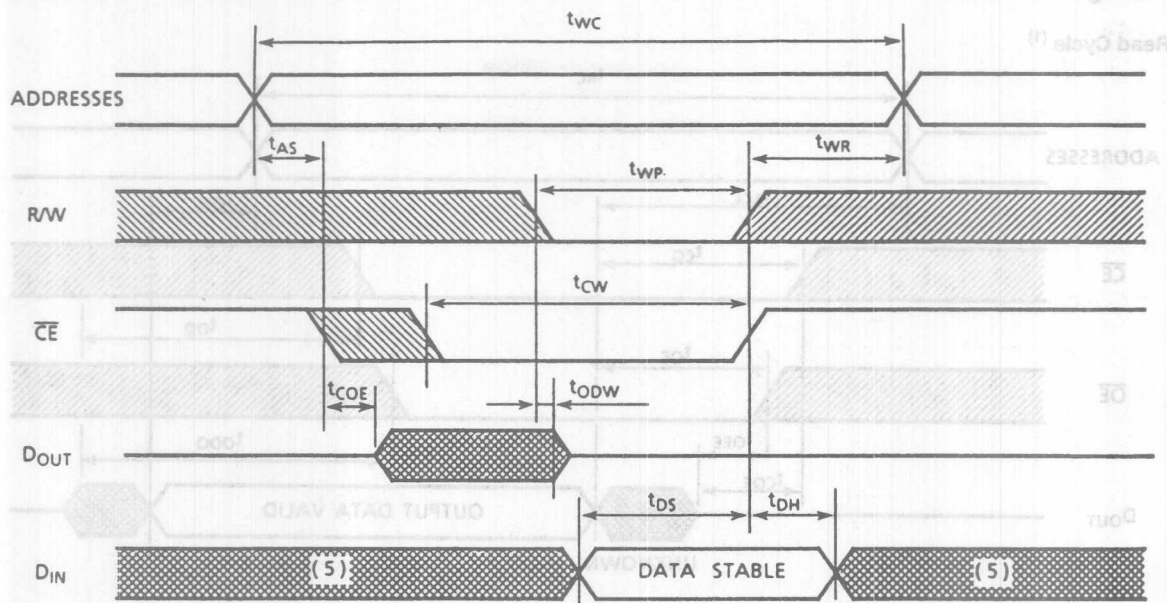
SYMBOL	PARAMETER	TC55257CPI/CFI/CSPI/CFTI/CTRI				UNIT
		-85		-10		
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	85	—	100	—	ns
t _{WP}	Write Pulse Width	60	—	70	—	
t _{CW}	Chip Selection to End of Write	65	—	90	—	
t _{AS}	Address Setup Time	0	—	0	—	
t _{WR}	Write Recovery Time	5	—	5	—	
t _{ODW}	R/W to Output in High-Z	—	30	—	50	
t _{OEW}	R/W to Output in Low-Z	0	—	0	—	
t _{DS}	Data Setup Time	40	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	

AC Test Conditions

Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and C _L = 100pF

Timing Waveforms

Read Cycle ⁽¹⁾Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)

Write Cycle 2 ⁽⁴⁾ ($\overline{\text{CE}}$ Controlled Write)

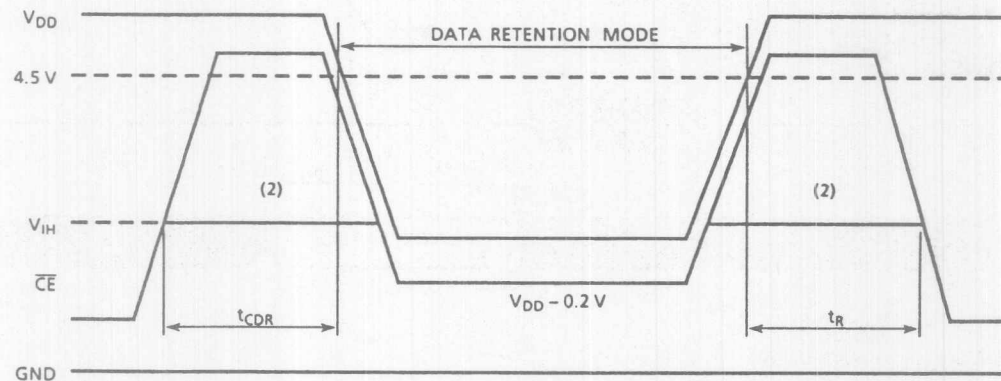
Notes:

1. R/W is high for read cycles.
2. If the $\overline{\text{CE}}$ low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the $\overline{\text{CE}}$ high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If $\overline{\text{OE}}$ is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.

Data Retention Characteristics (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DDS2}	Standby Current	$V_{DH} = 3.0V$	—	100	μA
		$V_{DH} = 5.5V$	—	200	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	ns
t_R	Recovery Time	$t_{RC(1)}$	—	—	

Note (1): Read Cycle Time

 \overline{CE} Controlled Data Retention ModeNote (2): If the V_{IH} of \overline{CE} is 2.4V in operation, I_{DDP1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.6V.

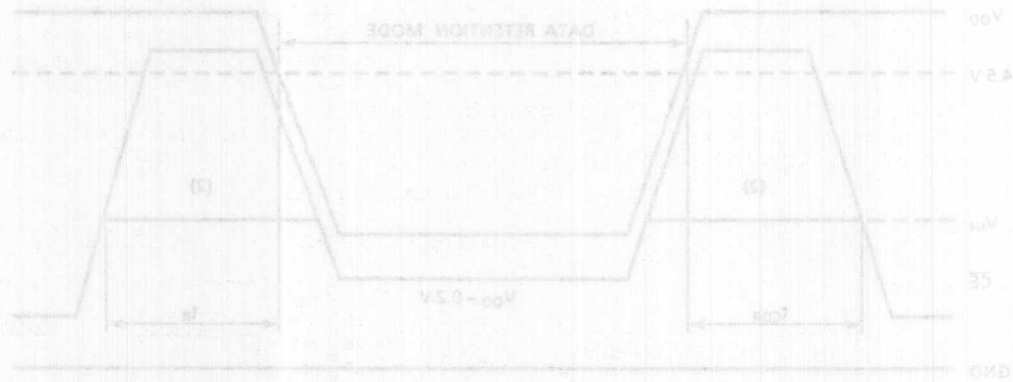
Notes

Data Retention Characteristics (Ta = -40 ~ 85°C)

PARAMETER	UNIT	MIN.	TYP.	MAX.
V _{DD} Data Retention Supply Voltage	V	2.5	—	2.5
I _{DD} Standby Current	μA	—	—	100
I _{DD} C ₁ Disabled in Data Retention Mode	μA	—	—	500
t _R Recovery Time	ns	—	—	—

Note (1): Read Cycle Time

CE Controlled Data Retention Mode



Note (2): If the V_{CE} is 2.4V or less, the current flows during the period that the V_{DD} voltage is being driven from 4.5V to 2.5V.

TC55257CPI/CFI/CSPI/CFTI/CTRI-85L/10L

SILICON GATE CMOS

PRELIMINARY

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257CPI is a 262,144 bit CMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 85ns.

When \overline{CE} is a logical high, the device is placed in a low power standby mode in which the standby current is $2\mu A$ at room temperature. The TC55257CPI has two control inputs. Chip enable (\overline{CE}) allows for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. The TC55257CPI is suitable for use in microprocessor systems where high speed, low power, and battery backup are required. The TC55257CPI is guaranteed over an operating temperature range of $-40 \sim 85^\circ C$ so the TC55257CPI is suitable for use in wide operating temperature systems.

The TC55257CPI is offered in a standard dual-in-line 28-pin plastic package (0.6/0.3 inch width), a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: $2\mu A$ (max.) at $T_a = 25^\circ C$
- Single 5V power supply
- Access time (max.)

	TC55257CPI/CFI/CSPI/CFTI/CTRI	
	-85L	-10L
Access Time	85ns	100ns
\overline{CE} Access Time	85ns	100ns
\overline{OE} Access Time	45ns	50ns

- Power down feature: \overline{CE}
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Wide operating temperature: $-40 \sim 85^\circ C$
- Package
 - TC55257CPI : DIP28-P-600
 - TC55257CFI : SOP28-P-450
 - TC55257CSPI : DIP28-P-300B
 - TC55257CFTI : TSOP28-P
 - TC55257CTRI : TSOP28-P-A

Pin Names

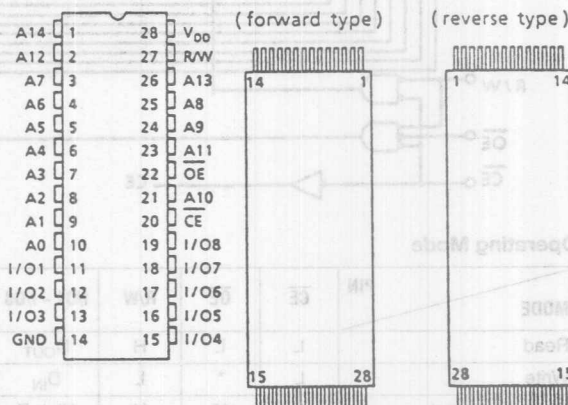
A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	\overline{OE}	A ₁₁	A ₉	A ₈	A ₁₃	R/W	V_{DD}	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀

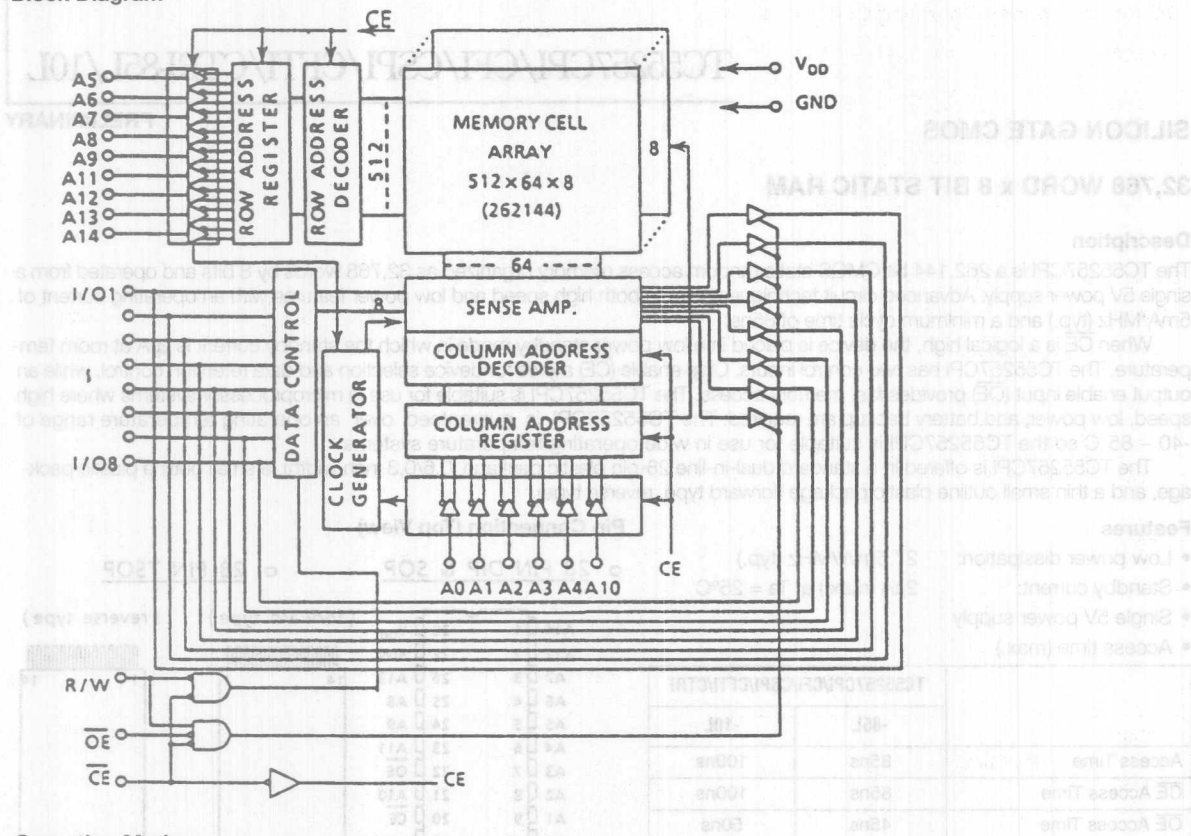
Pin Connection (Top View)

28 PIN DIP & SOP

28 PIN TSOP



Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	R/W	I/O1 ~ I/O8	POWER
Read		L	L	H	D _{OUT}	I _{DDO}
Write		L	*	L	D _{IN}	I _{DDO}
Output Deselect		L	H	H	High-Z	I _{DDO}
Standby		H	*	*	High-Z	I _{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{IO}	Input and Output Voltage	-0.5* ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.8/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	-40 ~ 85	°C

* -3.0V with a pulse width of 50ns

** Package dependent; 0.6 inch 1.0W, 0.3 inch 0.8W, 0.45 inch 0.6W

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	—	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

* -3.0V with a pulse width of 50ns

DC Characteristics ($T_a = -40 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-1.0	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	4.0	—	—	mA
I_{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ $R/W = V_{IH}$ Other Input = V_{IH}/V_{IL} $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 1\mu\text{s}$	—	10	—
			$t_{\text{cycle}} = \text{Min. cycle}$	—	—	70
I_{DDO2}		$\overline{CE} = 0.2V$ $R/W = V_{DD} - 0.2V$ Other Input = $V_{DD} - 0.2V/0.2V$ $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 1\mu\text{s}$	—	5	—
			$t_{\text{cycle}} = \text{Min. cycle}$	—	—	60
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	3	mA
		$\overline{CE} = V_{DD} - 0.2V$	$T_a = -40 \sim 85^\circ\text{C}$	—	30	μA
I_{DDS2}		$V_{DD} = 2.0V \sim 5.5V$	$T_a = 25^\circ\text{C}$	—	2	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

Read Cycle

Read Cycle						
SYMBOL	PARAMETER	TC55257CPI/CFI/CSPI/CFTI/CTRI				UNIT
		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	85	—	100	—	ns
t _{ACC}	Address Access Time	—	85	—	100	
t _{CO}	CE Access Time	—	85	—	100	
t _{OE}	Output Enable to Output in Valid	—	45	—	50	
t _{COE}	Chip Enable (CE) to Output in Low-Z	5	—	5	—	
t _{OEE}	Output Enable to Output in Low-Z	0	—	0	—	
t _{OD}	Chip Enable (CE) to Output in High-Z	—	30	—	50	
t _{ODO}	Output Enable to Output in High-Z	—	30	—	40	
t _{OH}	Output Data Hold Time	10	—	10	—	

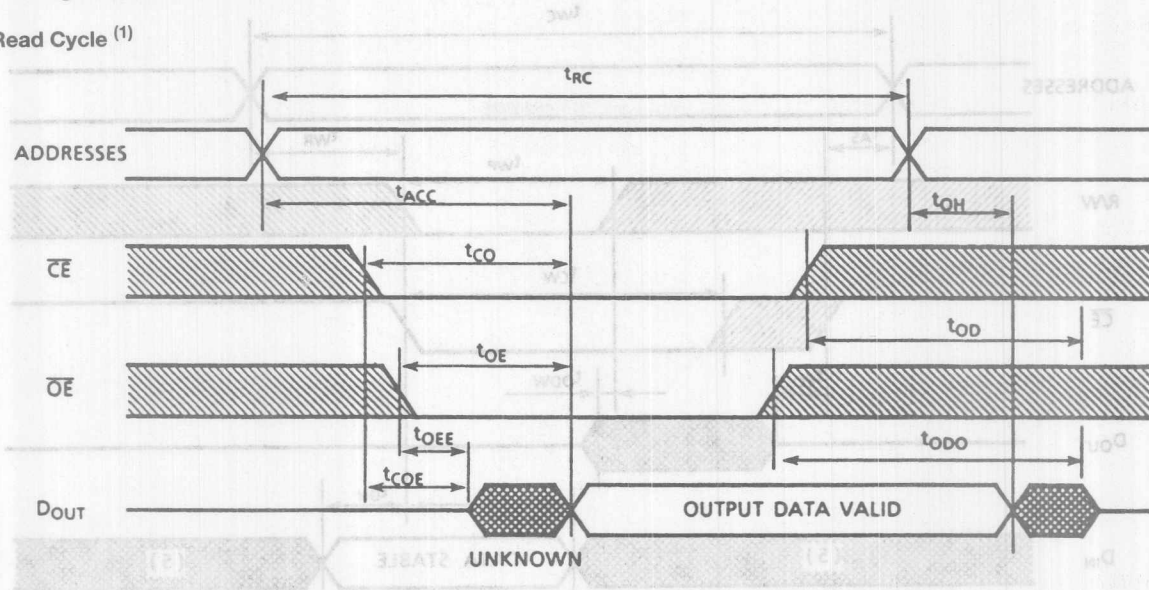
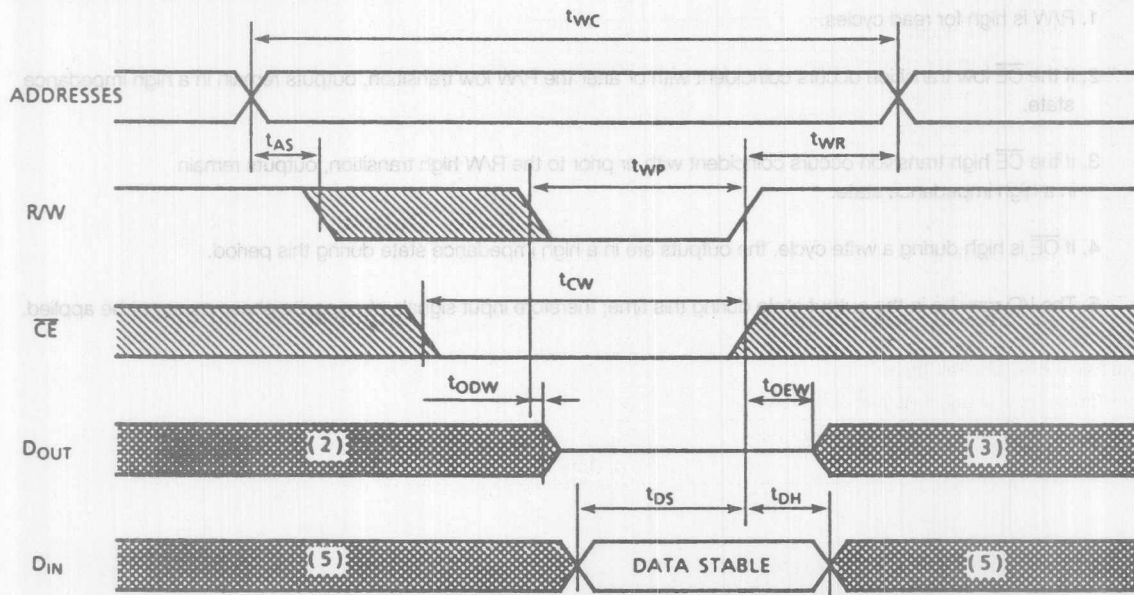
Write Cycle

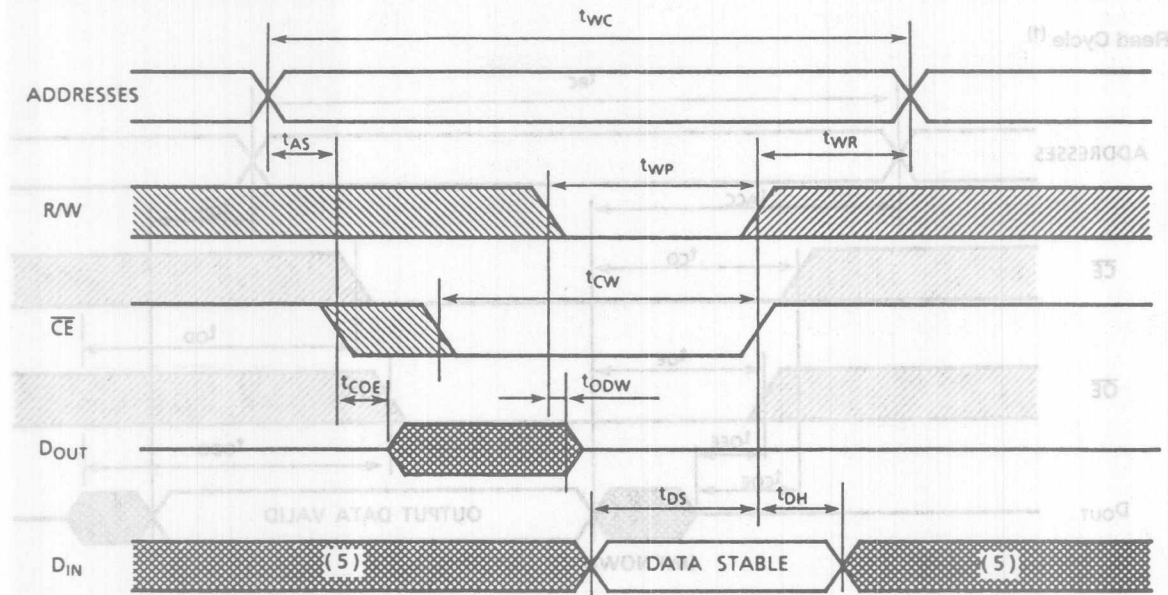
SYMBOL	PARAMETER	TC55257CPI/CFI/CSPI/CFTI/CTRI				UNIT
		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	85	—	100	—	ns
t _{WP}	Write Pulse Width	60	—	70	—	
t _{CW}	Chip Selection to End of Write	65	—	90	—	
t _{AS}	Address Setup Time	0	—	0	—	
t _{WR}	Write Recovery Time	5	—	5	—	
t _{ODW}	R/W to Output in High-Z	—	30	—	50	
t _{OEW}	R/W to Output in Low-Z	0	—	0	—	
t _{DS}	Data Setup Time	40	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	

AC Test Conditions

Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and C _L = 100pF

Timing Waveforms

Read Cycle ⁽¹⁾Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)

Write Cycle 2 ⁽⁴⁾ ($\overline{\text{CE}}$ Controlled Write)

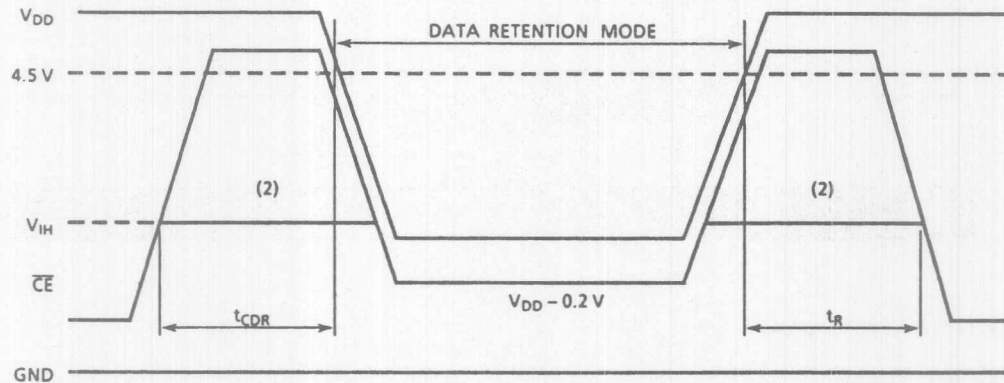
Notes:

1. R/W is high for read cycles.
2. If the $\overline{\text{CE}}$ low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the $\overline{\text{CE}}$ high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If $\overline{\text{OE}}$ is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.

Data Retention Characteristics (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DDS2}	Standby Current	$V_{DH} = 3.0V$	—	15*	μA
		$V_{DH} = 5.5V$	—	30	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	ns
t_R	Recovery Time	$t_{RC(1)}$	—	—	

Note (1): Read Cycle Time

*2 μA (max.) Ta = 0 ~ 40°C \overline{CE} Controlled Data Retention ModeNote (2): If the V_{IH} of \overline{CE} is 2.4V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.6V.

TC551001APL/AFL/AFTL/ATRL-70/85/10(LT)

SILICON GATE CMOS

131,072 WORD x 8 BIT STATIC RAM

Description

The TC551001APL is a 1,048,576 bit CMOS static random access memory organized as 131,072 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns. When $\overline{CE1}$ is a logical high, or $\overline{CE2}$ is low, the device is placed in a low power standby mode in which the standby current is 2 μ A typically. The TC551001APL has three control inputs. Chip enable inputs ($\overline{CE1}$, $\overline{CE2}$) allow for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. The TC551001APL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required. The TC551001APL-(LT) has an operating temperature range of -20 ~ 70°C so it is suitable for use in low temperature applications.

The TC551001APL is offered in a standard dual-in-line 32-pin plastic package, a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 100 μ A (max.)
- Single 5V power supply
- Access time (max.)

	TC551001APL/AFL/AFTL/ATRL		
	-70(LT)	-85(LT)	-10(LT)
Access Time	70ns	85ns	100ns
$\overline{CE1}$ Access Time	70ns	85ns	100ns
$\overline{CE2}$ Access Time	70ns	85ns	100ns
\overline{OE} Access Time	35ns	45ns	50ns

- Power down feature: $\overline{CE1}$, $\overline{CE2}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Wide operating temperature: -20 ~ 70°C
- Inputs and outputs TTL compatible
- Package
 - TC551001APL : DIP32-P-600
 - TC551001AFL : SOP32-P-525
 - TC551001AFTL : TSOP32-P-0820
 - TC551001ATRL : TSOP32-P-0820A

Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
$\overline{CE1}$, $\overline{CE2}$	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground
NC	No Connection

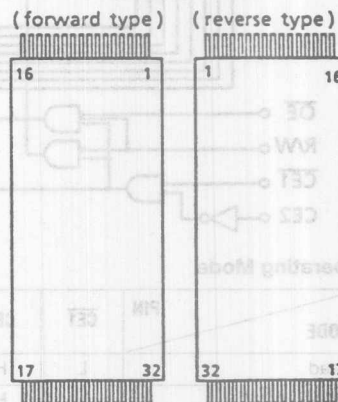
PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CE2	A ₁₅	V _{DD}	NC	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A ₁₀	\overline{OE}

Pin Connection (Top View)

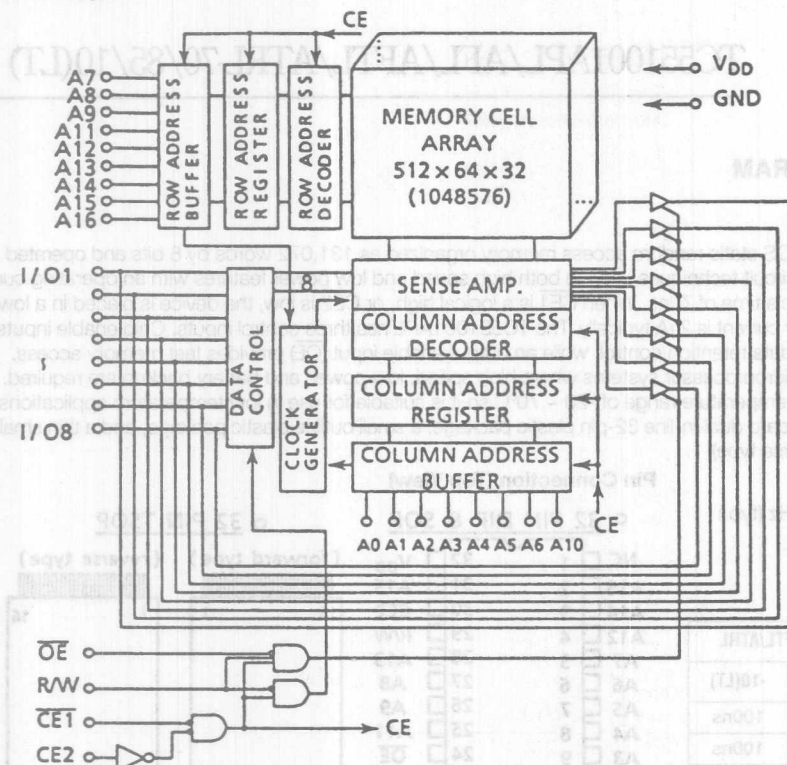
32 PIN DIP & SOP



32 PIN TSOP



Block Diagram



Operating Mode

MODE	PIN	CE1	CE2	OE	R/W	I/O1 ~ I/O8	POWER
Read		L	H	L	H	D _{OUT}	I _{DDO}
Write		L	H	*	L	D _{IN}	I _{DDO}
Output Deselect		L	H	H	H	High-Z	I _{DDO}
Standby		H	*	*	*	High-Z	I _{DDO}
		*	L	*	*	High-Z	I _{DDO}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	-20 ~ 70	°C

* -3.0V with a pulse width of 50ns

** SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3	—	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

DC Characteristics ($T_a = -20 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{LO}	Output Leakage Current	CE1 = V _{IH} or CE2 = V _{IL} or R/W = V _{IL} or OE = V _{IH} , V _{OUT} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V			-1.0	—	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V			4.0	—	—	mA
I _{DDO1}	Operating Current	CE1 = V _{IL} and CE2 = V _{IH} and R/W = V _{IH} , I _{OUT} = 0mA Other Inputs = V _{IH} /V _{IL}	t _{cycle}	Min.	—	—	70	mA
				1μs	—	—	20	
I _{DDO2}		CE1 = 0.2V and CE2 = V _{DD} - 0.2V R/W = V _{DD} - 0.2V I _{OUT} = 0mA Other Inputs = V _{DD} - 0.2V/0.2V	t _{cycle}	Min.	—	—	60	
				1μs	—	—	10	
I _{DDS1}	Standby Current	CE1 = V _{IH} or CE2 = V _{IL}			—	—	3	mA
I _{DDS2} ⁽¹⁾		CE1 = V _{DD} - 0.2V or CE2 = 0.2V V _{DD} = 2.0V ~ 5.5V		Ta = -20 ~ 70°C	—	—	100	μA
				Ta = 25°C	—	2	—	

Note (1): If $\overline{CE1} \geq V_{DD} - 0.2V$, the specified limits are guaranteed under the condition $CE2 \geq V_{DD} - 0.2V$ or $CE2 \leq 0.2V$.

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -20 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551001APL/AFL/AFTL/ATRL						UNIT
		-70(LT)		-85(LT)		-10(LT)		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	70	—	85	—	100	—	ns
t _{ACC}	Address Access Time	—	70	—	85	—	100	
t _{CO1}	CE1 Access Time	—	70	—	85	—	100	
t _{CO2}	CE2 Access Time	—	70	—	85	—	100	
t _{OE}	Output Enable to Output in Valid	—	35	—	45	—	50	
t _{COE}	Chip Enable (CE1, CE2) to Output in Low-Z	5	—	5	—	5	—	
t _{OEE}	Output Enable to Output in Low-Z	0	—	0	—	0	—	
t _{OD}	Chip Enable (CE1, CE2) to Output in High-Z	—	25	—	30	—	35	
t _{ODO}	Output Enable to Output in High-Z	—	25	—	30	—	35	
t _{OH}	Output Data Hold Time	10	—	10	—	10	—	

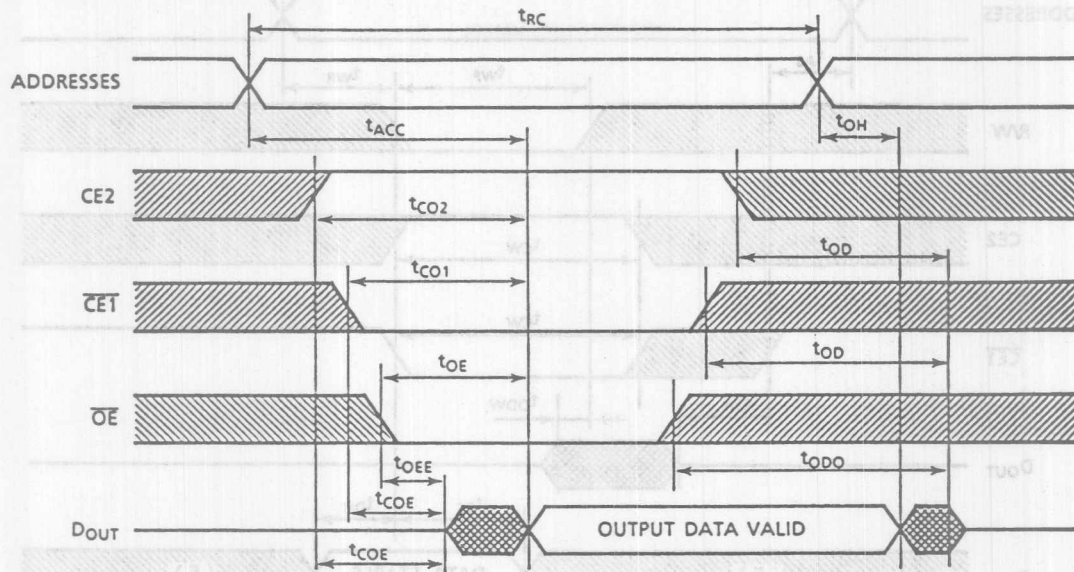
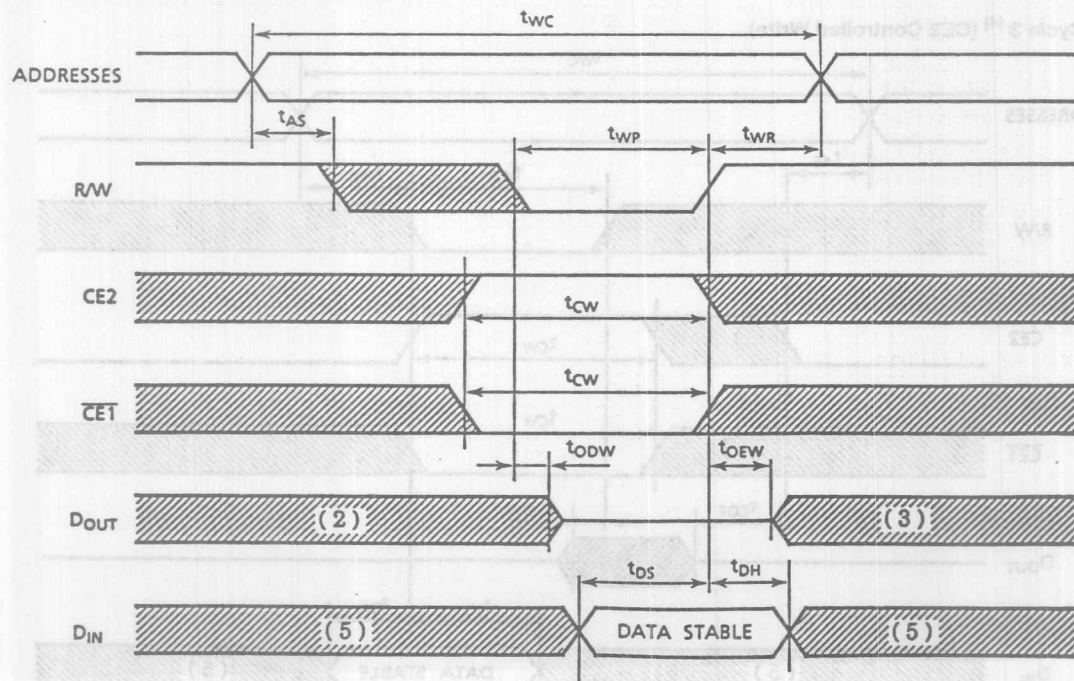
Write Cycle

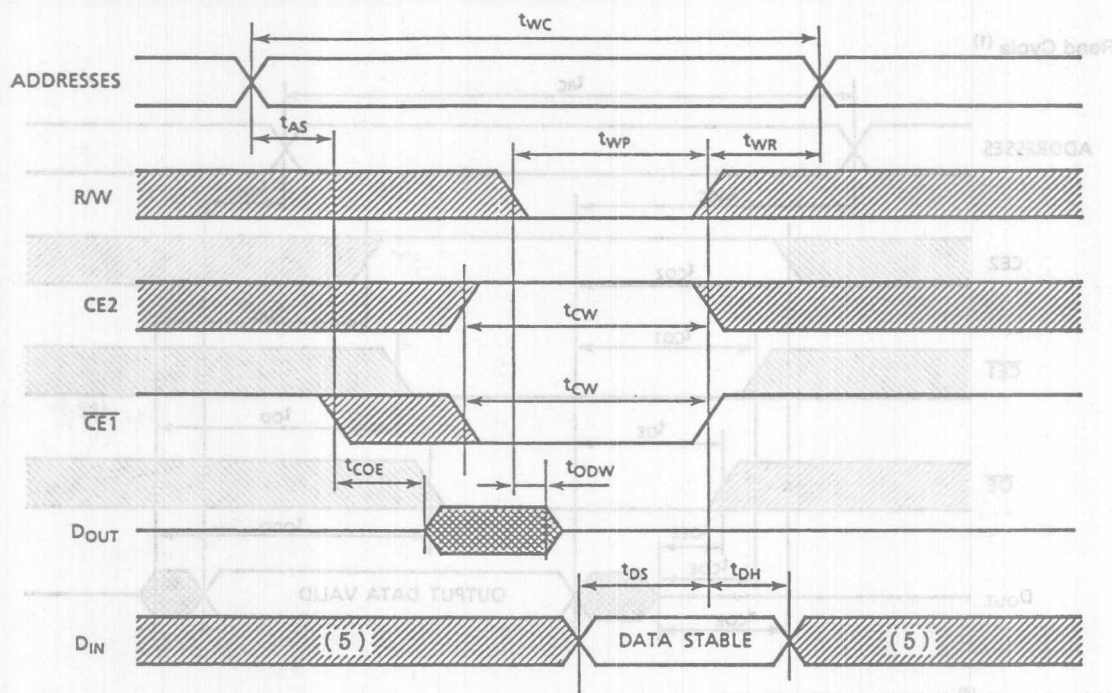
SYMBOL	PARAMETER	TC551001APL/AFL/AFTL/ATRL						UNIT
		-70(LT)		-85(LT)		-10(LT)		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	70	—	85	—	100	—	ns
t _{WP}	Write Pulse Width	50	—	60	—	60	—	
t _{CW}	Chip Selection to End of Write	60	—	75	—	80	—	
t _{AS}	Address Setup Time	0	—	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	
t _{ODW}	R/W to Output in High-Z	—	25	—	30	—	35	
t _{OEW}	R/W to Output in Low-Z	0	—	0	—	0	—	
t _{DS}	Data Setup Time	30	—	35	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	

AC Test Conditions

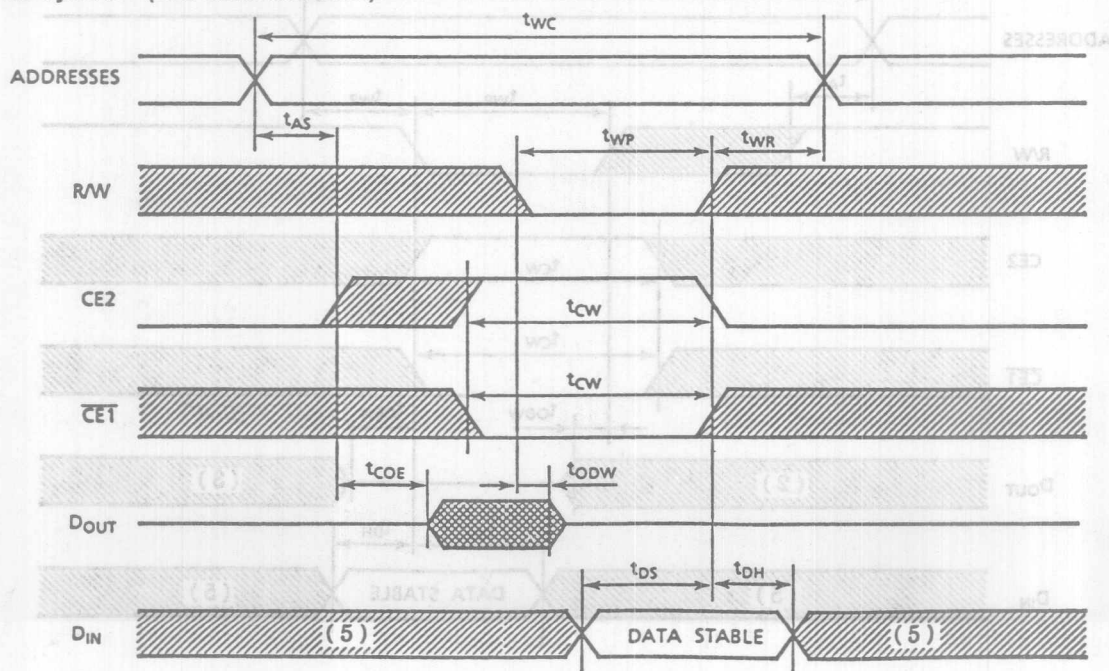
Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and C _L = 100pF

Timing Waveforms

Read Cycle ⁽¹⁾Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)



Write Cycle 3⁽⁴⁾ (CE2 Controlled Write)



Notes:

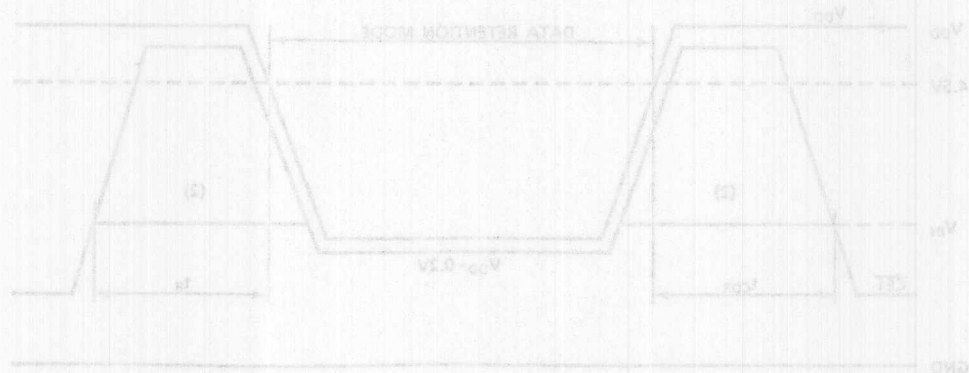
1. R/W is high for read cycles.

2. If the $\overline{\text{CE1}}$ low transition or CE2 high transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.

3. If the $\overline{\text{CE1}}$ high transition or CE2 low transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.

4. If $\overline{\text{OE}}$ is high during a write cycle, the outputs are in a high impedance state during this period.

5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.



Notes:

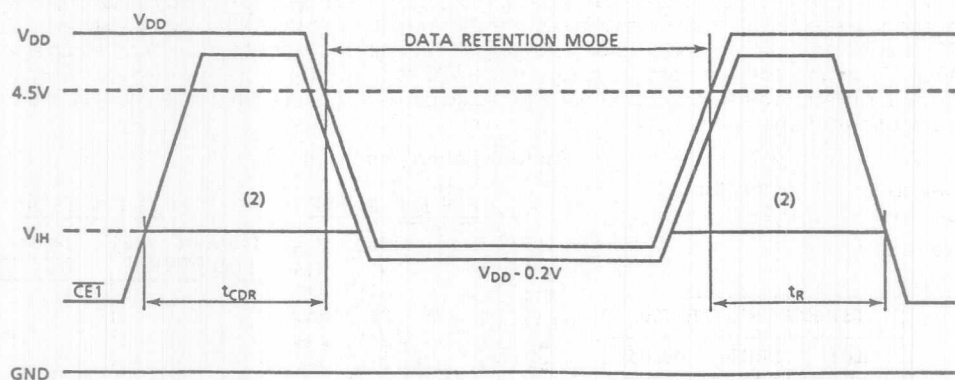
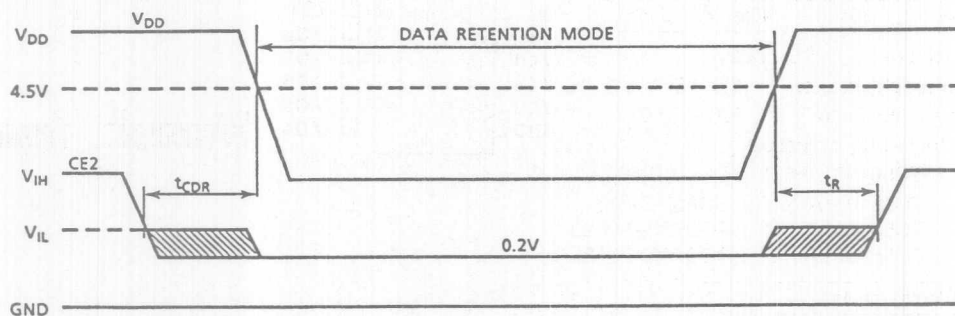
1. In the $\overline{\text{CE1}}$ controlled data retention mode, minimum standby current is achieved under the condition $\text{CE2} \leq 0.5\text{V}$ or $\text{CE2} \leq V_{\text{cc}} - 0.5\text{V}$.

2. If the V_{ce1} or V_{ce2} is 2.5V in operation, during the period that the V_{ce1} voltage is going down from 4.5V to 2.5V, power current flows.

3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition $\text{CE2} \leq 0.5\text{V}$.

Data Retention Characteristics (Ta = -20 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DSS2}	Standby Current	$V_{DH} = 3.0V$	—	50	μA
		$V_{DH} = 5.5V$	—	100	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	ns
t_R	Recovery Time	5	—	—	ms

 $\overline{CE1}$ Controlled Data Retention Mode ⁽¹⁾CE2 Controlled Data Retention Mode ⁽³⁾

Notes:

1. In the $\overline{CE1}$ controlled data retention mode, minimum standby current is achieved under the condition $CE2 \leq 0.2V$ or $CE2 \geq V_{DD} - 0.2V$.
2. If the V_{IH} of $\overline{CE1}$ is 2.4V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.6V, I_{DSS1} current flows.
3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition $CE2 \leq 0.2V$.

TC551001APL/AFL/AFTL/ATRL-70L/85L/10L(LT)

SILICON GATE CMOS

131,072 WORD x 8 BIT STATIC RAM

Description

The TC551001APL is a 1,048,576 bit CMOS static random access memory organized as 131,072 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns. When $\overline{CE1}$ is a logical high, or $\overline{CE2}$ is low, the device is placed in a low power standby mode in which the standby current is 2 μ A typically. The TC551001APL has three control inputs. Chip enable inputs ($\overline{CE1}$, $\overline{CE2}$) allow for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. The TC551001APL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required. The TC551001APL-L(LT) has an operating temperature range of -20 ~ 70°C so it is suitable for use in low temperature applications.

The TC551001APL is offered in a standard dual-in-line 32-pin plastic package, a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 4 μ A (max.) at Ta = 25°C
- Single 5V power supply
- Access time (max.)

	TC551001APL/AFL/AFTL/ATRL		
	-70L(LT)	-85L(LT)	-10L(LT)
Access Time	70ns	85ns	100ns
$\overline{CE1}$ Access Time	70ns	85ns	100ns
$\overline{CE2}$ Access Time	70ns	85ns	100ns
\overline{OE} Access Time	35ns	45ns	50ns

- Power down feature: $\overline{CE1}$, $\overline{CE2}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Wide operating temperature: -20 ~ 70°C
- Inputs and outputs TTL compatible
- Package
 - TC551001APL : DIP32-P-600
 - TC551001AFL : SOP32-P-525
 - TC551001AFTL : TSOP32-P-0820
 - TC551001ATRL : TSOP32-P-0820A

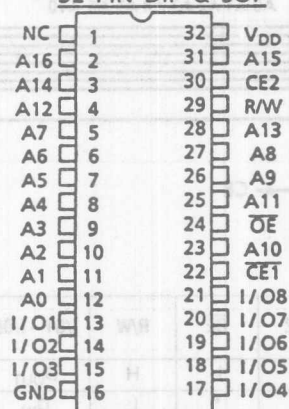
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
$\overline{CE1}$, $\overline{CE2}$	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground
NC	No Connection

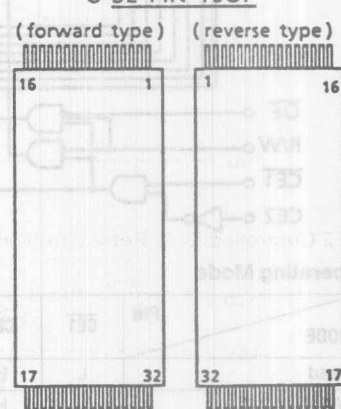
PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CE2	A ₁₅	V _{DD}	NC	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A ₁₀	\overline{OE}

Pin Connection (Top View)

32 PIN DIP & SOP



32 PIN TSOP



The diagram illustrates the internal structure of the T16C45 1024 x 8 bit static RAM. It features a central **MEMORY CELL ARRAY** (512 x 64 x 32, 1048576) connected to a **ROW ADDRESS DECODER** and a **COLUMN ADDRESS DECODER**. The row address decoder is driven by a **ROW ADDRESS REGISTER** and a **ROW ADDRESS BUFFER**, which receive inputs A7 through A16. The column address decoder is driven by a **COLUMN ADDRESS REGISTER** and a **COLUMN ADDRESS BUFFER**, which receive inputs A0 through A7. A **SENSE AMP.** (Sense Amplifier) is connected to the column address decoder and the memory cell array. A **DATA CONTROL** block and a **CLOCK GENERATOR** are also shown, with the clock generator receiving inputs I/O1 through I/O8. The data control block is connected to the row address register, the column address register, and the sense amplifier. The memory cell array is connected to the row address decoder and the column address decoder. The sense amplifier is connected to the column address decoder and the memory cell array. The data control block is connected to the row address register, the column address register, and the sense amplifier. The clock generator is connected to the row address register, the column address register, and the sense amplifier. The memory cell array is connected to the row address decoder and the column address decoder. The sense amplifier is connected to the column address decoder and the memory cell array. The data control block is connected to the row address register, the column address register, and the sense amplifier. The clock generator is connected to the row address register, the column address register, and the sense amplifier.

MODE \ PIN	$\overline{\text{CE1}}$	CE2	$\overline{\text{OE}}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D _{OUT}	I _{DDO}
Write	L	H	*	L	D _{IN}	I _{DDO}
Output Deselect	L	H	H	H	High-Z	I _{DDO}
Standby	H	*	*	*	High-Z	I _{DDS}
	*	L	*	*	High-Z	I _{DDS}

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
V_{IO}	Input and Output Voltage	-0.5 ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0/0.6**	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	-20 ~ 70	°C

** SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3	—	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

DC Characteristics ($T_a = -20 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{LO}	Output Leakage Current	CE1 = V _{IH} or CE2 = V _{IL} or R/W = V _{IL} or OE = V _{IH} , V _{OUT} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V			-1.0	—	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V			4.0	—	—	mA
I _{DDO1}	Operating Current	CE1 = V _{IL} and CE2 = V _{IH} and R/W = V _{IH} , I _{OUT} = 0mA Other Inputs = V _{IH} /V _{IL}	t _{cycle}	Min.	—	—	70	mA
I _{DDO2}				1μs	—	—	20	
		CE1 = 0.2V and CE2 = V _{DD} - 0.2V R/W = V _{DD} - 0.2V I _{OUT} = 0mA Other Inputs = V _{DD} - 0.2V/0.2V	t _{cycle}	Min.	—	—	60	
1μs				—	—	10		
I _{DDS1}	Standby Current	CE1 = V _{IH} or CE2 = V _{IL}		—	—	3	mA	
I _{DDS2} ⁽¹⁾		CE1 = V _{DD} - 0.2V or CE2 = 0.2V		Ta = -20 ~ 70°C		—	—	30
		V _{DD} = 2.0V ~ 5.5V		Ta = 25°C		—	2	4

Note (1): If $\overline{CE1} \geq V_{DD} - 0.2V$, the specified limits are guaranteed under the condition $CE2 \geq V_{DD} - 0.2V$ or $CE2 \leq 0.2V$.

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -20 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551001APL/AFL/AFTL/ATRL							UNIT
		-70L(LT)		-85L(LT)		-10L(LT)			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Read Cycle Time	70	—	85	—	100	—	ns	
t _{ACC}	Address Access Time	—	70	—	85	—	100		
t _{CO1}	CE1 Access Time	—	70	—	85	—	100		
t _{CO2}	CE2 Access Time	—	70	—	85	—	100		
t _{OE}	Output Enable to Output in Valid	—	35	—	45	—	50		
t _{COE}	Chip Enable (CE1, CE2) to Output in Low-Z	5	—	5	—	5	—		
t _{OEE}	Output Enable to Output in Low-Z	0	—	0	—	0	—		
t _{OD}	Chip Enable (CE1, CE2) to Output in High-Z	—	25	—	30	—	35		
t _{ODO}	Output Enable to Output in High-Z	—	25	—	30	—	35		
t _{OH}	Output Data Hold Time	10	—	10	—	10	—		

Write Cycle

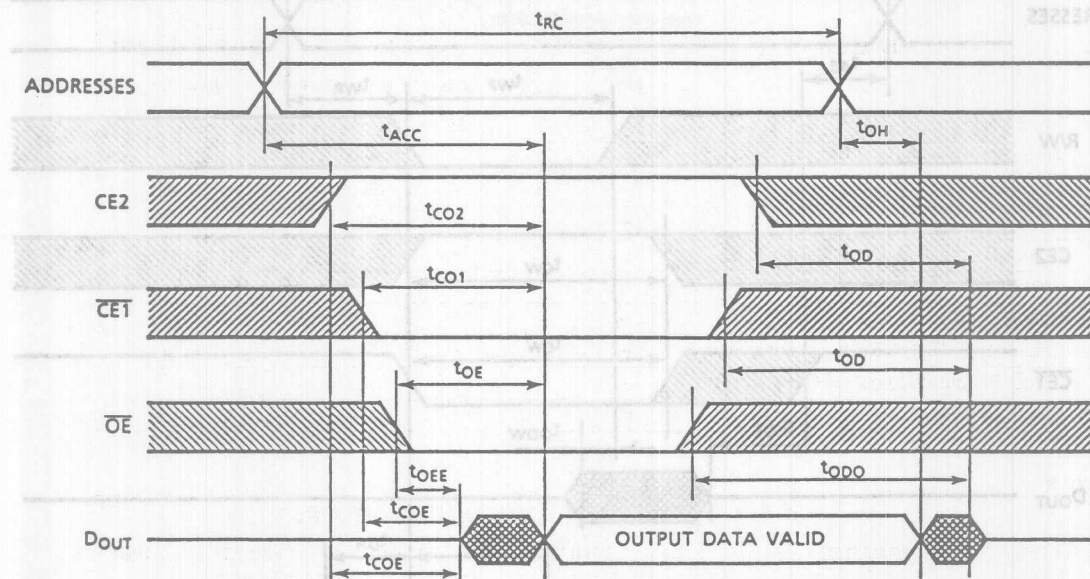
SYMBOL	PARAMETER	TC551001APL/AFL/AFTL/ATRL						UNIT
		-70L(LT)		-85L(LT)		-10L(LT)		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	70	—	85	—	100	—	ns
t _{WP}	Write Pulse Width	50	—	60	—	60	—	
t _{CW}	Chip Selection to End of Write	60	—	75	—	80	—	
t _{AS}	Address Setup Time	0	—	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	
t _{ODW}	R/W to Output in High-Z	—	25	—	30	—	35	
t _{OEW}	R/W to Output in Low-Z	0	—	0	—	0	—	
t _{DS}	Data Setup Time	30	—	35	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	

AC Test Conditions

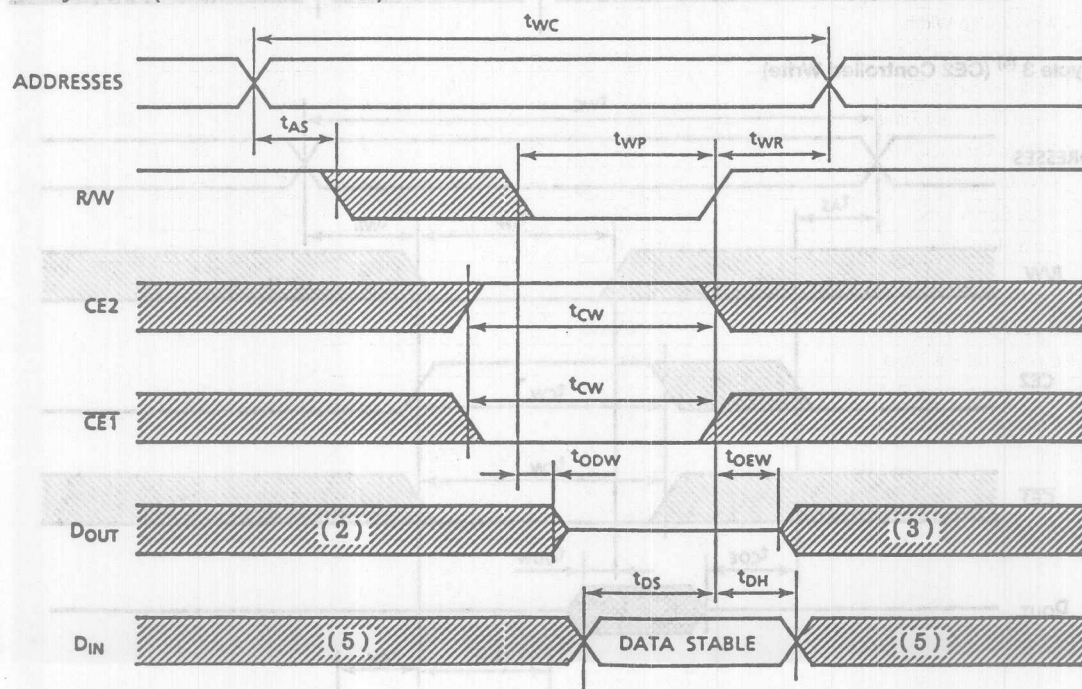
Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and C _L = 100pF

Timing Waveforms

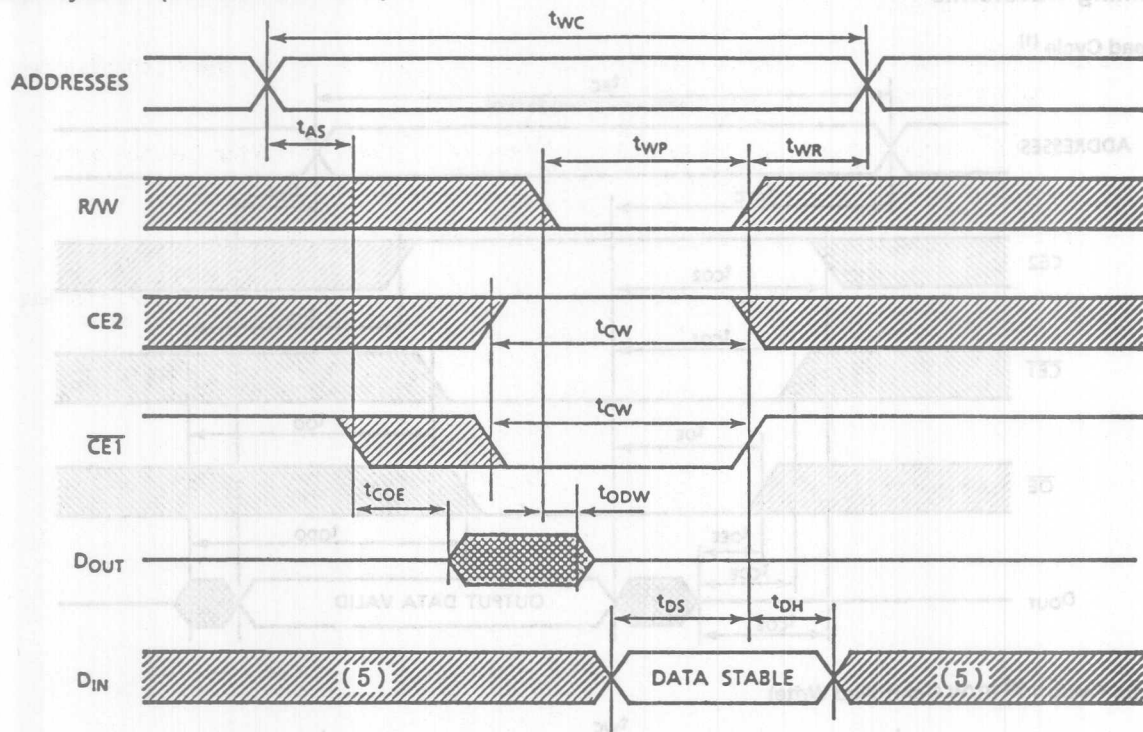
Read Cycle ⁽¹⁾



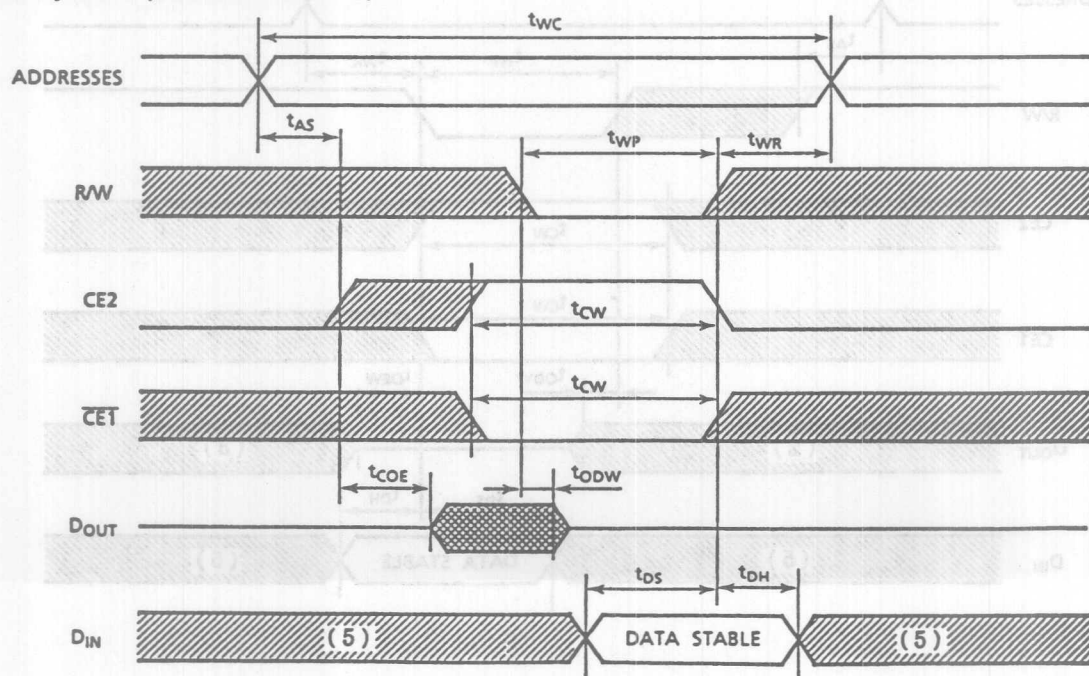
Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)



Write Cycle 2 ⁽⁴⁾ ($\overline{\text{CE1}}$ Controlled Write)

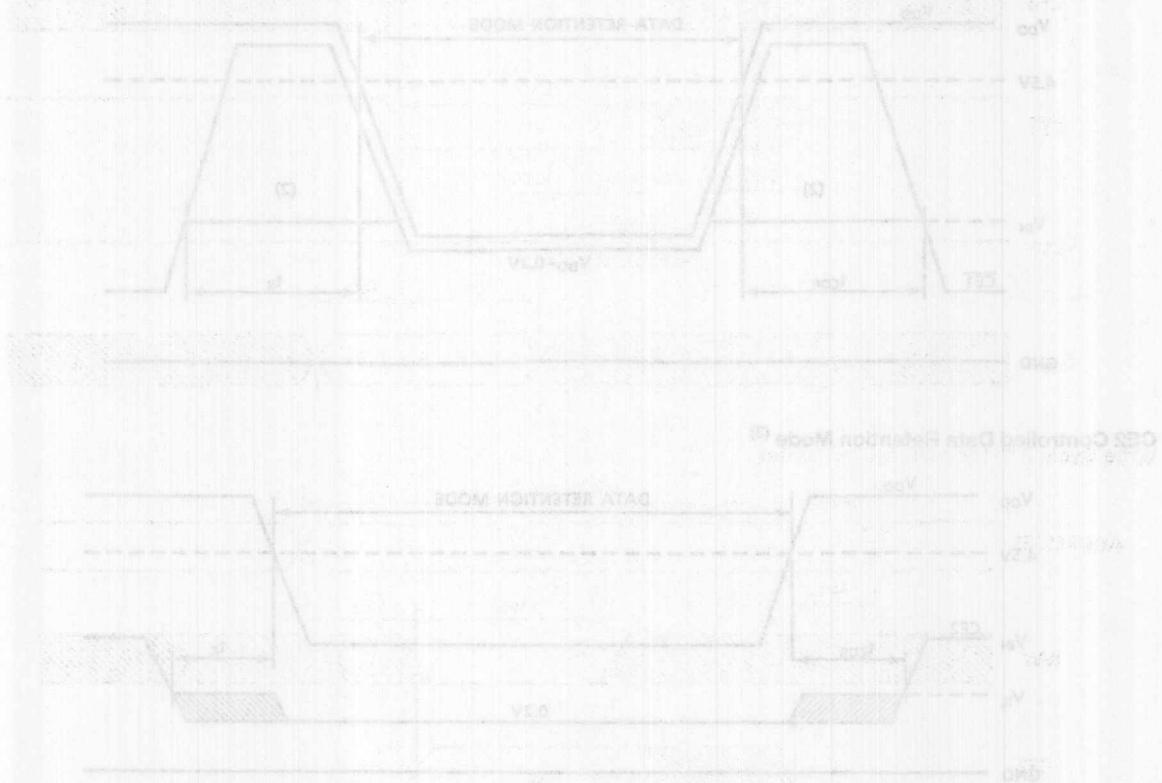


Write Cycle 3 ⁽⁴⁾ (CE2 Controlled Write)



Notes:

1. R/W is high for read cycles.
2. If the $\overline{CE1}$ low transition or CE2 high transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the $\overline{CE1}$ high transition or CE2 low transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.



Notes:

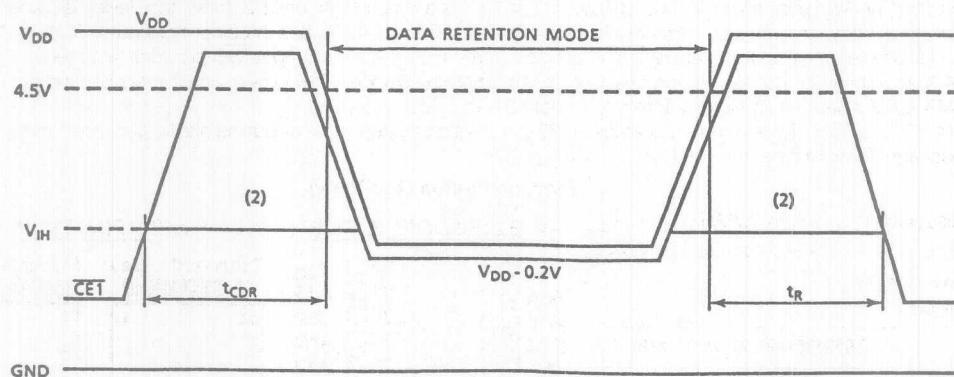
1. In the CE1 controlled data retention mode, minimum standby current is achieved under the condition $CE2 \leq 0.5V$ or $CE2 \leq 2.5V$.
2. In the V_{DD} of CE1 is 2.5V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.5V, logic current flows.
3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition $CE1 \leq 0.5V$.

Data Retention Characteristics (Ta = -20 ~ 70°C)

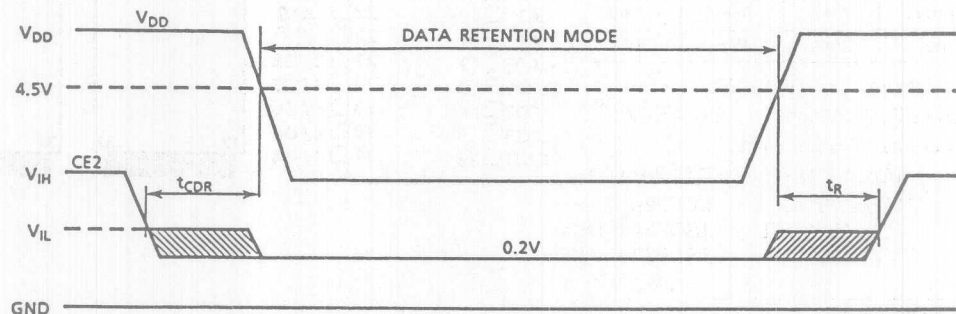
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DDS2}	Standby Current	$V_{DH} = 3.0V$	—	15*	μA
		$V_{DH} = 5.5V$	—	30	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	ns
t_R	Recovery Time	5	—	—	ms

* 3 μA (max.) Ta = -20 ~ 40°C

CE1 Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



Notes:

1. In the $\overline{CE1}$ controlled data retention mode, minimum standby current is achieved under the condition $CE2 \leq 0.2V$ or $CE2 \geq V_{DD} - 0.2V$.
2. If the V_{IH} of $\overline{CE1}$ is 2.4V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.6V, I_{DDS1} current flows.
3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition $CE2 \leq 0.2V$.

TC551001APL/AFL/AFTL/ATRL-70L/85L/10L(LV)

SILICON GATE CMOS

131,072 WORD x 8 BIT STATIC RAM

Description

The TC551001APL is a 1,048,576 bit CMOS static random access memory organized as 131,072 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns. When $\overline{CE1}$ is a logical high, or $\overline{CE2}$ is low, the device is placed in a low power standby mode in which the standby current is 2 μ A typically. The TC551001APL has three control inputs. Chip enable inputs ($\overline{CE1}$, $\overline{CE2}$) allow for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. The TC551001APL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required. The TC551001APL-L(LV) operates and is characterized at both 3 and 5 volts.

The TC551001APL is offered in a standard dual-in-line 32-pin plastic package, a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 4 μ A (max.) at $T_a = 25^\circ\text{C}$
- Single 5V power supply
- Access time (max.)

	TC551001APL/AFL/AFTL/ATRL		
	-70L(LV)	-85L(LV)	-10L(LV)
Access Time	70ns	85ns	100ns
$\overline{CE1}$ Access Time	70ns	85ns	100ns
$\overline{CE2}$ Access Time	70ns	85ns	100ns
\overline{OE} Access Time	35ns	45ns	50ns

- Power down feature: $\overline{CE1}$, $\overline{CE2}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package
 - TC551001APL : DIP32-P-600
 - TC551001AFL : SOP32-P-525
 - TC551001AFTL : TSOP32-P-0820
 - TC551001ATRL : TSOP32-P-0820A

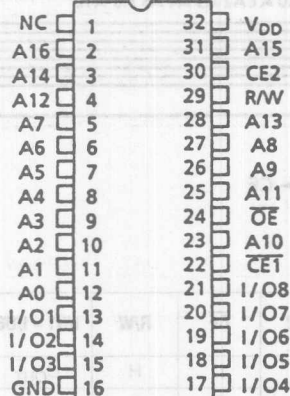
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
$\overline{CE1}$, $\overline{CE2}$	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground
NC	No Connection

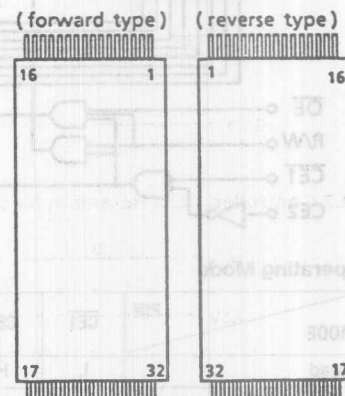
PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CE2	A ₁₅	V _{DD}	NC	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A ₁₀	\overline{OE}

Pin Connection (Top View)

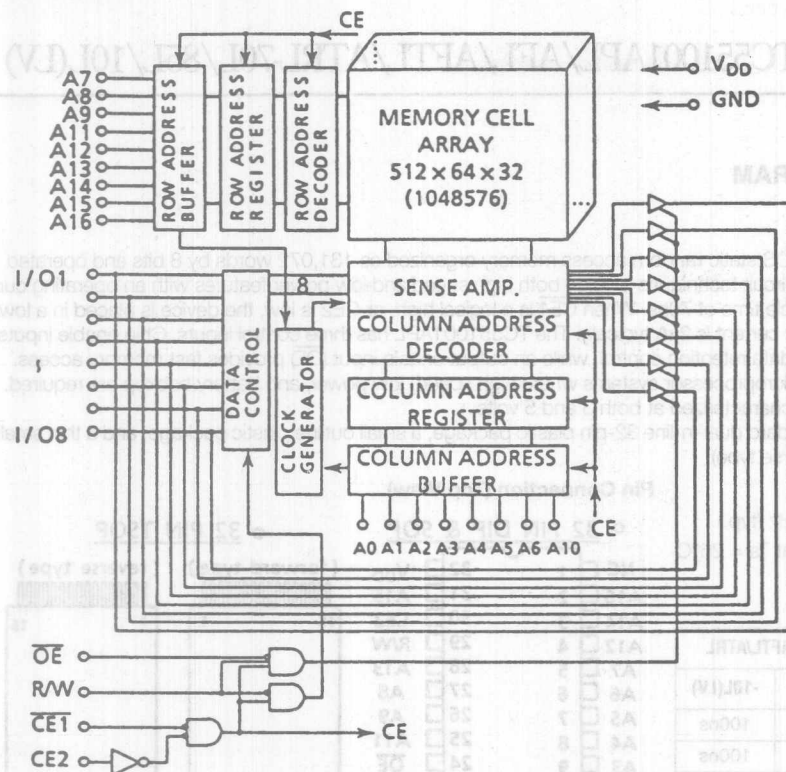
32 PIN DIP & SOP



32 PIN TSOP



Block Diagram



Operating Mode

MODE	PIN	$\overline{CE1}$	CE2	\overline{OE}	R/W	I/O1 ~ I/O8	POWER
Read		L	H	L	H	D _{OUT}	I _{DDO}
Write		L	H	*	L	D _{IN}	I _{DDO}
Output Deselect		L	H	H	H	High-Z	I _{DDO}
Standby		H	*	*	*	High-Z	I _{DDO}
		*	L	*	*	High-Z	I _{DDO}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V with a pulse width of 50ns

** SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3	—	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER		TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current		V _{IN} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{LO}	Output Leakage Current		CE1 = V _{IH} or CE2 = V _{IL} or R/W = V _{IL} or OE = V _{IH} , V _{OUT} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{OH}	Output High Current		V _{OH} = 2.4V			-1.0	—	—	mA
I _{OL}	Output Low Current		V _{OL} = 0.4V			4.0	—	—	mA
I _{DDO1}	Operating Current		CE1 = V _{IL} and CE2 = V _{IH} and R/W = V _{IH} , I _{OUT} = 0mA Other Inputs = V _{IH} /V _{IL}	t _{cycle}	Min.	—	—	70	mA
					1μs	—	—	20	
I _{DDO2}	Operating Current		CE1 = 0.2V and CE2 = V _{DD} - 0.2V R/W = V _{DD} - 0.2V I _{OUT} = 0mA Other Inputs = V _{DD} - 0.2V/0.2V	t _{cycle}	Min.	—	—	60	
					1μs	—	—	10	
I _{DDS1}	Standby Current		CE1 = V _{IH} or CE2 = V _{IL}		—	—	3	mA	
CE1 = V _{DD} - 0.2V or CE2 = 0.2V V _{DD} = 2.0V ~ 5.5V			Ta = 0 ~ 70°C		—	—	30	μA	
			Ta = 25°C		—	2	4		

Note (1): If $\overline{CE1} \geq V_{DD} - 0.2V$, the specified limits are guaranteed under the condition $CE2 \geq V_{DD} - 0.2V$ or $CE2 \leq 0.2V$.

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551001APL/AFL/AFTL/ATRL						UNIT
		-70L(LV)		-85L(LV)		-10L(LV)		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	70	—	85	—	100	—	ns
t _{ACC}	Address Access Time	—	70	—	85	—	100	
t _{CO1}	CE1 Access Time	—	70	—	85	—	100	
t _{CO2}	CE2 Access Time	—	70	—	85	—	100	
t _{OE}	Output Enable to Output in Valid	—	35	—	45	—	50	
t _{COE}	Chip Enable ($\overline{\text{CE1}}$, CE2) to Output in Low-Z	10	—	10	—	10	—	
t _{OOE}	Output Enable to Output in Low-Z	5	—	5	—	5	—	
t _{OD}	Chip Enable ($\overline{\text{CE1}}$, CE2) to Output in High-Z	—	25	—	30	—	35	
t _{ODO}	Output Enable to Output in High-Z	—	25	—	30	—	35	
t _{OH}	Output Data Hold Time	10	—	10	—	10	—	

Write Cycle

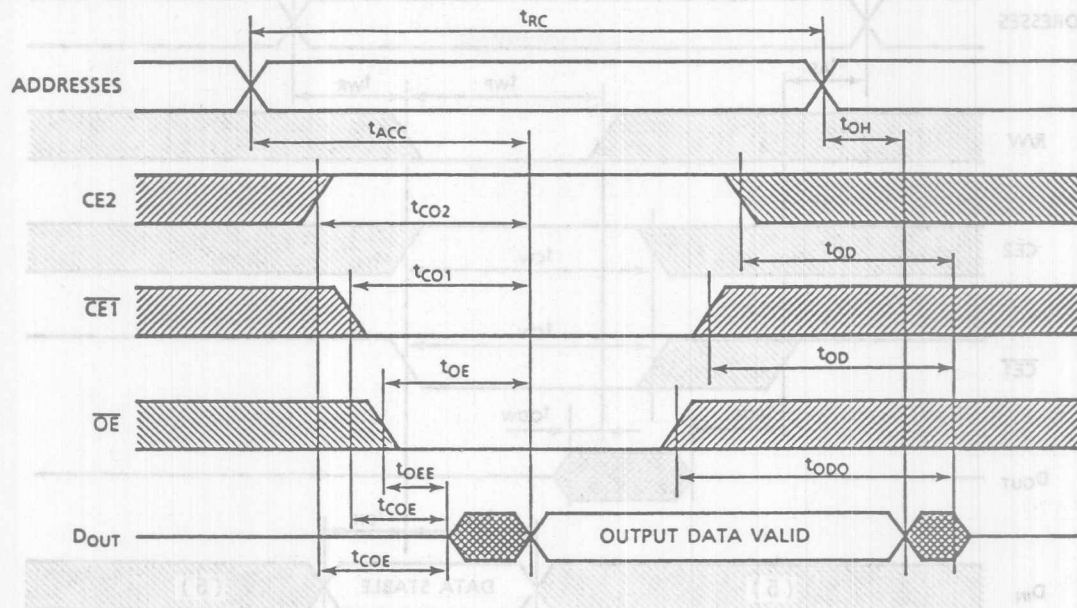
SYMBOL	PARAMETER	TC551001APL/AFL/AFTL/ATRL							UNIT
		-70L(LV)		-85L(LV)		-10L(LV)			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{WC}	Write Cycle Time	70	—	85	—	100	—	ns	
t _{WP}	Write Pulse Width	50	—	60	—	60	—		
t _{CW}	Chip Selection to End of Write	60	—	75	—	80	—		
t _{AS}	Address Setup Time	0	—	0	—	0	—		
t _{WR}	Write Recovery Time	0	—	0	—	0	—		
t _{ODW}	R/W to Output in High-Z	—	25	—	30	—	35		
t _{OEW}	R/W to Output in Low-Z	5	—	5	—	5	—		
t _{DS}	Data Setup Time	30	—	35	—	40	—		
t _{DH}	Data Hold Time	0	—	0	—	0	—		

AC Test Conditions

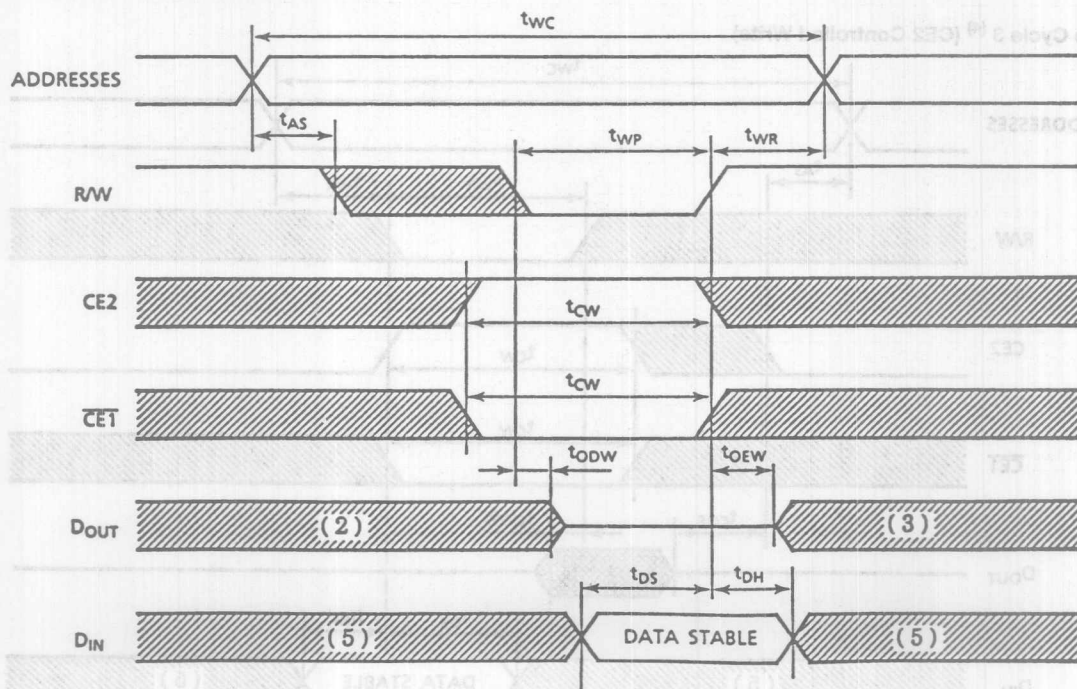
Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and C _L = 100pF

Timing Waveforms

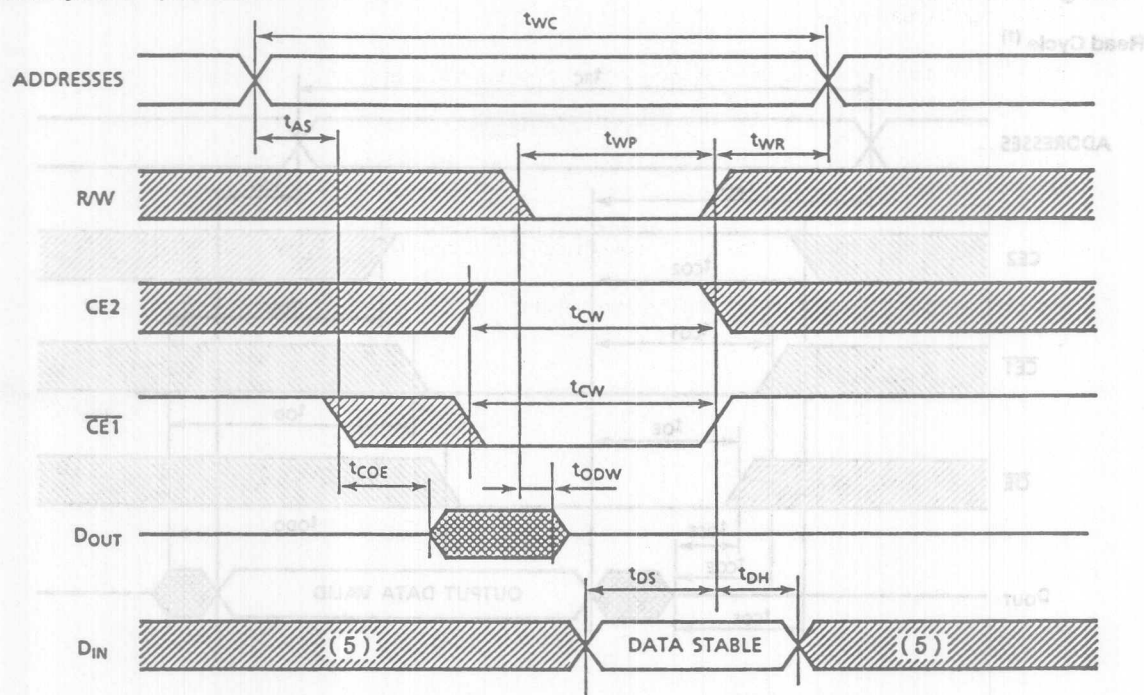
Read Cycle ⁽¹⁾



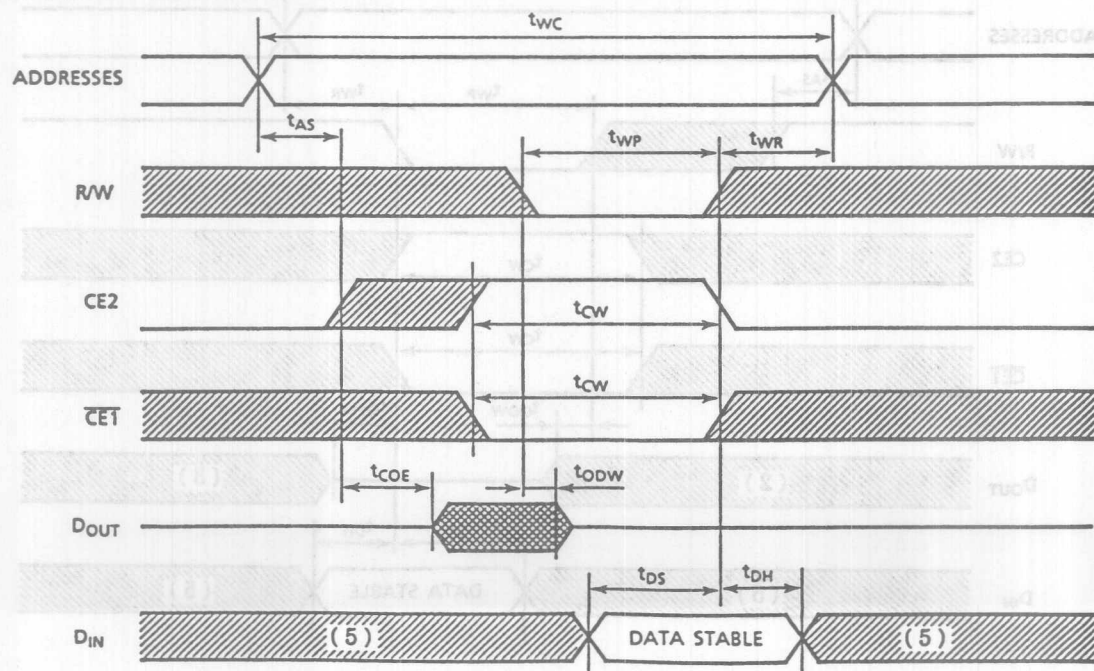
Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)



Write Cycle 2 ⁽⁴⁾ ($\overline{\text{CE1}}$ Controlled Write)

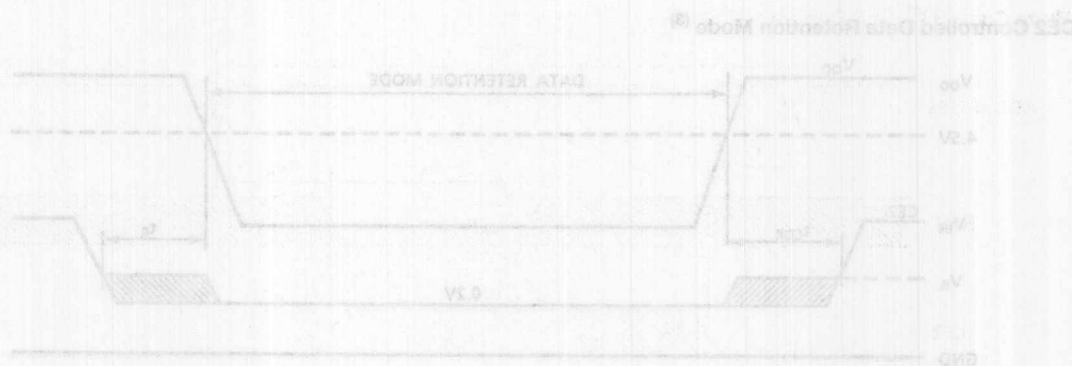
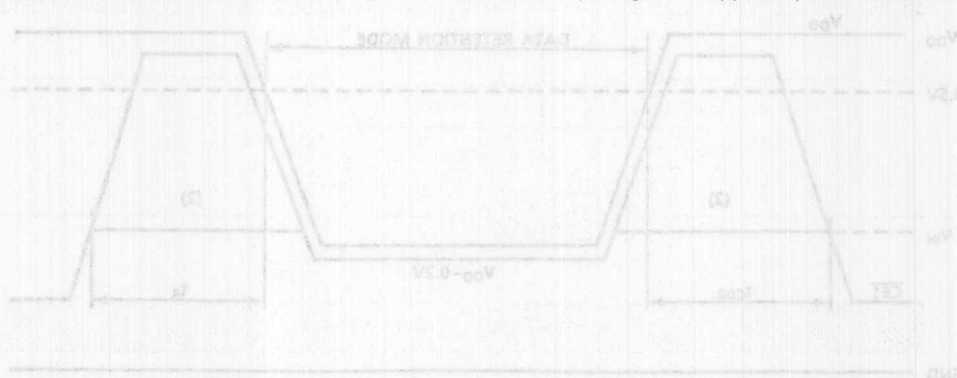


Write Cycle 3 ⁽⁴⁾ (CE2 Controlled Write)



Notes:

1. R/W is high for read cycles.
2. If the $\overline{CE1}$ low transition or CE2 high transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the $\overline{CE1}$ high transition or CE2 low transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.

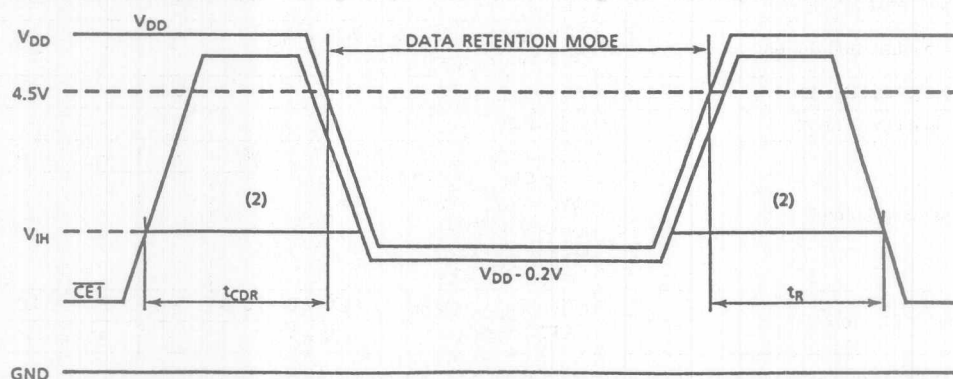
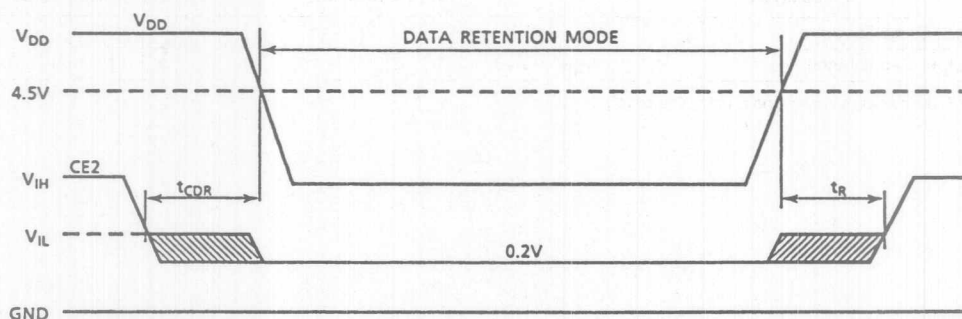


- Notes:
1. In the $\overline{CE1}$ controlled data retention mode, minimum standby current is achieved under the condition $V_{CE2} \leq 0.5V$ or $V_{CE2} = V_{DD} - 0.5V$.
 2. If the V_{CE1} of $\overline{CE1}$ is $2.5V$ in operation, during the period that the V_{DD} voltage is going down from $4.5V$ to $2.5V$, power cannot follow.
 3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition $V_{CE1} \leq 0.5V$.

Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DDS2}	Standby Current	$V_{DH} = 3.0V$	—	15*	μA
		$V_{DH} = 5.5V$	—	30	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	ns
t_R	Recovery Time	5	—	—	ms

* 3 μA (max.) Ta = 0 ~ 40°C

 $\overline{CE1}$ Controlled Data Retention Mode ⁽¹⁾

CE2 Controlled Data Retention Mode ⁽³⁾


Notes:

1. In the $\overline{CE1}$ controlled data retention mode, minimum standby current is achieved under the condition $CE2 \leq 0.2V$ or $CE2 \geq V_{DD} - 0.2V$.
2. If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.
3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition $CE2 \leq 0.2V$.

3V Operation

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	2.7	3.0	3.3	V
V_{IH}	Input High Voltage	$V_{DD} - 0.2$	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3	—	0.2	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 3V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = V_{DD} - 0.2V$	-0.1	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.2V$	0.1	—	—	mA
I_{DDO2}	Operating Current	$\overline{CE1} = 0.2V$ and $CE2 = V_{DD} - 0.2V$ $R/W = V_{DD} - 0.2V$ $I_{OUT} = 0\text{mA}$ Other Inputs = $V_{DD} - 0.2V/0.2V$	Min.	—	20	mA
			t_{cycle} 1 μs	—	5	
$I_{DDs2}^{(1)}$	Standby Current	$\overline{CE1} = V_{DD} - 0.2V$ or $CE2 = 0.2V$	$T_a = 0 \sim 70^\circ\text{C}$	—	20	μA
			$T_a = 25^\circ\text{C}$	1	2	

Note (1): If $\overline{CE1} \geq V_{DD} - 0.2V$, the specified limits are guaranteed under the condition $CE2 \geq V_{DD} - 0.2V$ or $CE2 \leq 0.2V$.

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

3V Operation

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 3V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	150	—	
t_{ACC}	Address Access Time	—	150	
t_{CO1}	CE1 Access Time	—	150	
t_{CO2}	CE2 Access Time	—	150	
t_{OE}	Output Enable to Output in Valid	—	75	ns
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	—	
t_{OOE}	Output Enable to Output in Low-Z	5	—	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	—	50	
t_{ODO}	Output Enable to Output in High-Z	—	50	
t_{OH}	Output Data Hold Time	10	—	

Write Cycle

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	150	—	ns
t_{WP}	Write Pulse Width	100	—	
t_{CW}	Chip Selection to End of Write	120	—	
t_{AS}	Address Setup Time	0	—	
t_{WR}	Write Recovery Time	0	—	
t_{ODW}	R/W to Output in High-Z	—	50	
t_{OEW}	R/W to Output in Low-Z	5	—	
t_{DS}	Data Setup Time	60	—	
t_{DH}	Data Hold Time	0	—	

AC Test Conditions

Input Pulse Levels	$V_{DD} - 0.2V/0.2V$
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	$C_L = 100\text{pF}$

TC551001API/AFI/AFTI/ATRI-85/10

SILICON GATE CMOS

131,072 WORD x 8 BIT STATIC RAM

Description

The TC551001API is a 1,048,576 bit CMOS static random access memory organized as 131,072 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 85ns. When $\overline{CE1}$ is a logical high, or $\overline{CE2}$ is low, the device is placed in a low power standby mode in which the standby current is 2 μ A typically. The TC551001API has three control inputs. Chip enable inputs ($\overline{CE1}$, $\overline{CE2}$) allow for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. The TC551001API is suitable for use in microprocessor systems where high speed, low power, and battery backup are required. The TC551001API has an operating temperature range of -40 ~ 85°C so it is suitable for use in wide operating temperature systems.

The TC551001API is offered in a standard dual in-line 32-pin plastic package, a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 200 μ A (max.)
- Single 5V power supply
- Access time (max.)

	TC551001API/AFI/AFTI/ATRI	
	-85	-10
Access Time	85ns	100ns
$\overline{CE1}$ Access Time	85ns	100ns
$\overline{CE2}$ Access Time	85ns	100ns
\overline{OE} Access Time	45ns	50ns

- Power down feature: $\overline{CE1}$, $\overline{CE2}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Wide operating temperature: -40 ~ 85°C
- Package

TC551001API	: DIP32-P-600
TC551001AFI	: SOP32-P-525
TC551001AFTI	: TSOP32-P-0820
TC551001ATRI	: TSOP32-P-0820A

Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
$\overline{CE1}$, $\overline{CE2}$	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground
NC	No Connection

Pin Connection (Top View)

32 PIN DIP & SOP

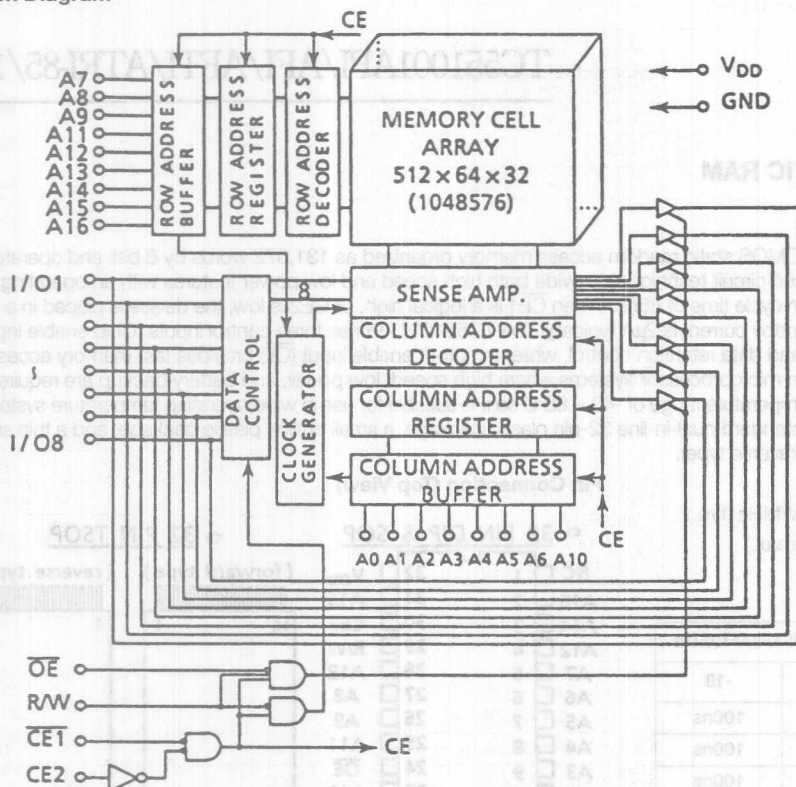
NC	1	32	V _{DD}
A16	2	31	A15
A14	3	30	$\overline{CE2}$
A12	4	29	R/W
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	\overline{OE}
A2	10	23	A10
A1	11	22	$\overline{CE1}$
A0	12	21	I/O8
I/O1	13	20	I/O7
I/O2	14	19	I/O6
I/O3	15	18	I/O5
GND	16	17	I/O4

32 PIN TSOP

(forward type)		(reverse type)	
16	1	1	16
17	32	32	17

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	$\overline{CE2}$	A ₁₅	V _{DD}	NC	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A ₁₀	\overline{OE}

Block Diagram



Operating Mode

MODE	PIN	CE1	CE2	OE	R/W	I/O1 ~ I/O8	POWER
Read		L	H	L	H	D _{OUT}	I _{DDO}
Write		L	H	*	L	D _{IN}	I _{DDO}
Output Deselect		L	H	H	H	High-Z	I _{DDO}
Standby		H	*	*	*	High-Z	I _{DDO}
		*	L	*	*	High-Z	I _{DDO}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3 ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	-40 ~ 85	°C

* -3.0V with a pulse width of 50ns

** SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3	—	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

DC Characteristics ($T_a = -40 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{LO}	Output Leakage Current	CE1 = V _{IH} or CE2 = V _{IL} or R/W = V _{IL} or OE = V _{IH} , V _{OUT} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V			-1.0	—	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V			4.0	—	—	mA
I _{DDO1}	Operating Current	CE1 = V _{IL} and CE2 = V _{IH} and R/W = V _{IH} , I _{OUT} = 0mA Other Inputs = V _{IH} /V _{IL}	t _{cycle}	Min.	—	—	70	mA
				1μs	—	—	20	
I _{DDO2}		CE1 = 0.2V and CE2 = V _{DD} - 0.2V R/W = V _{DD} - 0.2V I _{OUT} = 0mA Other Inputs = V _{DD} - 0.2V/0.2V	t _{cycle}	Min.	—	—	60	
				1μs	—	—	10	
I _{DDS1}	Standby Current	CE1 = V _{IH} or CE2 = V _{IL}		—	—	3	mA	
I _{DDS2} ⁽¹⁾		CE1 = V _{DD} - 0.2V or CE2 = 0.2V V _{DD} = 2.0V ~ 5.5V	Ta = -40 ~ 85°C	—	—	200	μA	
			Ta = 25°C	—	2	—		

Note (1): If $\overline{CE1} \geq V_{DD} - 0.2V$, the specified limits are guaranteed under the condition $CE2 \geq V_{DD} - 0.2V$ or $CE2 \leq 0.2V$.

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551001API/AFI/AFTI/ATRI				UNIT
		-85		-10		
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	85	—	100	—	ns
t _{ACC}	Address Access Time	—	85	—	100	
t _{CO1}	$\overline{\text{CE1}}$ Access Time	—	85	—	100	
t _{CO2}	CE2 Access Time	—	85	—	100	
t _{OE}	Output Enable to Output in Valid	—	45	—	50	
t _{COE}	Chip Enable ($\overline{\text{CE1}}$, CE2) to Output in Low-Z	5	—	5	—	
t _{OEE}	Output Enable to Output in Low-Z	0	—	0	—	
t _{OD}	Chip Enable ($\overline{\text{CE1}}$, CE2) to Output in High-Z	—	35	—	40	
t _{ODO}	Output Enable to Output in High-Z	—	35	—	40	
t _{OH}	Output Data Hold Time	10	—	10	—	

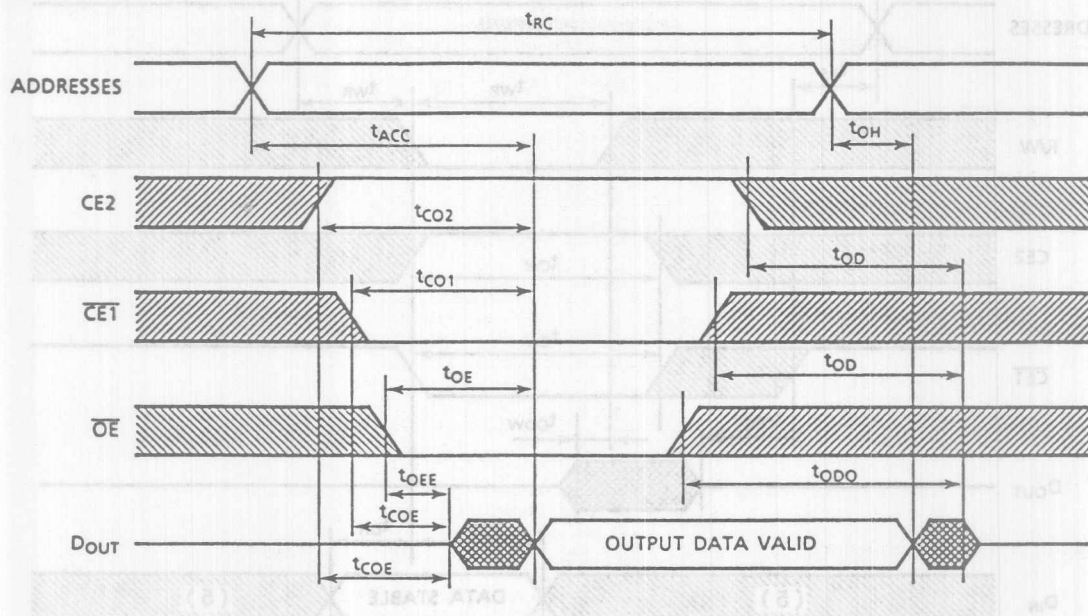
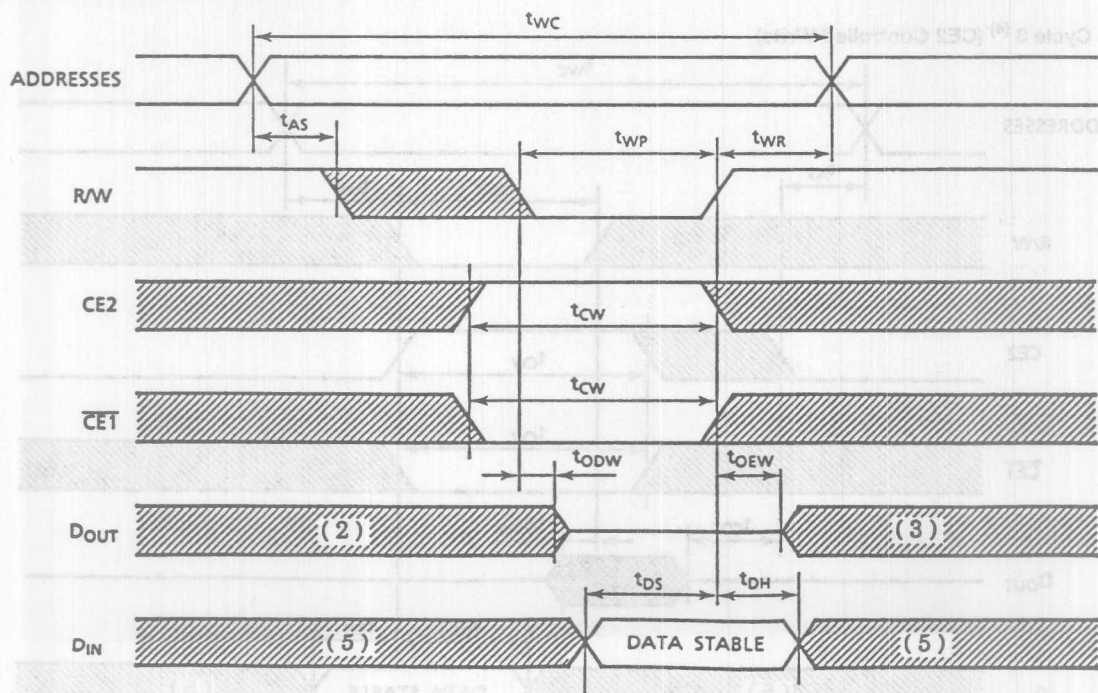
Write Cycle

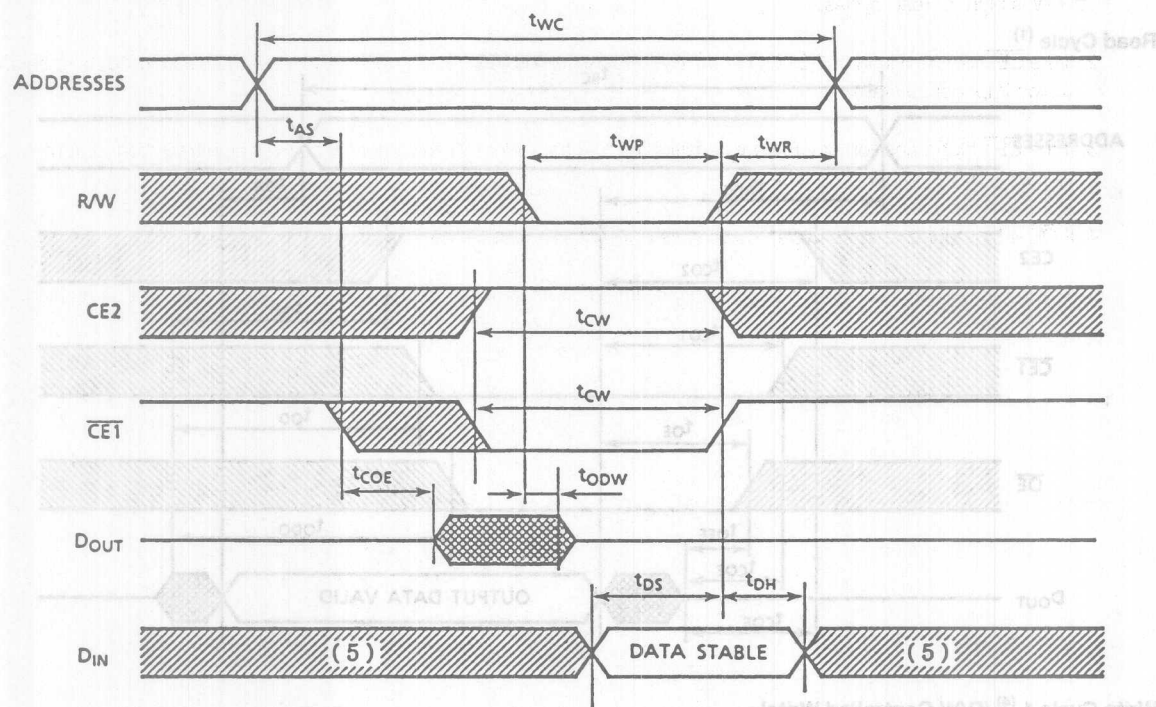
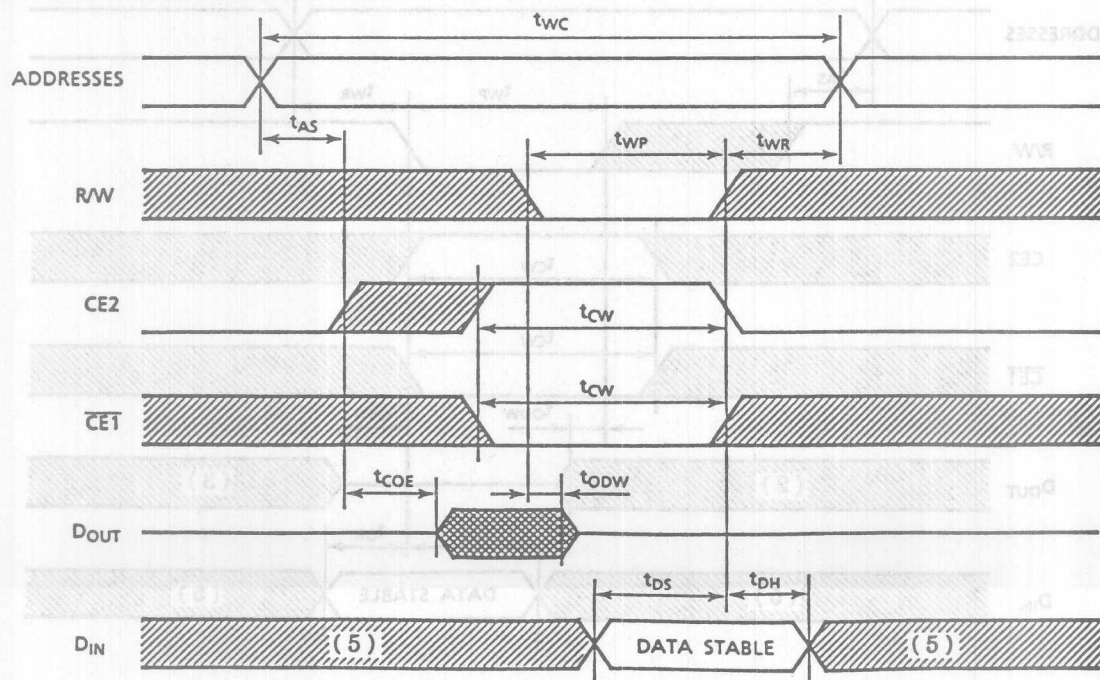
SYMBOL	PARAMETER	TC551001API/AFI/AFTI/ATRI				UNIT
		-85		-10		
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	85	—	100	—	ns
t _{WP}	Write Pulse Width	60	—	60	—	
t _{CW}	Chip Selection to End of Write	75	—	80	—	
t _{AS}	Address Setup Time	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	
t _{ODW}	R/W to Output in High-Z	—	35	—	40	
t _{OEW}	R/W to Output in Low-Z	0	—	0	—	
t _{DS}	Data Setup Time	35	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	

AC Test Conditions

Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and C _L = 100pF

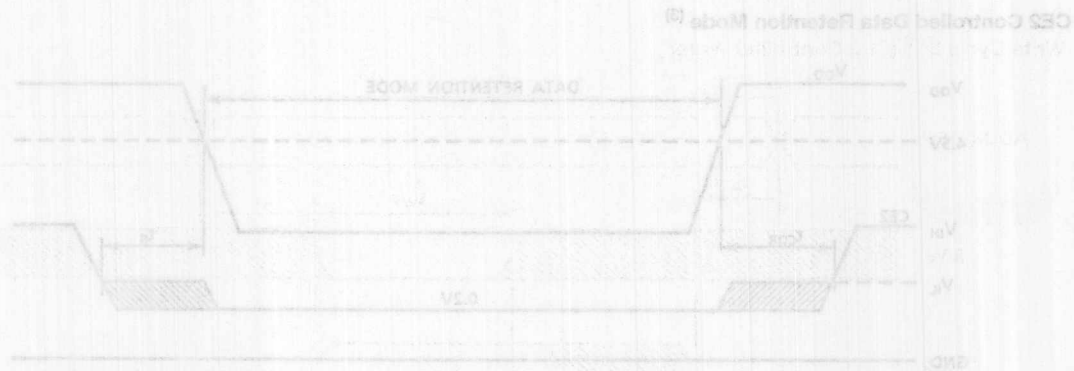
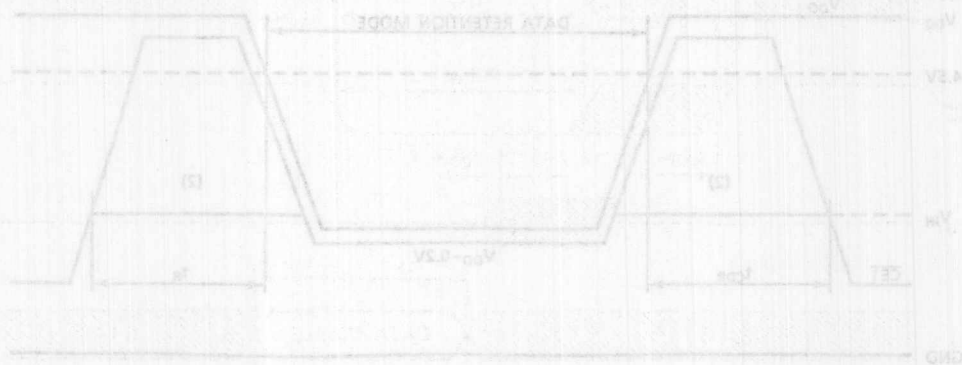
Timing Waveforms

Read Cycle ⁽¹⁾Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)

Write Cycle 2 ⁽⁴⁾ ($\overline{\text{CE1}}$ Controlled Write)Write Cycle 3 ⁽⁴⁾ (CE2 Controlled Write)

Notes:

1. R/W is high for read cycles.
2. If the $\overline{\text{CE1}}$ low transition or CE2 high transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the $\overline{\text{CE1}}$ high transition or CE2 low transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If $\overline{\text{OE}}$ is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.

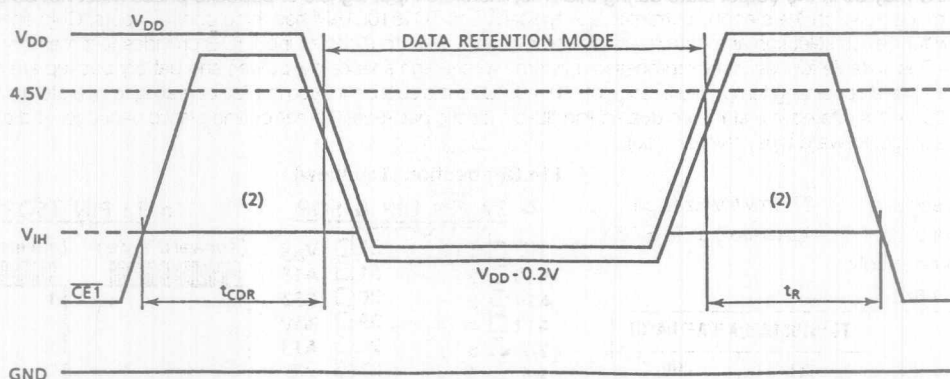
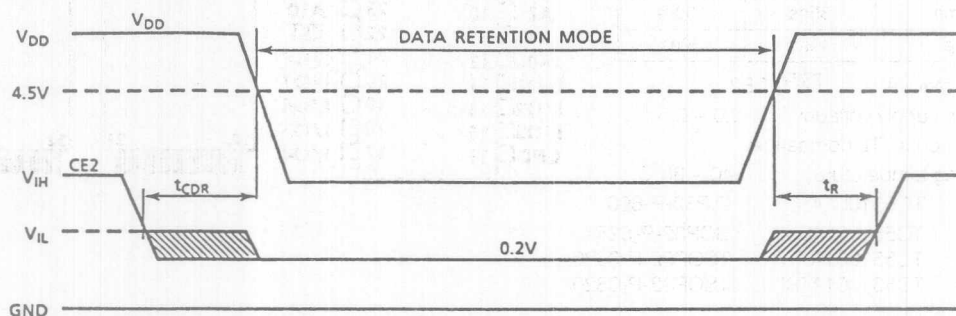


Notes:

1. In the CE1 controlled data retention mode, minimum standby current is achieved when the output CE1 is 2.5V or less.
2. If the Vcc or CE1 is 2.5V in operation, during the period that the Vcc voltage is going down from 4.5V to 2.5V, the current flows.
3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition CE2 is 0.5V.

Data Retention Characteristics (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DDS2}	Standby Current	$V_{DH} = 3.0V$	—	100	μA
		$V_{DH} = 5.5V$	—	200	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	ns
t_R	Recovery Time	5	—	—	ms

 $\overline{CE1}$ Controlled Data Retention Mode ⁽¹⁾CE2 Controlled Data Retention Mode ⁽³⁾

Notes:

1. In the $\overline{CE1}$ controlled data retention mode, minimum standby current is achieved under the condition $CE2 \leq 0.2V$ or $CE2 \geq V_{DD} - 0.2V$.
2. If the V_{IH} of $\overline{CE1}$ is 2.4V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.6V, I_{DPS1} current flows.
3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition $CE2 \leq 0.2V$.

TC551001API/AFI/AFTI/ATRI-85L/10L

SILICON GATE CMOS

131,072 WORD x 8 BIT STATIC RAM

Description

The TC551001API is a 1,048,576 bit CMOS static random access memory organized as 131,072 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 85ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in a low power standby mode in which the standby current is 2 μ A typically. The TC551001API has three control inputs. Chip enable inputs ($\overline{CE1}$, CE2) allow for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. The TC551001API is suitable for use in microprocessor systems where high speed, low power, and battery backup are required. The TC551001API has an operating temperature range of -40 ~ 85°C so it is suitable for use in wide operating temperature systems.

The TC551001API is offered in a standard dual-in-line 32-pin plastic package, a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 4 μ A (max.) at $T_a = 25^\circ\text{C}$
- Single 5V power supply
- Access time (max.)

	TC551001API/AFI/AFTI/ATRI	
	-85L	-10L
Access Time	85ns	100ns
$\overline{CE1}$ Access Time	85ns	100ns
CE2 Access Time	85ns	100ns
\overline{OE} Access Time	45ns	50ns

- Power down feature: $\overline{CE1}$, CE2
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Wide operating temperature: -40 ~ 85°C
- Package

TC551001API	: DIP32-P-600
TC551001AFI	: SOP32-P-525
TC551001AFTI	: TSOP32-P-0820
TC551001ATRI	: TSOP32-P-0820A

Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
NC	No Connection

Pin Connection (Top View)

32 PIN DIP & SOP

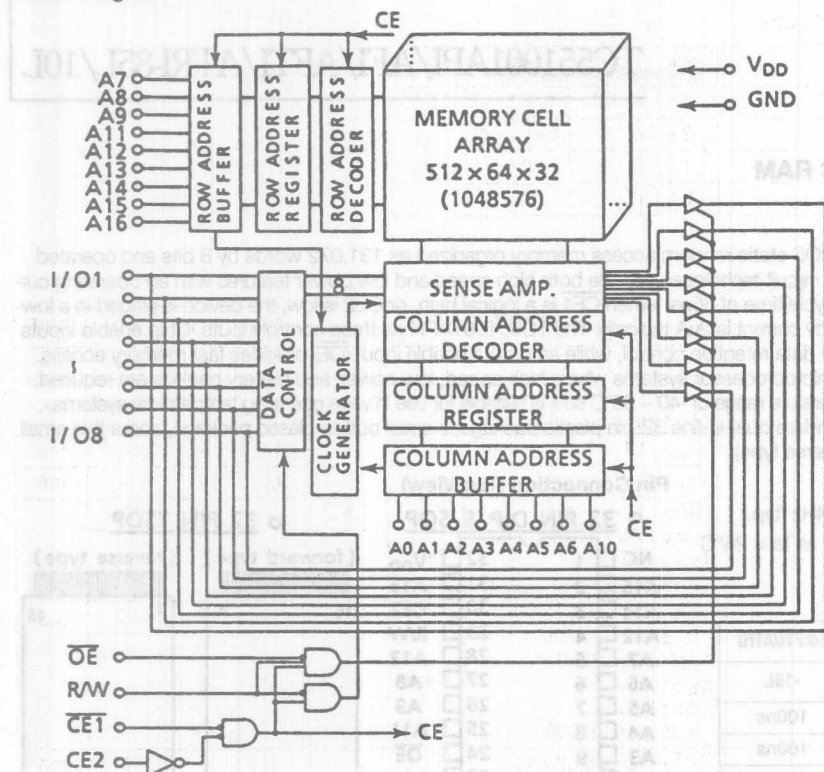
NC	1	32	V_{DD}
A16	2	31	A15
A14	3	30	CE2
A12	4	29	R/W
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	\overline{OE}
A2	10	23	A10
A1	11	22	$\overline{CE1}$
A0	12	21	I/O8
I/O1	13	20	I/O7
I/O2	14	19	I/O6
I/O3	15	18	I/O5
GND	16	17	I/O4

32 PIN TSOP

(forward type)	(reverse type)
16	1
17	32
32	17
1	16

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CE2	A ₁₅	V_{DD}	NC	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A ₁₀	\overline{OE}

Block Diagram



Operating Mode

MODE	PIN	$\overline{CE1}$	CE2	\overline{OE}	R/W	I/O1 ~ I/O8	POWER
Read		L	H	L	H	D _{OUT}	I _{DDO}
Write		L	H	*	L	D _{IN}	I _{DDO}
Output Deselect		L	H	H	H	High-Z	I _{DDO}
Standby		H	*	*	*	High-Z	I _{DDS}
		*	L	*	*	High-Z	I _{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	-40 ~ 85	°C

* -3.0V with a pulse width of 50ns

** SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3	—	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

DC Characteristics ($T_a = -40 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	-1.0	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	4.0	—	—	mA
I_{DDO1}	Operating Current	$\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$ and $R/W = V_{IH}$, $I_{OUT} = 0\text{mA}$ Other Inputs = V_{IH}/V_{IL}	Min.	—	—	70
			1 μs	—	—	20
I_{DDO2}		$\overline{CE1} = 0.2\text{V}$ and $CE2 = V_{DD} - 0.2\text{V}$ $R/W = V_{DD} - 0.2\text{V}$ $I_{OUT} = 0\text{mA}$ Other Inputs $= V_{DD} - 0.2\text{V}/0.2\text{V}$	Min.	—	—	60
			1 μs	—	—	10
I_{DDS1}	Standby Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$	—	—	3	mA
$I_{DDS2}^{(1)}$		$\overline{CE1} = V_{DD} - 0.2\text{V}$ or $CE2 = 0.2\text{V}$	$T_a = -40 \sim 85^\circ\text{C}$	—	—	70
		$V_{DD} = 2.0\text{V} \sim 5.5\text{V}$	$T_a = 25^\circ\text{C}$	—	2	4 μA

Note (1): If $\overline{CE1} \geq V_{DD} - 0.2\text{V}$, the specified limits are guaranteed under the condition $CE2 \geq V_{DD} - 0.2\text{V}$ or $CE2 \leq 0.2\text{V}$.

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551001API/AFI/AFTI/ATRI				UNIT
		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	85	—	100	—	ns
t _{ACC}	Address Access Time	—	85	—	100	
t _{CO1}	CE1 Access Time	—	85	—	100	
t _{CO2}	CE2 Access Time	—	85	—	100	
t _{OE}	Output Enable to Output in Valid	—	45	—	50	
t _{COE}	Chip Enable (CE1, CE2) to Output in Low-Z	5	—	5	—	
t _{OEE}	Output Enable to Output in Low-Z	0	—	0	—	
t _{OD}	Chip Enable (CE1, CE2) to Output in High-Z	—	35	—	40	
t _{ODO}	Output Enable to Output in High-Z	—	35	—	40	
t _{OH}	Output Data Hold Time	10	—	10	—	

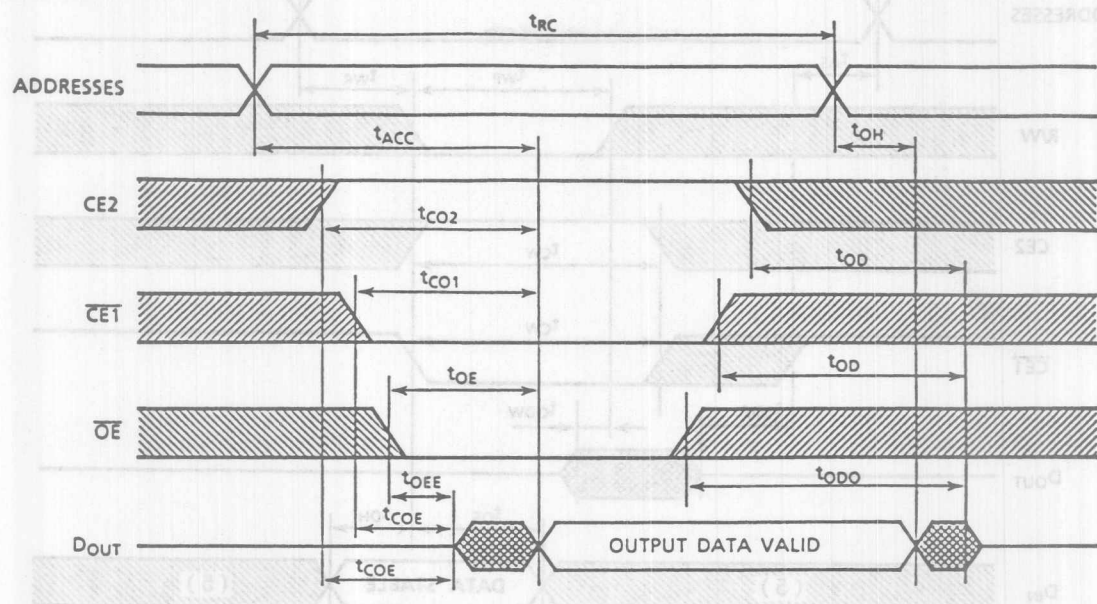
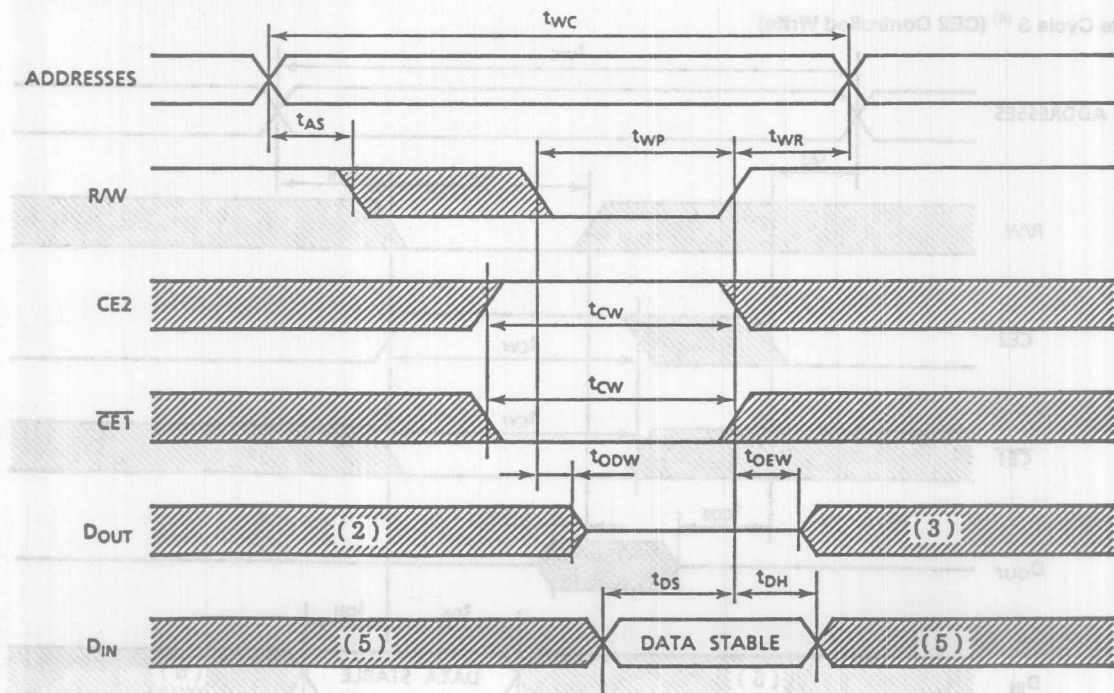
Write Cycle

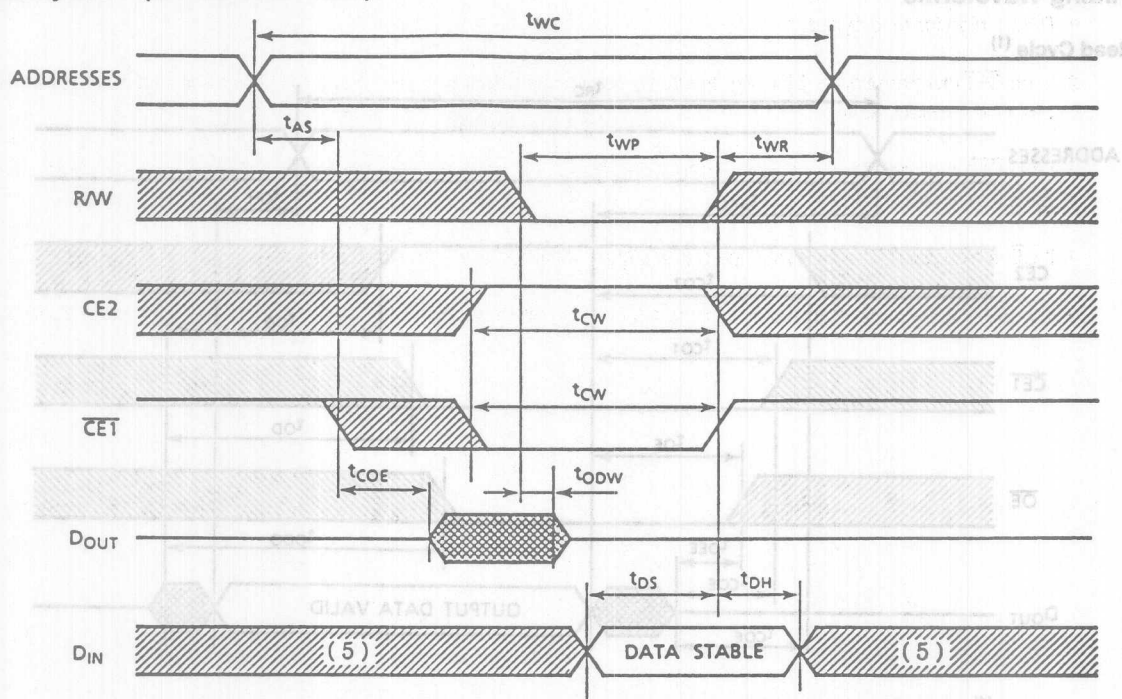
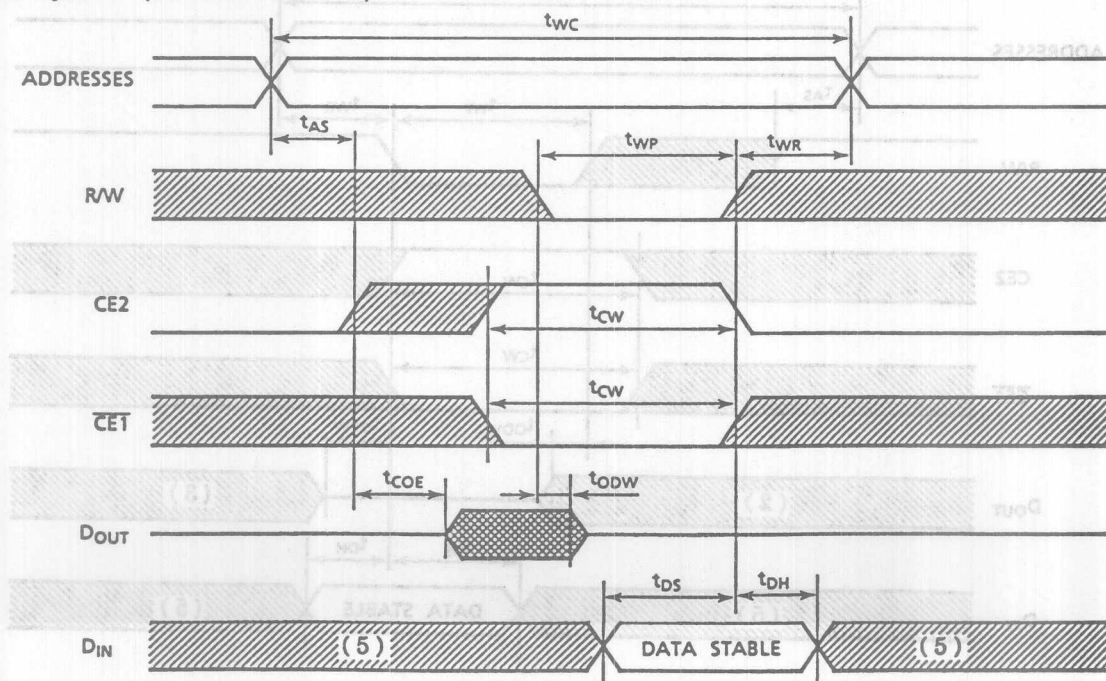
SYMBOL	PARAMETER	TC551001API/AFI/AFTI/ATRI				UNIT
		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	85	—	100	—	ns
t _{WP}	Write Pulse Width	60	—	60	—	
t _{CW}	Chip Selection to End of Write	75	—	80	—	
t _{AS}	Address Setup Time	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	
t _{ODW}	R/W to Output in High-Z	—	35	—	40	
t _{OEW}	R/W to Output in Low-Z	0	—	0	—	
t _{DS}	Data Setup Time	35	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	

AC Test Conditions

Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and C _L = 100pF

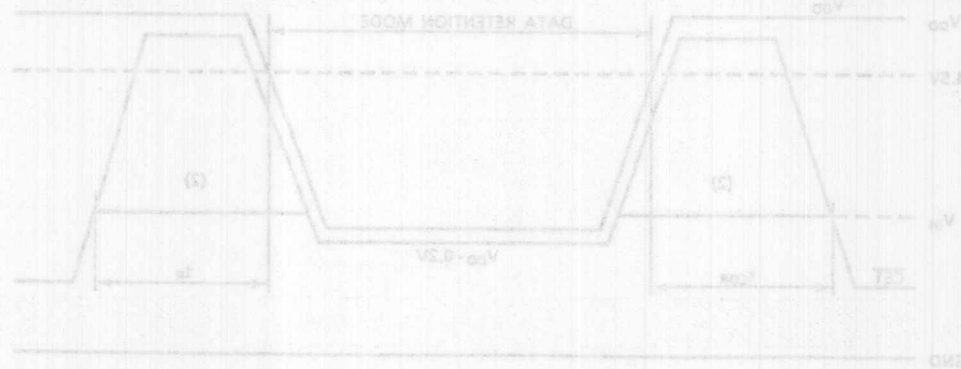
Timing Waveforms

Read Cycle ⁽¹⁾Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)

Write Cycle 2 ⁽⁴⁾ ($\overline{\text{CE1}}$ Controlled Write)Write Cycle 3 ⁽⁴⁾ (CE2 Controlled Write)

Notes:

1. R/W is high for read cycles.
2. If the $\overline{\text{CE1}}$ low transition or CE2 high transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the $\overline{\text{CE1}}$ high transition or CE2 low transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If $\overline{\text{OE}}$ is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.



Notes:

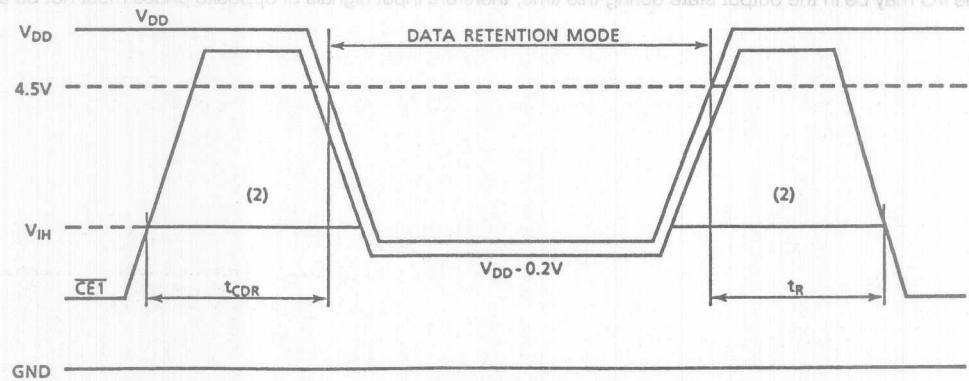
1. In the $\overline{\text{CE1}}$ controlled data retention mode, minimum standby current is achieved under the condition $\text{CE2} \leq 0.3\text{V}$ or $\text{CE2} = V_{\text{DD}} - 0.2\text{V}$.
2. If the V_{CE1} or CE2 is 2.0V or less, during the period that the V_{DD} voltage is going down from 4.5V to 2.0V, power current flows.
3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition $\text{CE1} \leq 0.3\text{V}$.

Data Retention Characteristics (Ta = -40 ~ 85°C)

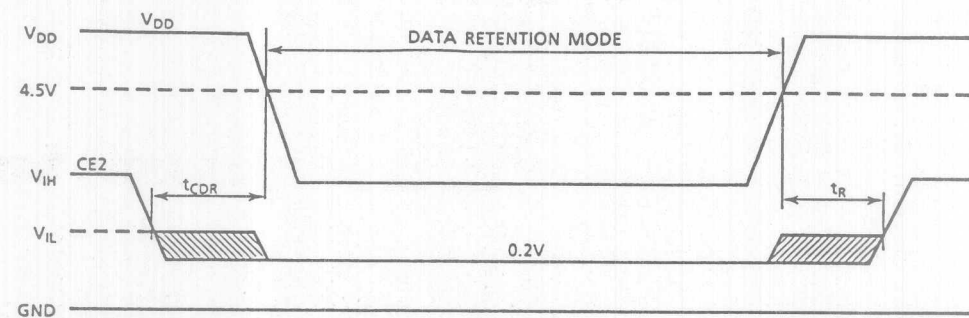
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V _{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I _{DDS2}	Standby Current	V _{DH} = 3.0V	—	—	35*	μA
		V _{DH} = 5.5V	—	—	70	
t _{CDR}	Chip Deselect to Data Retention Mode		0	—	—	ns
t _R	Recovery Time		5	—	—	ms

*3μA (max.) Ta = -40 ~ 40°C

CE1 Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



Notes:

1. In the $\overline{\text{CE1}}$ controlled data retention mode, minimum standby current is achieved under the condition $\text{CE2} \leq 0.2\text{V}$ or $\text{CE2} \geq V_{\text{DD}} - 0.2\text{V}$.
2. If the V_{IH} of $\overline{\text{CE1}}$ is 2.4V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.6V, I_{DDS1} current flows.
3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition CE2 ≤ 0.2V.

TC551001BPL/BFL/BFTL/BTRL-70/85/10

SILICON GATE CMOS

131,072 WORD x 8 BIT STATIC RAM

Description

The TC551001BPL is a 1,048,576 bit CMOS static random access memory organized as 131,072 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns. When CE1 is a logical high, or CE2 is low, the device is placed in a low power standby mode in which the standby current is 2μA typically. The TC551001BPL has three control inputs. Chip enable inputs (CE1, CE2) allow for device selection and data retention control, while an output enable input (OE) provides fast memory access. The TC551001BPL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required.

The TC551001BPL is offered in a standard dual-in-line 32-pin plastic package, a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 100μA (max.)
- Single 5V power supply
- Access time (max.)

	TC551001BPL/BFL/BFTL/BTRL		
	-70	-85	-10
Access Time	70ns	85ns	100ns
CE1 Access Time	70ns	85ns	100ns
CE2 Access Time	70ns	85ns	100ns
OE Access Time	35ns	45ns	50ns

- Power down feature: CE1, CE2
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package
 - TC551001BPL : DIP32-P-600
 - TC551001BFL : SOP32-P-525
 - TC551001BFTL : TSOP32-P-0820
 - TC551001BTRL : TSOP32-P-0820A

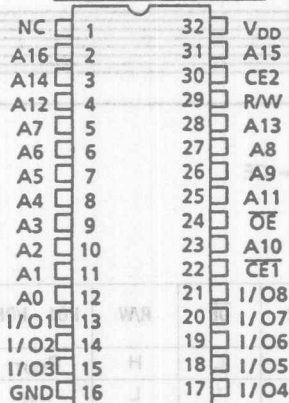
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
OE	Output Enable Input
CE1, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground
NC	No Connection

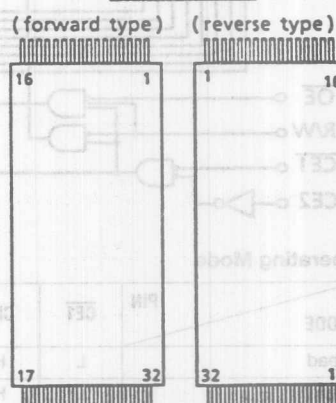
PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CE2	A ₁₅	V _{DD}	NC	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	CE1	A ₁₀	OE

Pin Connection (Top View)

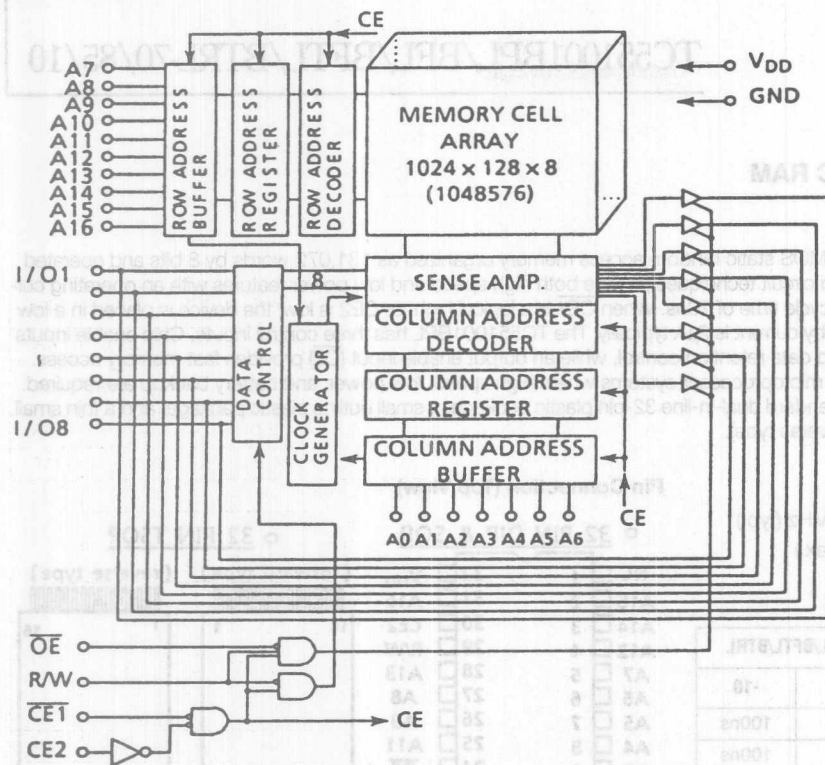
32 PIN DIP & SOP



32 PIN TSOP



Block Diagram



Operating Mode

MODE	PIN	$\overline{CE1}$	CE2	\overline{OE}	R/W	I/O1 ~ I/O8	POWER
Read		L	H	L	H	D _{OUT}	I _{DDO}
Write		L	H	*	L	D _{IN}	I _{DDO}
Output Deselect		L	H	H	H	High-Z	I _{DDO}
Standby		H	*	*	*	High-Z	I _{DDO}
		*	L	*	*	High-Z	I _{DDO}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{IO}	Input and Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V with a pulse width of 50ns

** SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	—	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

* -3.0V with a pulse width of 50ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{LO}	Output Leakage Current	CE1 = V _{IH} or CE2 = V _{IL} or R/W = V _{IL} or OE = V _{IH} , V _{OUT} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V			-1.0	—	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V			4.0	—	—	mA
I _{DDO1}	Operating Current	CE1 = V _{IL} and CE2 = V _{IH} and R/W = V _{IH} , I _{OUT} = 0mA Other Inputs = V _{IH} /V _{IL}	t _{cycle}	Min.	—	—	70	mA
				1μs	—	—	20	
I _{DDO2}		CE1 = 0.2V and CE2 = V _{DD} - 0.2V R/W = V _{DD} - 0.2V I _{OUT} = 0mA Other Inputs = V _{DD} - 0.2V/0.2V	t _{cycle}	Min.	—	—	60	
				1μs	—	—	10	
I _{DDS1}	Standby Current	CE1 = V _{IH} or CE2 = V _{IL}			—	—	3	mA
I _{DDS2} ⁽¹⁾		CE1 = V _{DD} - 0.2V or CE2 = 0.2V		Ta = 0 ~ 70°C	—	—	100	μA
		V _{DD} = 2.0V ~ 5.5V		Ta = 25°C	—	2	—	

Note (1): If $\overline{CE1} \geq V_{DD} - 0.2V$, the specified limits are guaranteed under the condition $CE2 \geq V_{DD} - 0.2V$ or $CE2 \leq 0.2V$.

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

Read Cycle

SYMBOL	PARAMETER	TC551001BPL/BFL/BFTL/BTRL							UNIT
		-70		-85		-10			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Read Cycle Time	70	—	85	—	100	—	ns	
t _{ACC}	Address Access Time	—	70	—	85	—	100		
t _{CO1}	CE1 Access Time	—	70	—	85	—	100		
t _{CO2}	CE2 Access Time	—	70	—	85	—	100		
t _{OE}	Output Enable to Output in Valid	—	35	—	45	—	50		
t _{COE}	Chip Enable (CE1, CE2) to Output in Low-Z	10	—	10	—	10	—		
t _{OEE}	Output Enable to Output in Low-Z	5	—	5	—	5	—		
t _{OD}	Chip Enable (CE1, CE2) to Output in High-Z	—	25	—	30	—	35		
t _{ODO}	Output Enable to Output in High-Z	—	25	—	30	—	35		
t _{OH}	Output Data Hold Time	10	—	10	—	10	—		

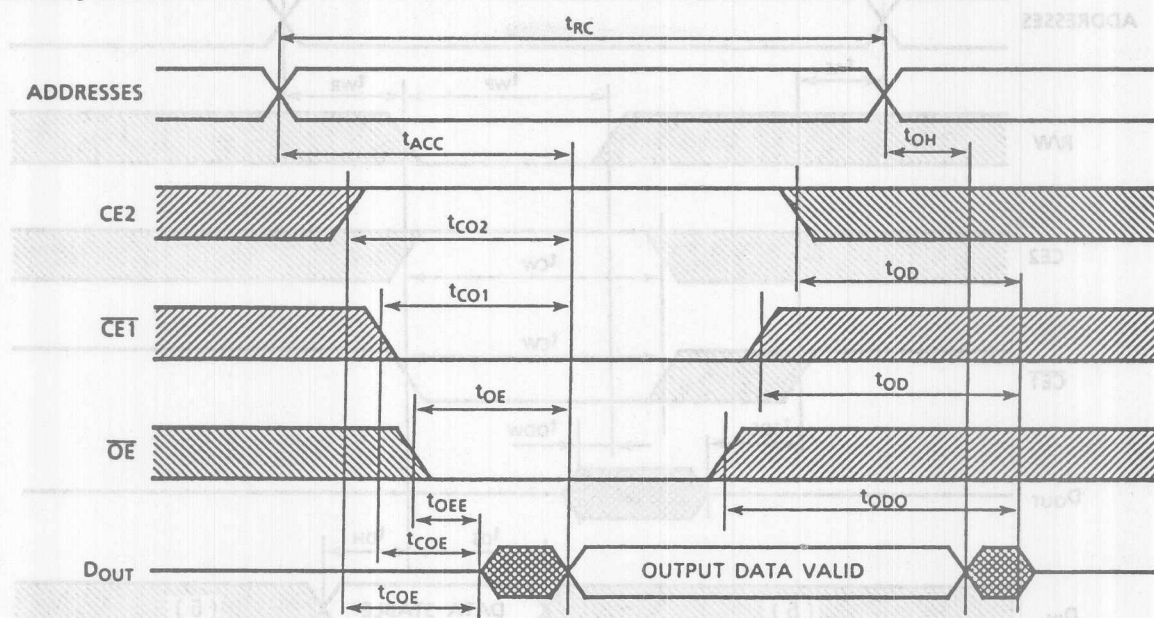
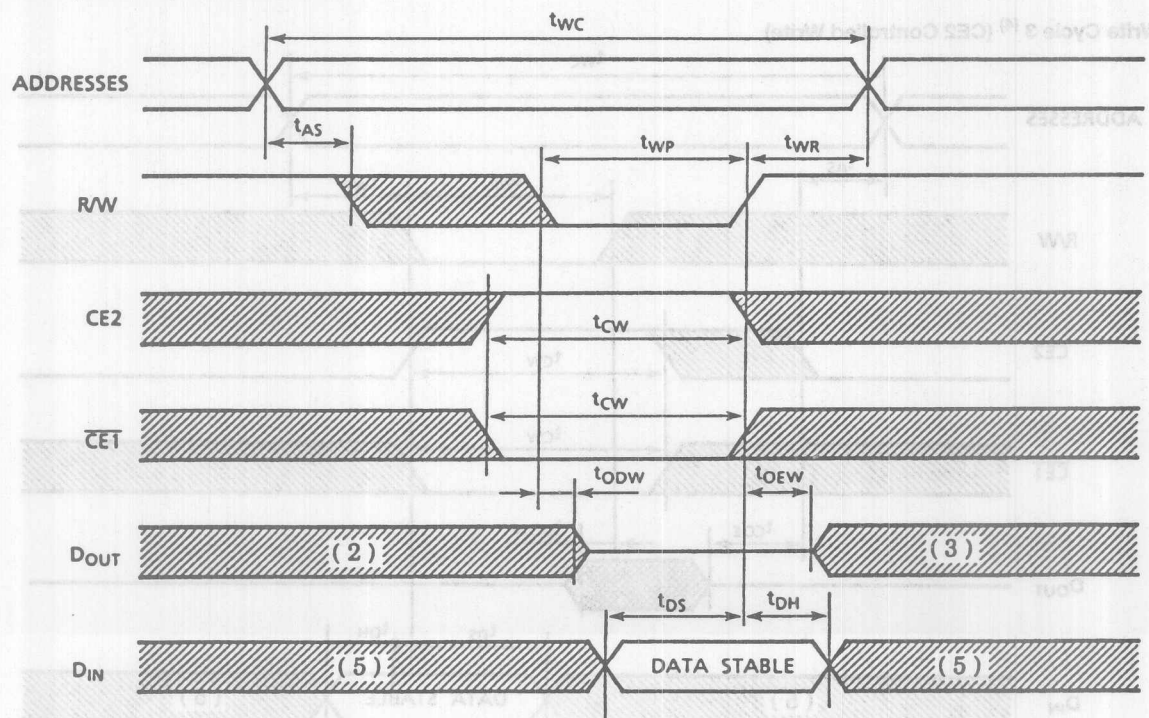
Write Cycle

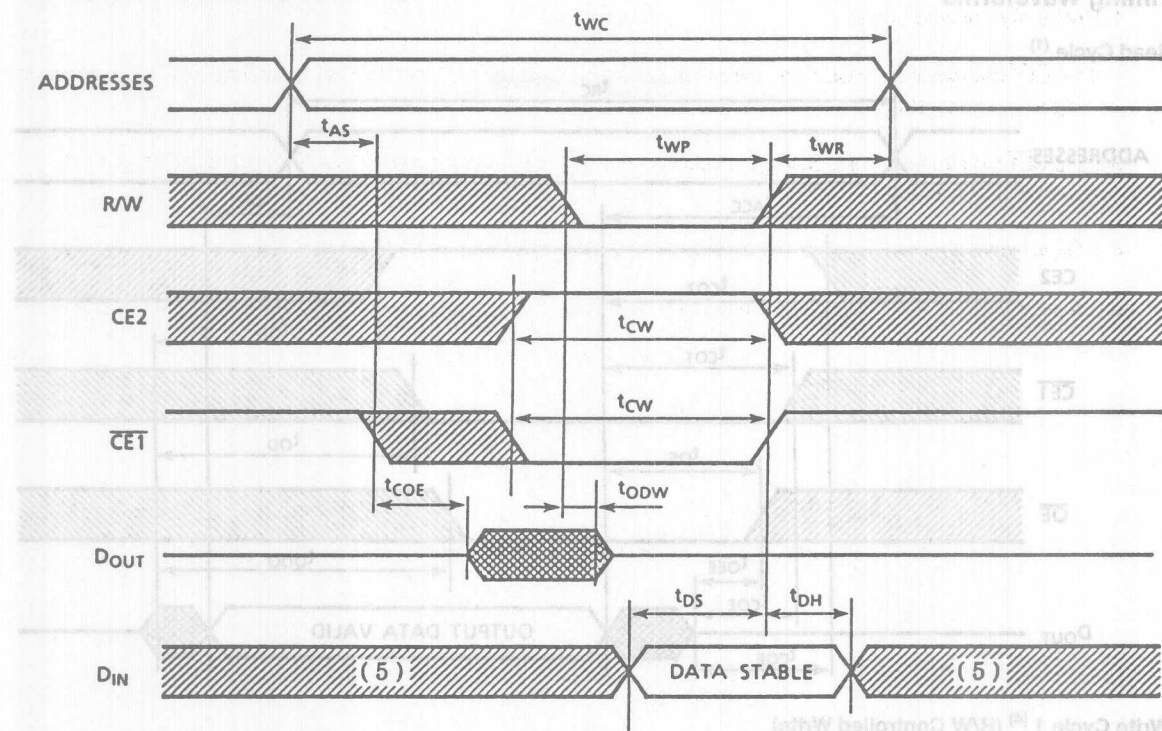
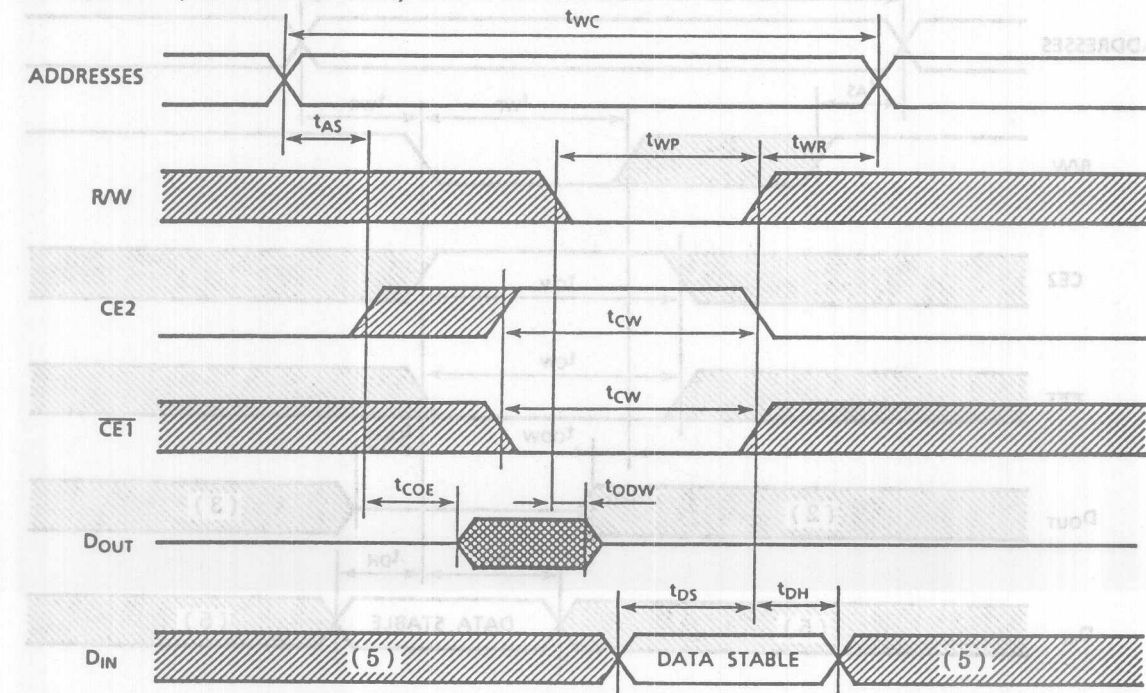
SYMBOL	PARAMETER	TC551001BPL/BFL/BFTL/BTRL						UNIT
		-70		-85		-10		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	70	—	85	—	100	—	ns
t _{WP}	Write Pulse Width	50	—	60	—	60	—	
t _{CW}	Chip Selection to End of Write	60	—	75	—	80	—	
t _{AS}	Address Setup Time	0	—	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	
t _{ODW}	R/W to Output in High-Z	—	25	—	30	—	35	
t _{OEW}	R/W to Output in Low-Z	5	—	5	—	5	—	
t _{DS}	Data Setup Time	30	—	35	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	

AC Test Conditions

Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and $C_L = 100\text{pF}$

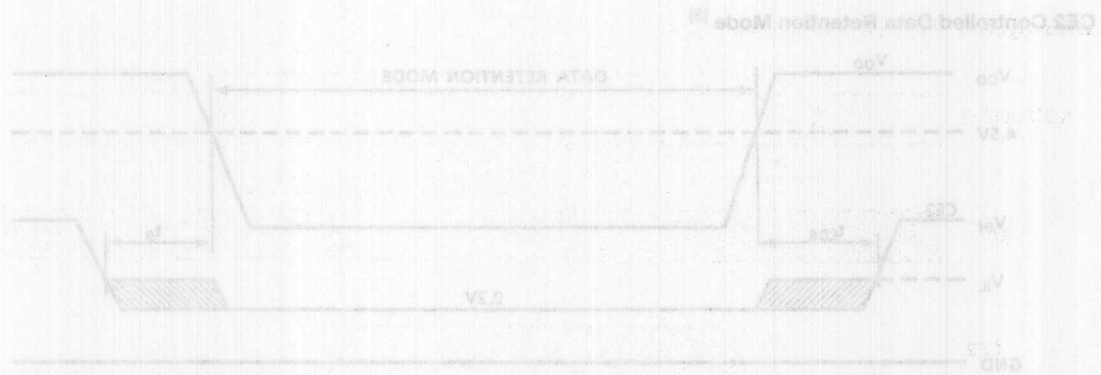
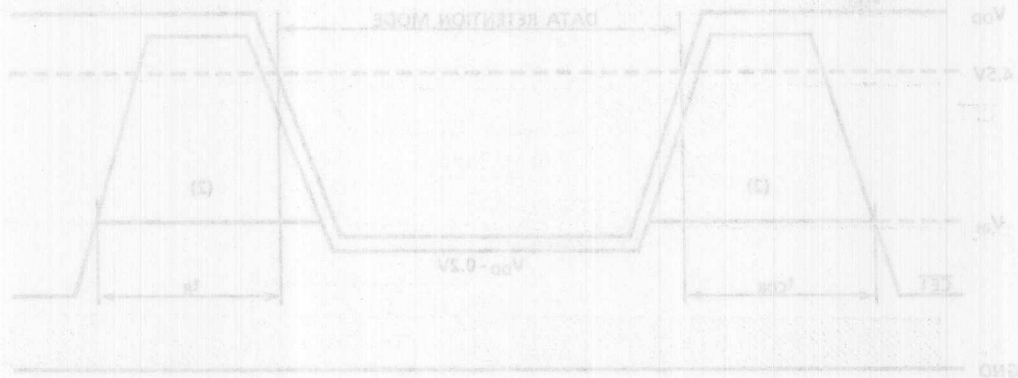
Timing Waveforms

Read Cycle ⁽¹⁾Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)

Write Cycle 2 ⁽⁴⁾ ($\overline{\text{CE1}}$ Controlled Write)Write Cycle 3 ⁽⁴⁾ (CE2 Controlled Write)

Notes:

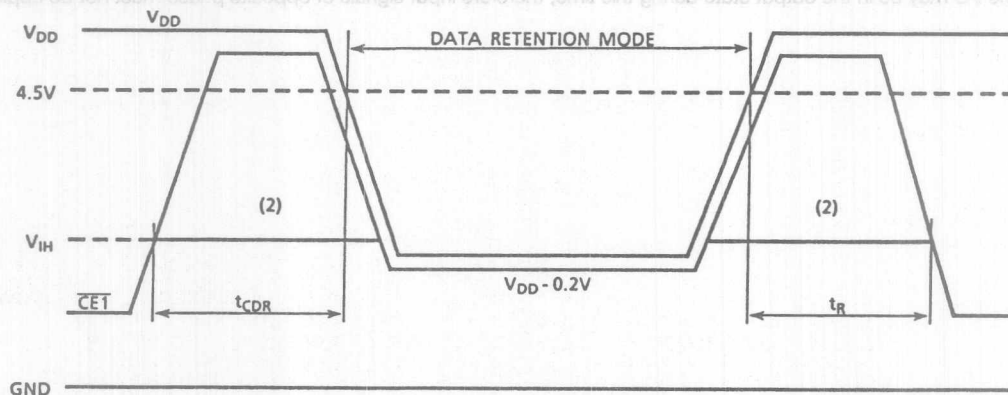
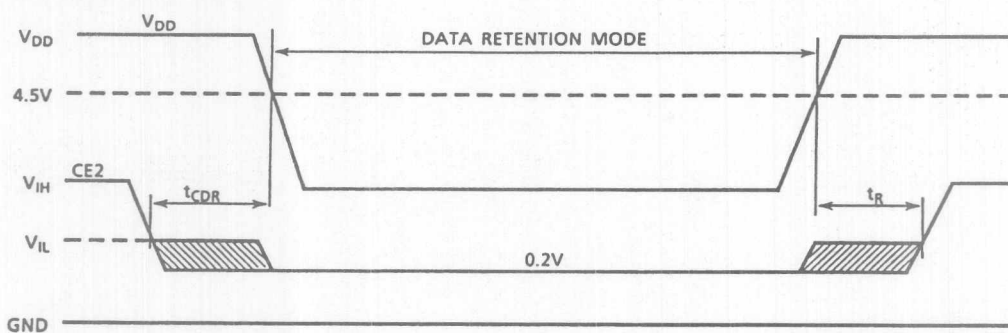
1. R/W is high for read cycles.
2. If the $\overline{CE1}$ low transition or $CE2$ high transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the $\overline{CE1}$ high transition or $CE2$ low transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.



- Notes:
1. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition $CE2 \leq 0.2V$ or $CE2 \leq V_{DD} - 0.2V$.
 2. If the V_{CE1} of $\overline{CE1}$ is 2.5V in operation, during the period that the V_{DD} voltage is going down from 5V to 2.5V, I_{CC} current flows.
 3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition $CE2 \leq 0.2V$.

Data Retention Characteristics ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DDS2}	Standby Current	$V_{DH} = 3.0\text{V}$	—	50	μA
		$V_{DH} = 5.5\text{V}$	—	100	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	ns
t_R	Recovery Time	5	—	—	ms

 $\overline{\text{CE1}}$ Controlled Data Retention Mode ⁽¹⁾CE2 Controlled Data Retention Mode ⁽³⁾

Notes:

1. In the $\overline{\text{CE1}}$ controlled data retention mode, minimum standby current is achieved under the condition $\text{CE2} \leq 0.2\text{V}$ or $\text{CE2} \geq V_{DD} - 0.2\text{V}$.
2. If the V_{IH} of $\overline{\text{CE1}}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.
3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition $\text{CE2} \leq 0.2\text{V}$.

TC551001BPL/BFL/BFTL/BTRL-70L/85L/10L

SILICON GATE CMOS

131,072 WORD x 8 BIT STATIC RAM

Description

The TC551001BPL is a 1,048,576 bit CMOS static random access memory organized as 131,072 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns. When $\overline{CE1}$ is a logical high, or $\overline{CE2}$ is low, the device is placed in a low power standby mode in which the standby current is 2 μ A typically. The TC551001BPL has three control inputs. Chip enable inputs ($\overline{CE1}$, $\overline{CE2}$) allow for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. The TC551001BPL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required.

The TC551001BPL is offered in a standard dual-in-line 32-pin plastic package, a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 4 μ A (max.) at $T_a = 25^\circ\text{C}$
- Single 5V power supply
- Access time (max.)

	TC551001BPL/BFL/BFTL/BTRL		
	-70L	-85L	-10L
Access Time	70ns	85ns	100ns
$\overline{CE1}$ Access Time	70ns	85ns	100ns
$\overline{CE2}$ Access Time	70ns	85ns	100ns
\overline{OE} Access Time	35ns	45ns	50ns

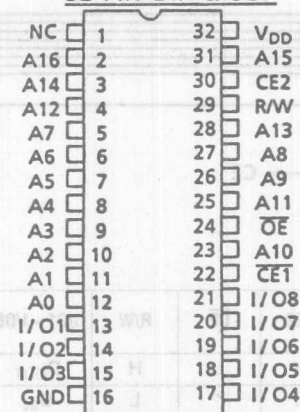
- Power down feature: $\overline{CE1}$, $\overline{CE2}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package
 - TC551001BPL : DIP32-P-600
 - TC551001BFL : SOP32-P-525
 - TC551001BFTL : TSOP32-P-0820
 - TC551001BTRL : TSOP32-P-0820A

Pin Names

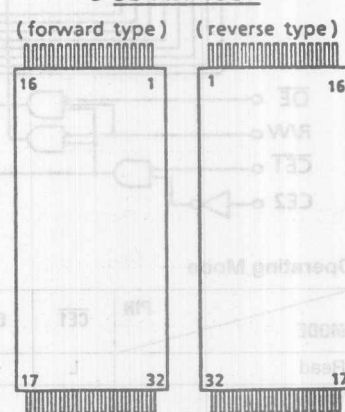
A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
$\overline{CE1}$, $\overline{CE2}$	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
NC	No Connection

Pin Connection (Top View)

32 PIN DIP & SOP

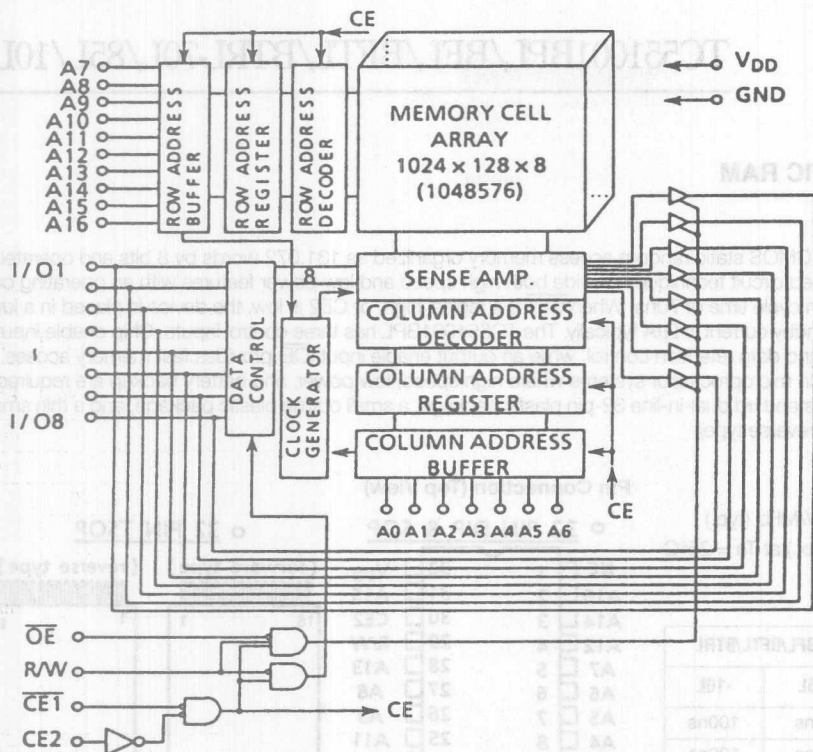


32 PIN TSOP



PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CE2	A ₁₅	V _{DD}	NC	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A ₁₀	\overline{OE}

Block Diagram



Operating Mode

MODE	PIN	CE1	CE2	OE	R/W	I/O1 ~ I/O8	POWER
Read		L	H	L	H	D _{OUT}	I _{DDO}
Write		L	H	*	L	D _{IN}	I _{DDO}
Output Deselect		L	H	H	H	High-Z	I _{DDO}
Standby		H	*	*	*	High-Z	I _{DDO}
		*	L	*	*	High-Z	I _{DDO}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{IO}	Input and Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V with a pulse width of 50ns

** SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	—	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

* -3.0V with a pulse width of 50ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER		TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current		V _{IN} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{LO}	Output Leakage Current		CE1 = V _{IH} or CE2 = V _{IL} or R/W = V _{IL} or OE = V _{IH} , V _{OUT} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{OH}	Output High Current		V _{OH} = 2.4V			-1.0	—	—	mA
I _{OL}	Output Low Current		V _{OL} = 0.4V			4.0	—	—	mA
I _{DDO1}	Operating Current		CE1 = V _{IL} and CE2 = V _{IH} and R/W = V _{IH} , I _{OUT} = 0mA Other Inputs = V _{IH} /V _{IL}	t _{cycle}	Min.	—	—	70	mA
					1μs	—	—	20	
I _{DDO2}			CE1 = 0.2V and CE2 = V _{DD} - 0.2V R/W = V _{DD} - 0.2V I _{OUT} = 0mA Other Inputs = V _{DD} - 0.2V/0.2V	t _{cycle}	Min.	—	—	60	
					1μs	—	—	10	
I _{DDS1}	Standby Current		CE1 = V _{IH} or CE2 = V _{IL}		—	—	3	mA	
I _{DDS2} ⁽¹⁾			CE1 = V _{DD} - 0.2V or CE2 = 0.2V V _{DD} = 2.0V ~ 5.5V		Ta = 0 ~ 70°C	—	—	30	μA
					Ta = 25°C	—	2	4	

Note (1): If $\overline{CE1} \geq V_{DD} - 0.2V$, the specified limits are guaranteed under the condition $CE2 \geq V_{DD} - 0.2V$ or $CE2 \leq 0.2V$.Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551001BPL/BFL/BFTL/BTRL						UNIT
		-70L		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	70	—	85	—	100	—	ns
t _{ACC}	Address Access Time	—	70	—	85	—	100	
t _{CO1}	$\overline{CE1}$ Access Time	—	70	—	85	—	100	
t _{CO2}	CE2 Access Time	—	70	—	85	—	100	
t _{OE}	Output Enable to Output in Valid	—	35	—	45	—	50	
t _{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	—	10	—	10	—	
t _{OEE}	Output Enable to Output in Low-Z	5	—	5	—	5	—	
t _{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	—	25	—	30	—	35	
t _{ODO}	Output Enable to Output in High-Z	—	25	—	30	—	35	
t _{OH}	Output Data Hold Time	10	—	10	—	10	—	

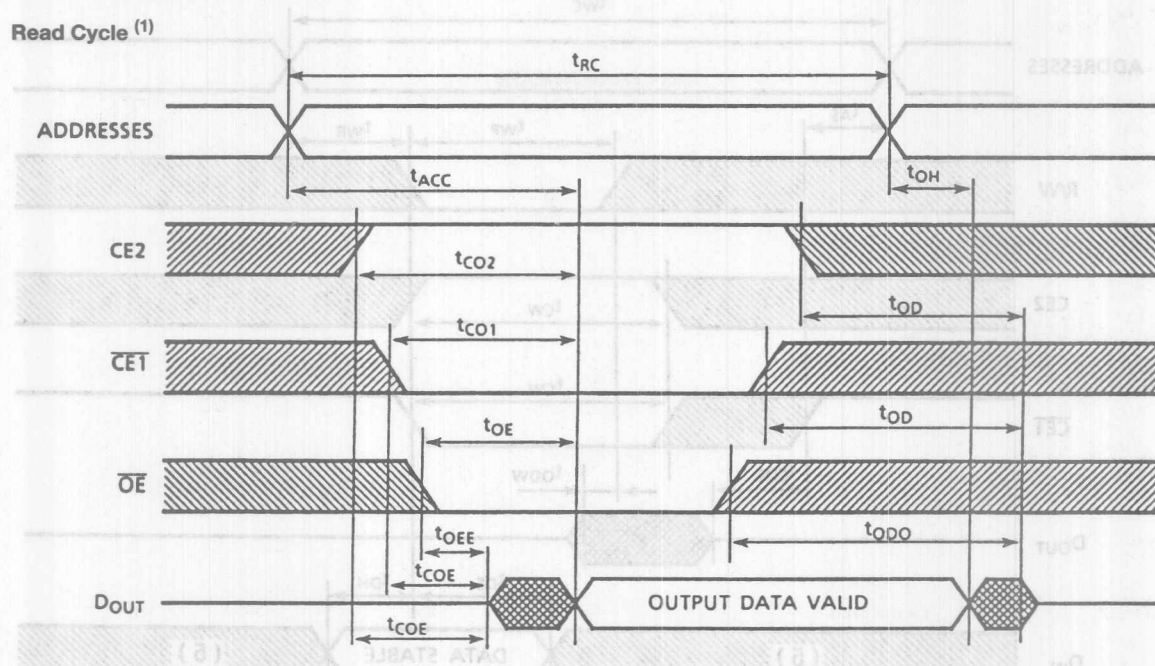
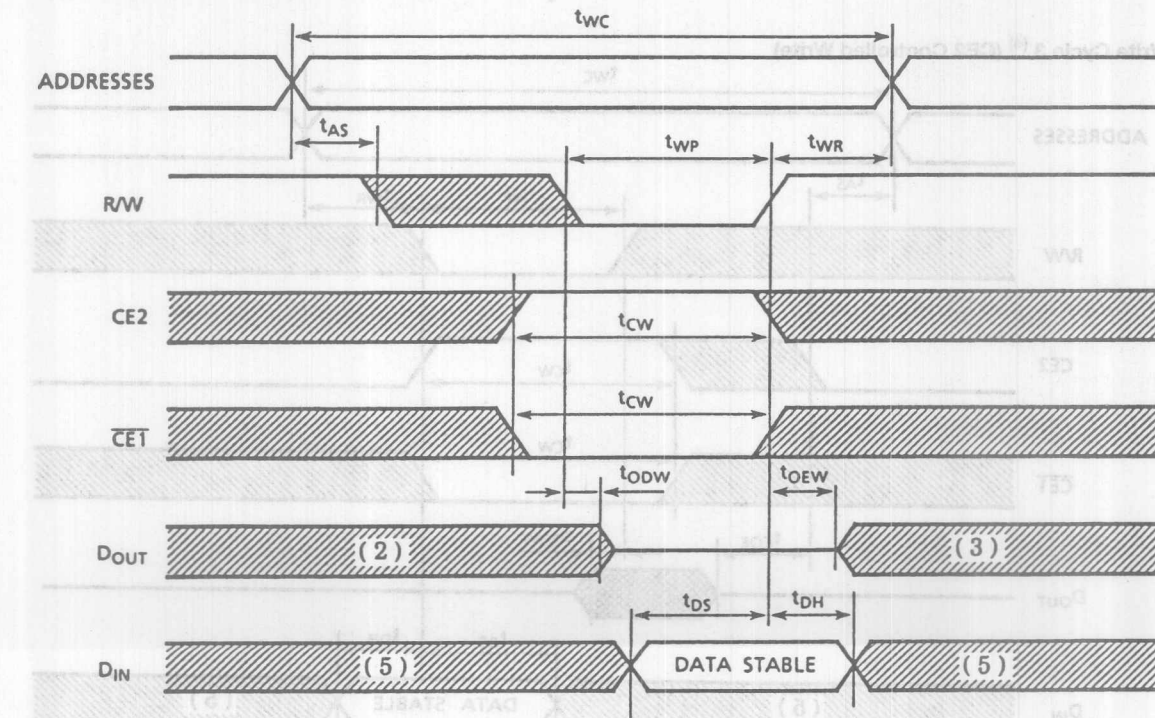
Write Cycle

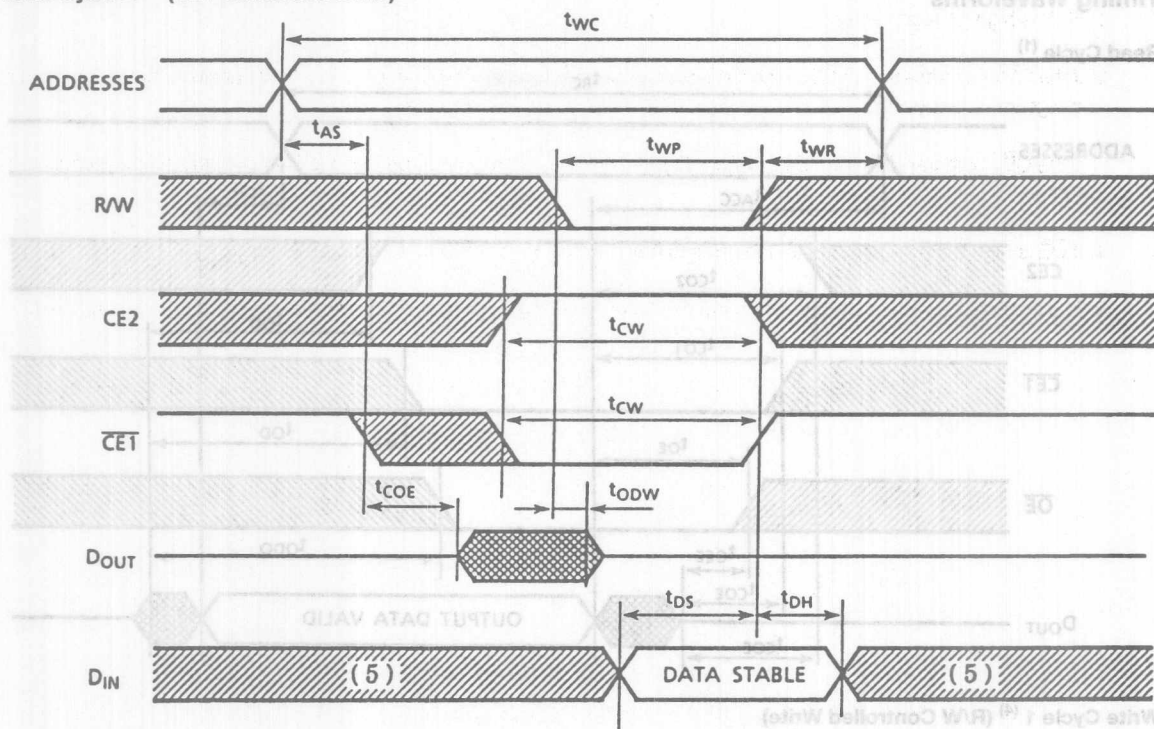
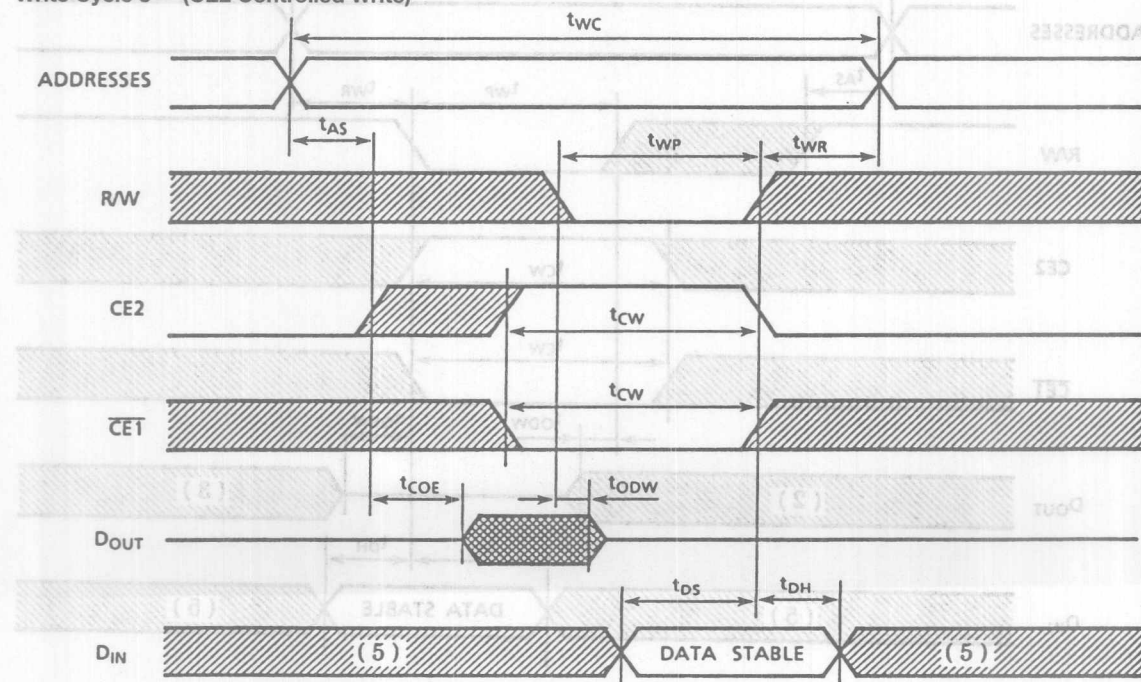
SYMBOL	PARAMETER	TC551001BPL/BFL/BFTL/BTRL						UNIT
		-70L		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	70	—	85	—	100	—	ns
t _{WP}	Write Pulse Width	50	—	60	—	60	—	
t _{CW}	Chip Selection to End of Write	60	—	75	—	80	—	
t _{AS}	Address Setup Time	0	—	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	
t _{ODW}	R/W to Output in High-Z	—	25	—	30	—	35	
t _{OEW}	R/W to Output in Low-Z	5	—	5	—	5	—	
t _{DS}	Data Setup Time	30	—	35	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	

AC Test Conditions

Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and C _L = 100pF

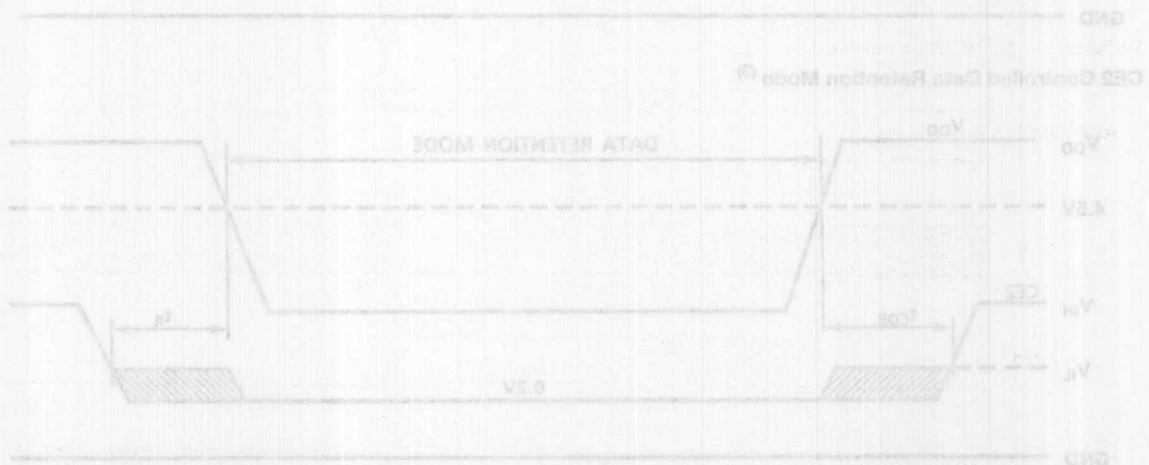
Timing Waveforms

Read Cycle ⁽¹⁾Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)

Write Cycle 2 ⁽⁴⁾ ($\overline{\text{CE1}}$ Controlled Write)Write Cycle 3 ⁽⁴⁾ (CE2 Controlled Write)

Notes:

1. R/W is high for read cycles.
2. If the $\overline{\text{CE1}}$ low transition or CE2 high transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the $\overline{\text{CE1}}$ high transition or CE2 low transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If $\overline{\text{OE}}$ is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.

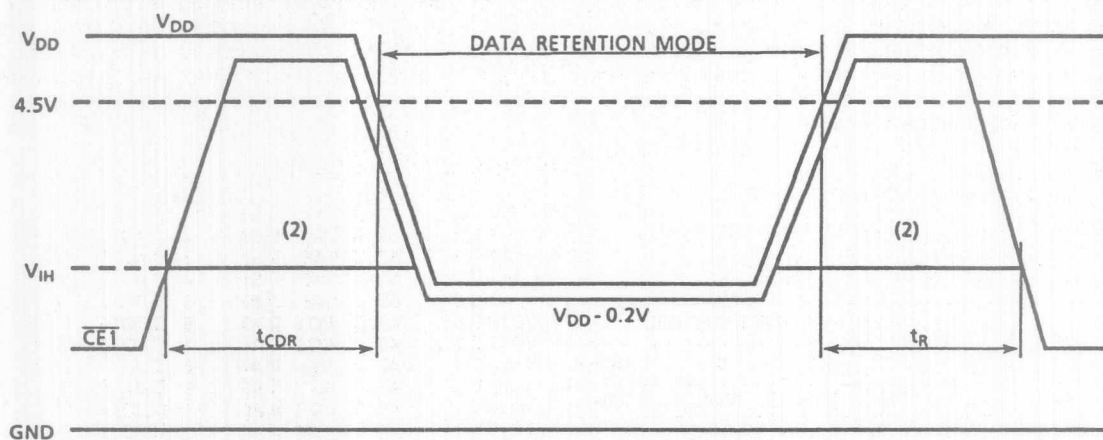
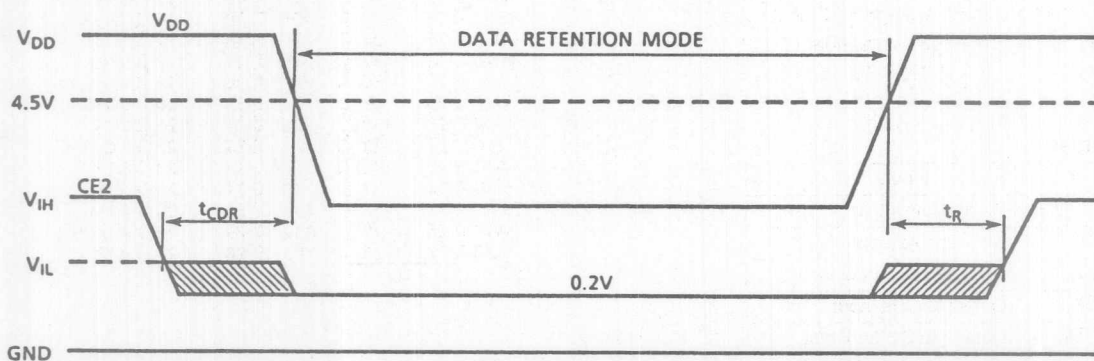


Notes:

1. In the CE1 controlled data retention mode, minimum standby current is achieved under the condition $\text{CE2} \leq 0.3\text{V}$ or $\text{CE2} = V_{\text{DD}} - 0.3\text{V}$.
2. If the V_{IL} or CE1 is 2.5V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.5V, pass current flows.
3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition $\text{CE2} \leq 0.3\text{V}$.

Data Retention Characteristics ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DDS2}	Standby Current	$V_{DH} = 3.0\text{V}$	—	15*	μA
		$V_{DH} = 5.5\text{V}$	—	30	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	ns
t_R	Recovery Time	5	—	—	ms

*3 μA (max.) $T_a = 0 \sim 40^\circ\text{C}$ **CE1 Controlled Data Retention Mode ⁽¹⁾****CE2 Controlled Data Retention Mode ⁽³⁾**

Notes:

1. In the $\overline{\text{CE1}}$ controlled data retention mode, minimum standby current is achieved under the condition $\text{CE2} \leq 0.2\text{V}$ or $\text{CE2} \geq V_{DD} - 0.2\text{V}$.
2. If the V_{IH} of $\overline{\text{CE1}}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.
3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition $\text{CE2} \leq 0.2\text{V}$.

TC554161FTL/TRL-70/85/10

SILICON GATE CMOS

PRELIMINARY

262,144 WORD x 16 BIT STATIC RAM

Description

The TC554161FTL/TRL is a 4,194,304 bit CMOS static random access memory organized as 262,144 words by 16 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 10mA/MHz (typ.) and a minimum cycle time of 70ns. When \overline{CE} is a logical high, the device is placed in a low power standby mode in which the standby current is 100 μ A (max.). The TC554161FTL/TRL has two control inputs. A chip enable input (\overline{CE}) allows for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. Byte access is supported by upper and lower byte controls. The TC554161FTL/TRL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required. The TC554161FTL/TRL is offered in a 54-pin thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 55mW/MHz (typ.)
- Standby current: 100 μ A (max.)
- Single 5V power supply
- Access time (max.)

	TC554161FTL/TRL		
	-70	-85	-10
Access Time	70ns	85ns	100ns
\overline{CE} Access Time	70ns	85ns	100ns
\overline{OE} Access Time	35ns	45ns	50ns

- Power down feature: \overline{CE}
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package TC554161FTL : TSOP54-P-400
TC554161TRL : TSOP54-P-400A

Pin Names

A0 ~ A17	Address Inputs
I/O1 ~ I/O16	Data Input/Output
\overline{CE}	Chip Enable Input
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
\overline{LB} , \overline{UB}	Data Byte Control Input
V _{DD}	Power (+5V)
GND	Ground
NC	No Connection

Pin Connection (Top View)

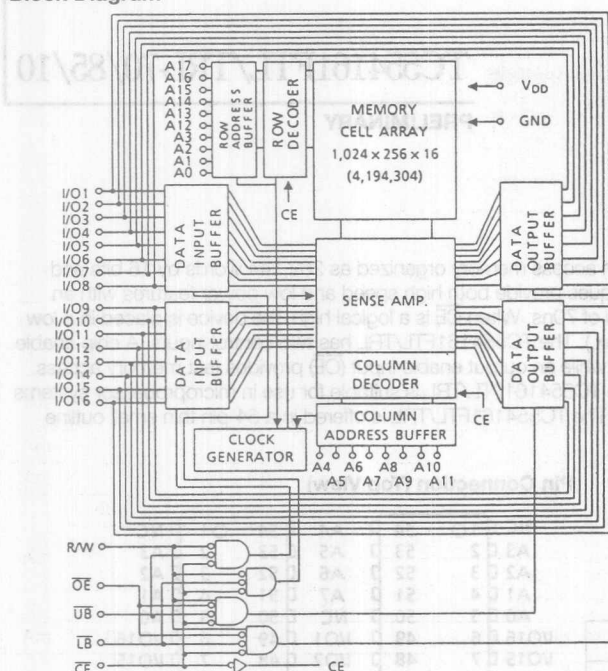
NC	1	54	A4	54	1	NC
A3	2	53	A5	53	2	A3
A2	3	52	A6	52	3	A2
A1	4	51	A7	51	4	A1
A0	5	50	NC	50	5	A0
I/O16	6	49	I/O1	49	6	I/O16
I/O15	7	48	I/O2	48	7	I/O15
V _{CC}	8	47	V _{CC}	47	8	V _{CC}
GND	9	46	GND	46	9	GND
I/O14	10	45	I/O3	45	10	I/O14
I/O13	11	44	I/O4	44	11	I/O13
\overline{UB}	12	43	\overline{LB}	43	12	\overline{UB}
\overline{CE}	13	42	\overline{OE}	42	13	\overline{CE}
NC	14	41	NC	41	14	NC
R/W	15	40	NC	40	15	R/W
I/O12	16	39	I/O5	39	16	I/O12
I/O11	17	38	I/O6	38	17	I/O11
GND	18	37	GND	37	18	GND
V _{CC}	19	36	V _{CC}	36	19	V _{CC}
I/O10	20	35	I/O7	35	20	I/O10
I/O9	21	34	I/O8	34	21	I/O9
NC	22	33	A8	33	22	NC
A17	23	32	A9	32	23	A17
A16	24	31	A10	31	24	A16
A15	25	30	A11	30	25	A15
A14	26	29	A12	29	26	A14
A13	27	28	NC	28	27	A13

FTL

TRL

UNIT	RATING	ITEM	SYMBOL
V	-0.3 ~ 7.0	Power Supply Voltage	V _{CC}
V	-0.3 ~ 7.0	Input Voltage	V _I
V	-0.3 ~ V _{CC} + 0.5	Input and Output Voltage	V _O
W	0.8	Power Dissipation	P _D
sec	100 ~ 10	Storage Temperature * Time	T _{STG}
°C	-55 ~ 120	Storage Temperature	T _{STG}
°C	0 ~ 70	Operating Temperature	T _{OP}

Block Diagram



Operating Mode

MODE	PIN	CE	OE	R/W	LB	UB	I/O1 ~ I/O8	I/O9 ~ I/O16	POWER
Read		L	L	H	L	L	Output	Output	I_{DDO}
					H	L	High Impedance	Output	I_{DDO}
					L	H	Output	High Impedance	I_{DDO}
Write		L	*	L	L	L	Input	Input	I_{DDO}
					H	L	High Impedance	Input	I_{DDO}
					L	H	Input	High Impedance	I_{DDO}
Output Deselect		L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
		L	*	*	H	H	High Impedance	High Impedance	I_{DDO}
Standby		H	*	*	*	*	High Impedance	High Impedance	I_{DDO}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
V_{IO}	Input and Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	0.6	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V with a pulse width of 30ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	—	V _{DD} + 0.3	
V _{IL}	Input Low Voltage	-0.3*	—	0.8	
V _{DH}	Data Retention Supply Voltage	2.0	—	5.5	

* -3.0V with a pulse width of 30ns

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{LO}	Output Leakage Current	CE = V _{IH} or R/W = V _{IL} or OE = V _{IH} V _{OUT} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V			-1.0	—	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V			2.1	—	—	mA
I _{DDO1}	Operating Current	CE = V _{IL} , I _{OUT} = 0mA Other Inputs = V _{IH} /V _{IL}	t _{cycle}	Min.	—	—	100	mA
				1μs	—	15	—	
I _{DDO2}		CE = 0.2V, I _{OUT} = 0mA Other Inputs = V _{IH} /V _{IL}	t _{cycle}	Min.	—	—	90	
				1μs	—	10	—	
I _{DDS1}	Standby Current	CE = V _{IH} , Other Inputs = V _{IH} /V _{IL}			—	—	3	mA
I _{DDS2}		CE = V _{DD} - 0.2V V _{DD} = 2.0V ~ 5.5V			—	—	100	μA

Capacitance* (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC554161FTL/TRL							UNIT
		-70		-85		-10			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Read Cycle Time	70	—	85	—	100	—	ns	
t _{ACC}	Address Access Time	—	70	—	85	—	100		
t _{CO}	$\overline{\text{CE}}$ Access Time	—	70	—	85	—	100		
t _{OE}	$\overline{\text{OE}}$ Access Time	—	35	—	45	—	50		
t _{BA}	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Access Time	—	35	—	45	—	50		
t _{OH}	Output Data Hold Time from Address Change	10	—	10	—	10	—		
t _{COE}	Output Enable Time from $\overline{\text{CE}}$	10	—	10	—	10	—		
t _{OEE}	Output Enable Time from $\overline{\text{OE}}$	5	—	5	—	5	—		
t _{BE}	Output Enable Time from $\overline{\text{UB}}$, $\overline{\text{LB}}$	5	—	5	—	5	—		
t _{OD}	Output Disable Time from $\overline{\text{CE}}$	—	25	—	30	—	35		
t _{ODO}	Output Disable Time from $\overline{\text{OE}}$	—	25	—	30	—	35		
t _{BD}	Output Disable Time from $\overline{\text{UB}}$, $\overline{\text{LB}}$	—	25	—	30	—	35		

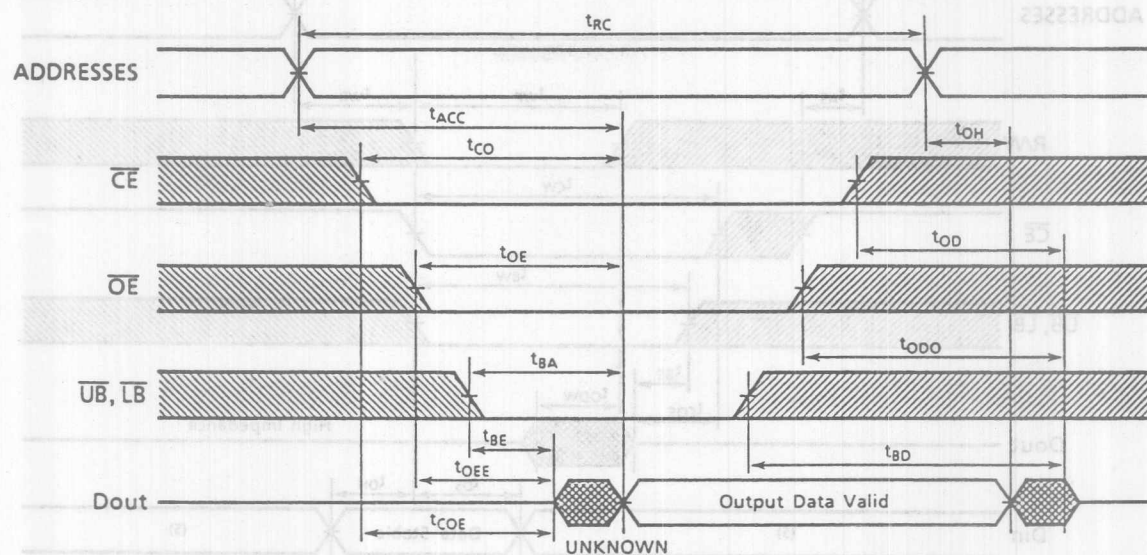
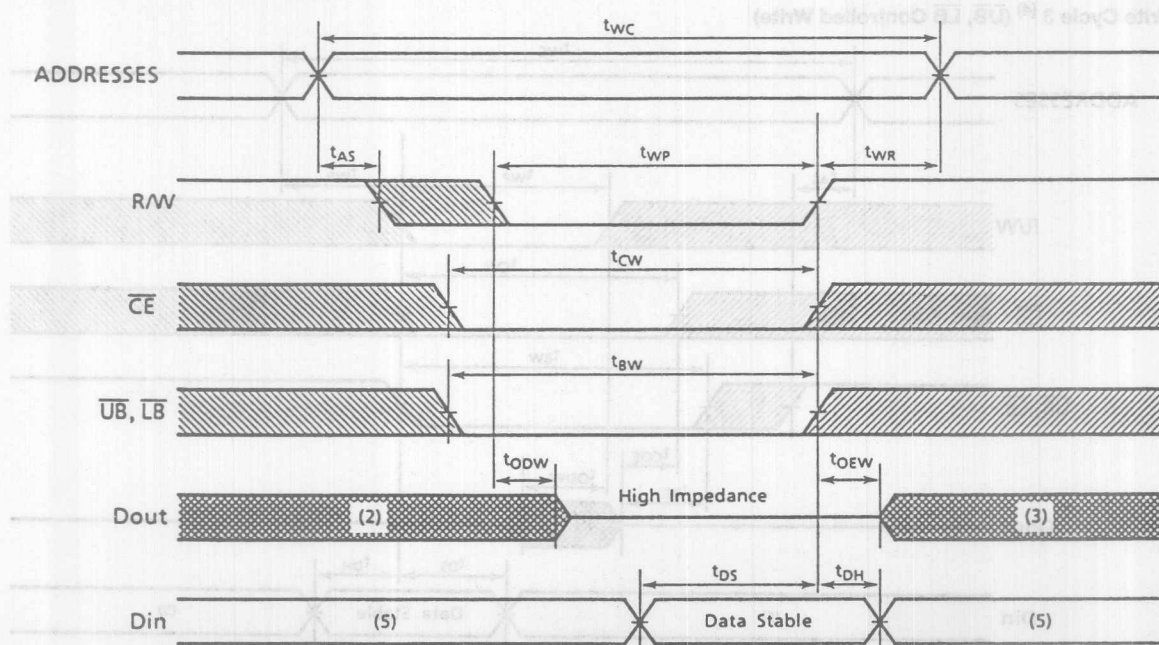
Write Cycle

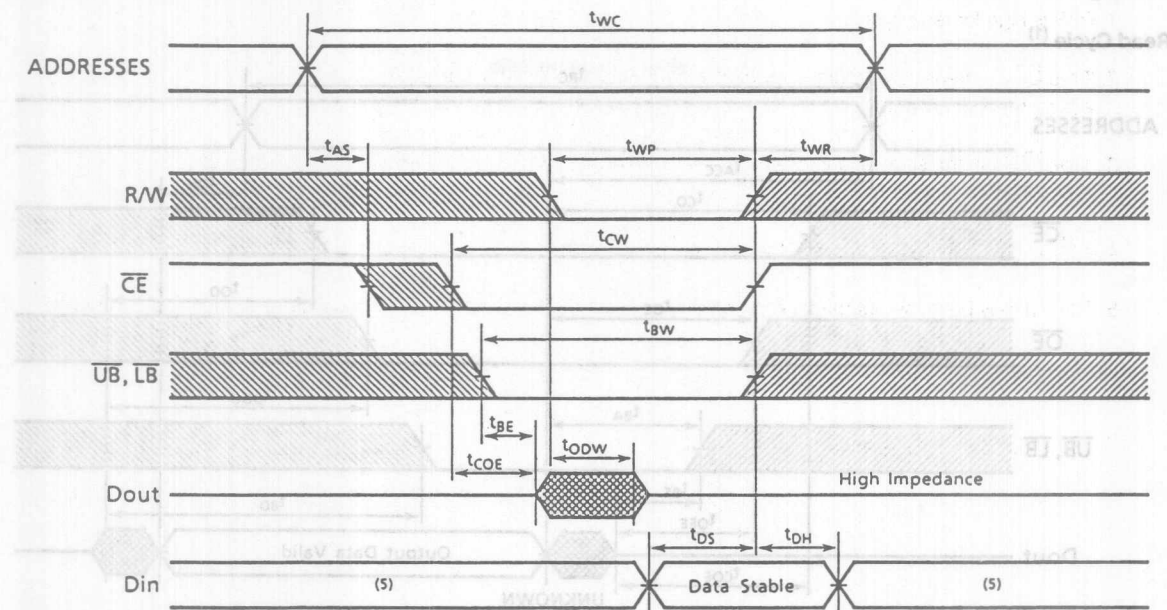
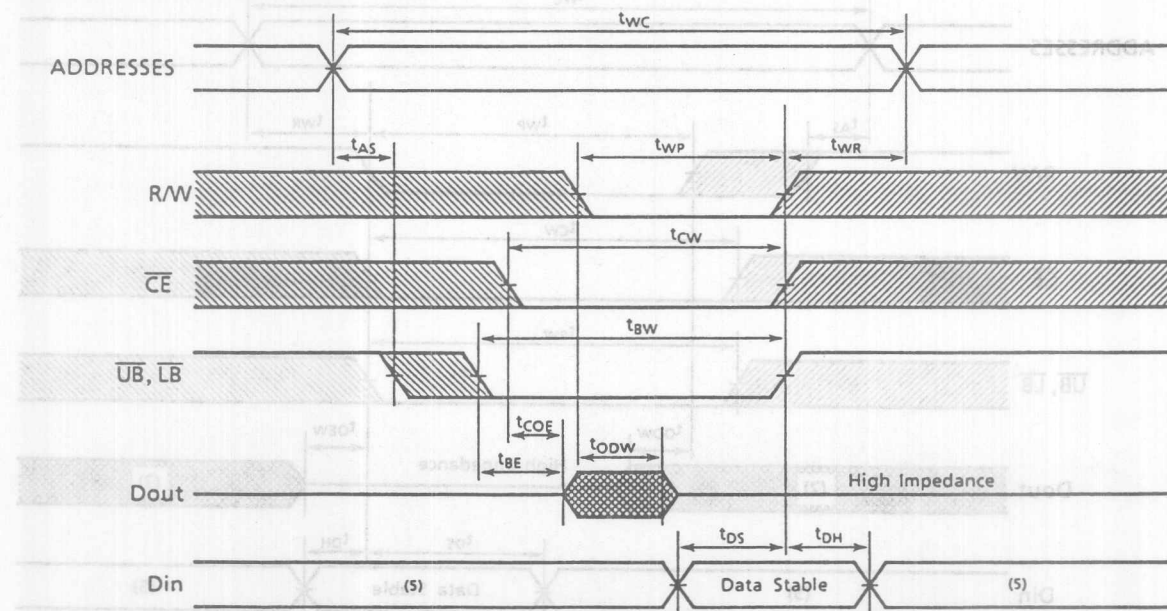
SYMBOL	PARAMETER	TC554161FTL/TRL						UNIT
		-70		-85		-10		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	70	—	85	—	100	—	ns
t _{WP}	Write Pulse Width	50	—	55	—	60	—	
t _{CW}	Chip Enable to End of Write	60	—	70	—	80	—	
t _{BW}	UB, LB Enable to End of Write	50	—	55	—	60	—	
t _{AS}	Address Setup Time	0	—	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	
t _{DS}	Data Setup Time	30	—	35	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	
t _{OEW}	Output Enable Time from R/W	5	—	5	—	5	—	
t _{ODW}	Output Disable Time from R/W	—	25	—	30	—	35	

AC Test Conditions

Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and C _L = 100pF

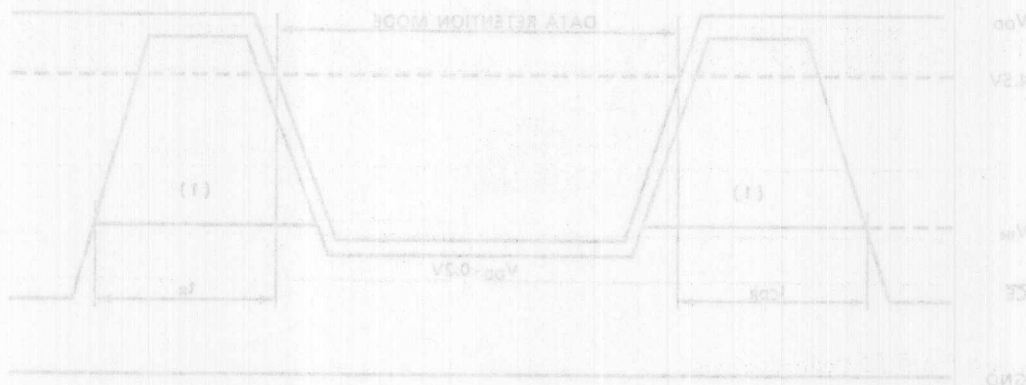
Timing Waveforms

Read Cycle ⁽¹⁾Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)

Write Cycle 2 ⁽⁴⁾ ($\overline{\text{CE}}$ Controlled Write)Write Cycle 3 ⁽⁴⁾ ($\overline{\text{UB}}, \overline{\text{LB}}$ Controlled Write)

Notes:

1. R/W is high for read cycles.
2. If the \overline{CE} low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the \overline{CE} high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.

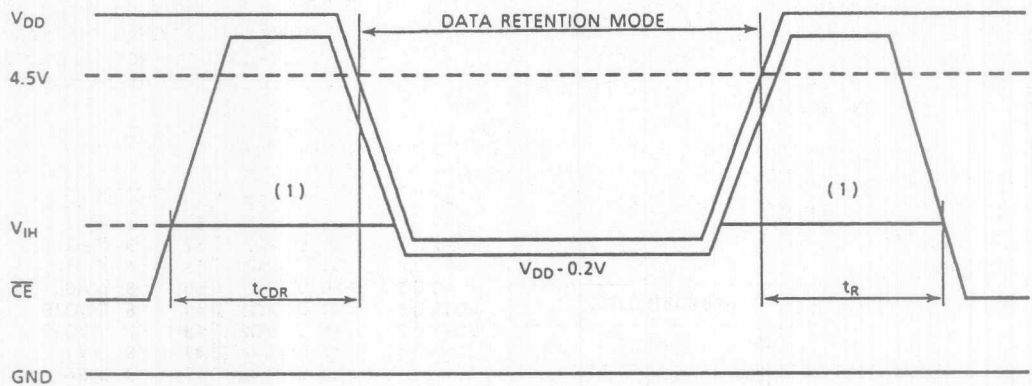


Note: If the V_{CE} to CE is 2.5V in operation, during the period the VDD is going down from 5.0V to 2.5V, I_{CC1} current flows.

Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I _{DD} S2	Standby Current	V _{DH} = 3.0V	—	50	μA
		V _{DH} = 5.5V	—	100	
t _{CDR}	Chip Deselect to Data Retention Mode	0	—	—	ns
t _R	Recovery Time	5	—	—	ms

\overline{CE} Controlled Data Retention Mode



- Note:
1. If the V_{IH} of \overline{CE} is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, $I_{DD}S1$ current flows.

TC554161FTL/TRL-70L/85L/10L

SILICON GATE CMOS

262,144 WORD x 16 BIT STATIC RAM

Description

The TC554161FTL/TRL is a 4,194,304 bit CMOS static random access memory organized as 262,144 words by 16 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 10mA/MHz (typ.) and a minimum cycle time of 70ns. When \overline{CE} is a logical high, the device is placed in a low power standby mode in which the standby current is 60 μ A (max.). The TC554161FTL/TRL has two control inputs. A chip enable input (\overline{CE}) allows for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. Byte access is supported by upper and lower byte controls. The TC554161FTL/TRL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required. The TC554161FTL/TRL is offered in a 54-pin thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 55mW/MHz (typ.)
- Standby current: 8 μ A (max.) at $T_a = 25^\circ\text{C}$
- Single 5V power supply
- Access time (max.)

	TC554161FTL/TRL		
	-70L	-85L	-10L
Access Time	70ns	85ns	100ns
\overline{CE} Access Time	70ns	85ns	100ns
\overline{OE} Access Time	35ns	45ns	50ns

- Power down feature: \overline{CE}
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package TC554161FTL : TSOP54-P-400
TC554161TRL : TSOP54-P-400A

Pin Names

A0 ~ A17	Address Inputs
I/O1 ~ I/O16	Data Input/Output
\overline{CE}	Chip Enable Input
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
LB, UB	Data Byte Control Input
V _{DD}	Power (+5V)
GND	Ground
NC	No Connection

Pin Connection (Top View)

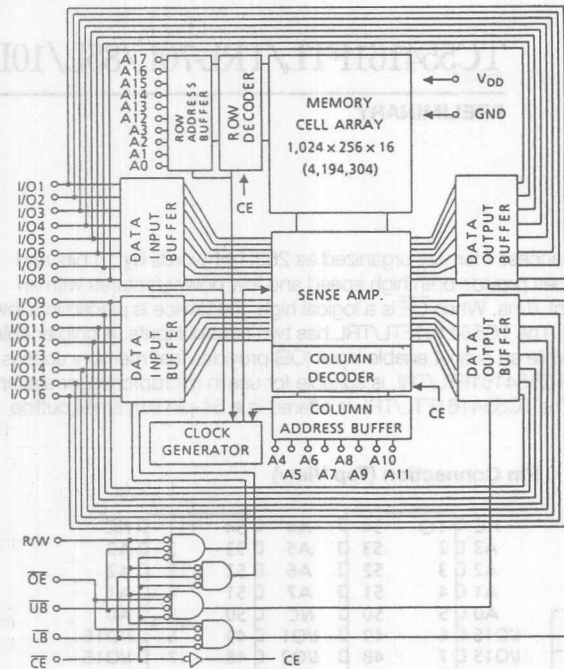
NC	1	54	A4	54	1	NC
A3	2	53	A5	53	2	A3
A2	3	52	A6	52	3	A2
A1	4	51	A7	51	4	A1
A0	5	50	NC	50	5	A0
I/O16	6	49	I/O1	49	6	I/O16
I/O15	7	48	I/O2	48	7	I/O15
V _{CC}	8	47	V _{CC}	47	8	V _{CC}
GND	9	46	GND	46	9	GND
I/O14	10	45	I/O3	45	10	I/O14
I/O13	11	44	I/O4	44	11	I/O13
UB	12	43	LB	43	12	UB
\overline{CE}	13	42	\overline{OE}	42	13	\overline{CE}
NC	14	41	NC	41	14	NC
R/W	15	40	NC	40	15	R/W
I/O12	16	39	I/O5	39	16	I/O12
I/O11	17	38	I/O6	38	17	I/O11
GND	18	37	GND	37	18	GND
V _{CC}	19	36	V _{CC}	36	19	V _{CC}
I/O10	20	35	I/O7	35	20	I/O10
I/O9	21	34	I/O8	34	21	I/O9
NC	22	33	A8	33	22	NC
A17	23	32	A9	32	23	A17
A16	24	31	A10	31	24	A16
A15	25	30	A11	30	25	A15
A14	26	29	A12	29	26	A14
A13	27	28	NC	28	27	A13

FTL

TRL

UNIT	RATING	ITEM	SYMBOL
V	-0.3 ~ 7.0	Power Supply Voltage	V _{DD}
V	-0.3 ~ 7.0	Input Voltage	V _{IN}
V	-0.3 ~ V _{DD} + 0.3	Output Voltage	V _{OUT}
W	0.8	Power Dissipation	P _D
°C	55 ~ 100	Storage Temperature	T _{STG}
°C	-55 ~ 150	Operating Temperature	T _{OP}

Block Diagram



Operating Mode

MODE	PIN	CE	OE	R/W	LB	UB	I/O1 ~ I/O8	I/O9 ~ I/O16	POWER
Read		L	L	H	L	L	Output	Output	I_{DDO}
					H	L	High Impedance	Output	I_{DDO}
					L	H	Output	High Impedance	I_{DDO}
Write		L	*	L	L	L	Input	Input	I_{DDO}
					H	L	High Impedance	Input	I_{DDO}
					L	H	Input	High Impedance	I_{DDO}
Output Deselect		L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
		L	*	*	H	H	High Impedance	High Impedance	I_{DDO}
Standby		H	*	*	*	*	High Impedance	High Impedance	I_{DDO}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
V_{IO}	Input and Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	0.6	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V with a pulse width of 30ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	—	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

* -3.0V with a pulse width of 30ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{LO}	Output Leakage Current	C _Ē = V _{IH} or R/W = V _{IL} or C _Ē = V _{IH} V _{OUT} = 0 ~ V _{DD}			—	—	±1.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V			-1.0	—	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V			2.1	—	—	mA
I _{DDO1}	Operating Current	C _Ē = V _{IL} , I _{OUT} = 0mA Other Inputs = V _{IH} /V _{IL}	t _{cycle}	Min.	—	—	100	mA
				1μs	—	15	—	
I _{DDO2}		C _Ē = 0.2V, I _{OUT} = 0mA Other Inputs = V _{IH} /V _{IL}	t _{cycle}	Min.	—	—	90	
				1μs	—	10	—	
I _{DDS1}	Standby Current	C _Ē = V _{IH} , Other Inputs = V _{IH} /V _{IL}			—	—	3	mA
I _{DDS2}		C _Ē = V _{DD} - 0.2V V _{DD} = 2.0V ~ 5.5V	Ta = 0 ~ 70°C		—	—	60	μA
			Ta = 25°C		—	4	8	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC554161FTL/TRL						UNIT
		-70L		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	70	—	85	—	100	—	ns
t _{ACC}	Address Access Time	—	70	—	85	—	100	
t _{CO}	$\overline{\text{CE}}$ Access Time	—	70	—	85	—	100	
t _{OE}	$\overline{\text{OE}}$ Access Time	—	35	—	45	—	50	
t _{BA}	$\overline{\text{UB}}, \overline{\text{LB}}$ Access Time	—	35	—	45	—	50	
t _{OH}	Output Data Hold Time from Address Change	10	—	10	—	10	—	
t _{COE}	Output Enable Time from $\overline{\text{CE}}$	10	—	10	—	10	—	
t _{OEE}	Output Enable Time from $\overline{\text{OE}}$	5	—	5	—	5	—	
t _{BE}	Output Enable Time from $\overline{\text{UB}}, \overline{\text{LB}}$	5	—	5	—	5	—	
t _{OD}	Output Disable Time from $\overline{\text{CE}}$	—	25	—	30	—	35	
t _{ODO}	Output Disable Time from $\overline{\text{OE}}$	—	25	—	30	—	35	
t _{BD}	Output Disable Time from $\overline{\text{UB}}, \overline{\text{LB}}$	—	25	—	30	—	35	

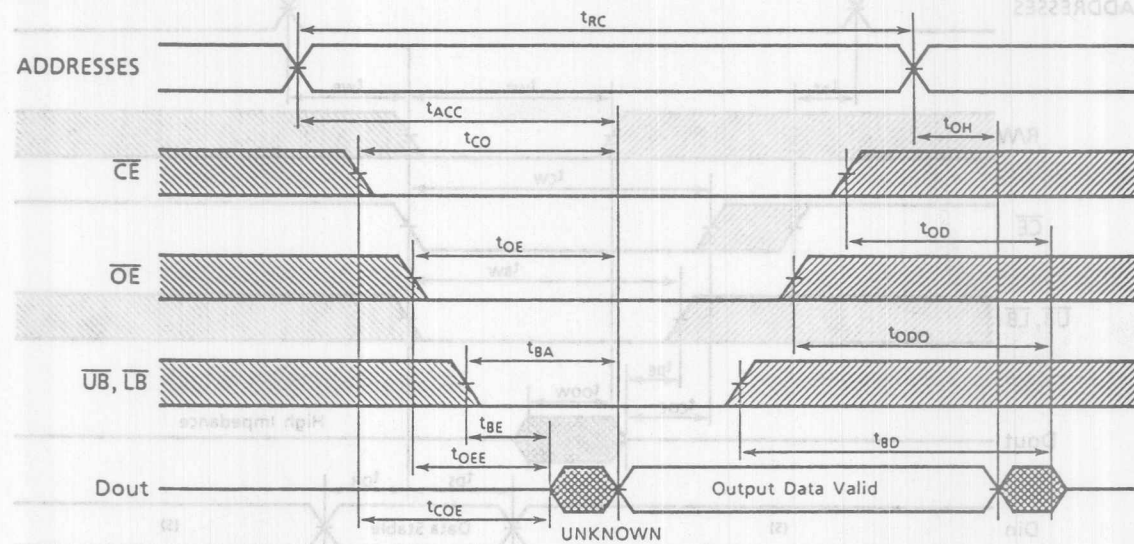
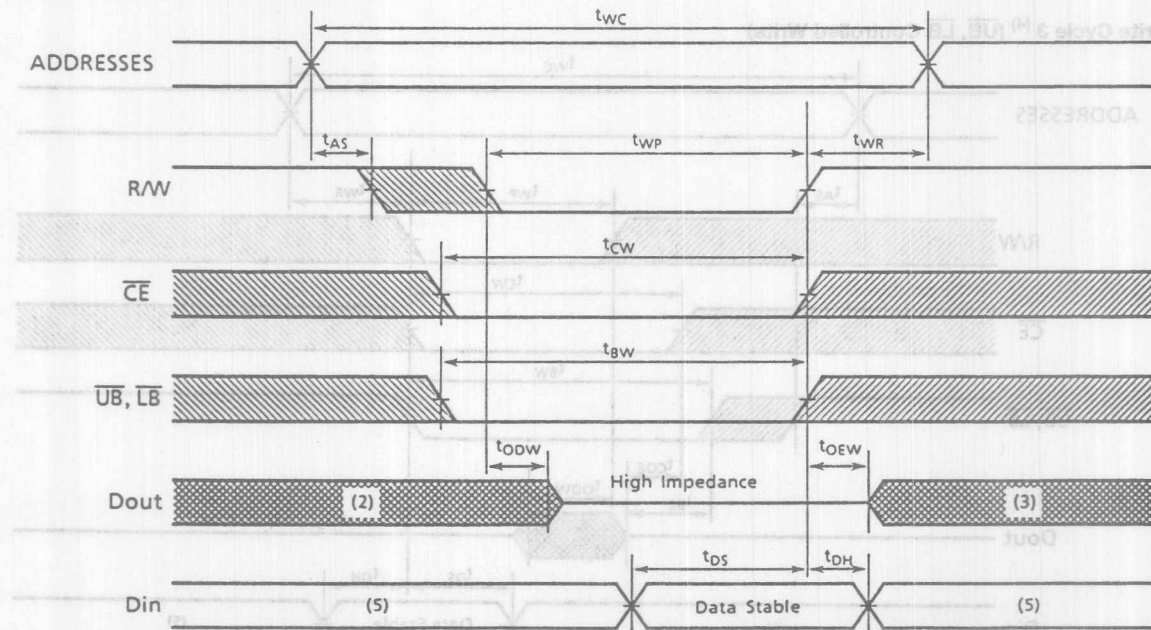
Write Cycle

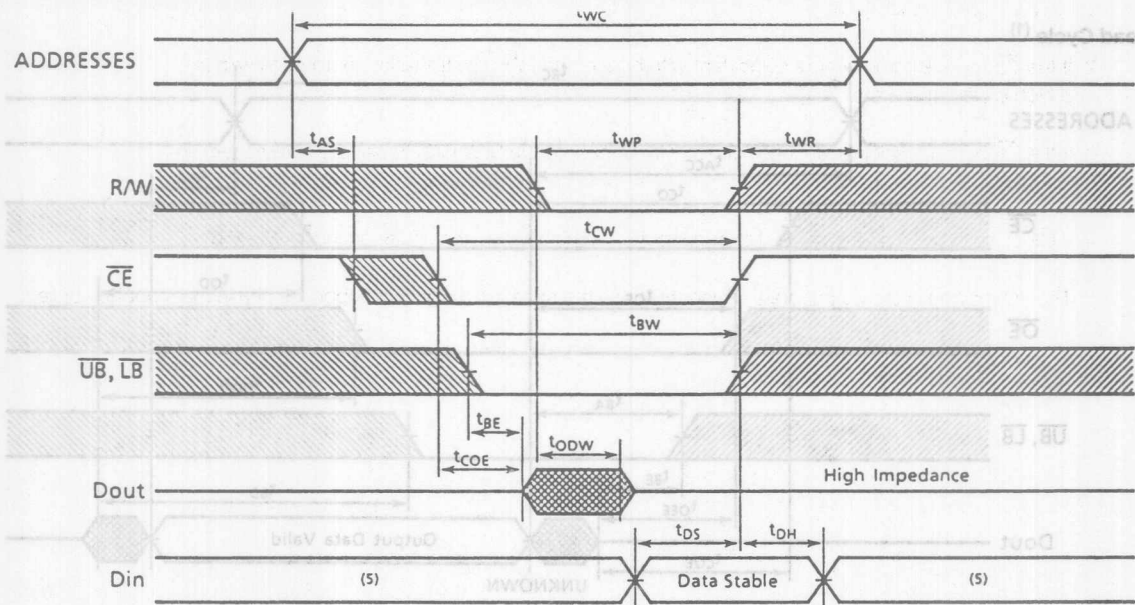
SYMBOL	PARAMETER	TC554161FTL/TRL						UNIT
		-70L		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	70	—	85	—	100	—	ns
t _{WP}	Write Pulse Width	50	—	55	—	60	—	
t _{CW}	Chip Enable to End of Write	60	—	70	—	80	—	
t _{BW}	UB, LB Enable to End of Write	50	—	55	—	60	—	
t _{AS}	Address Setup Time	0	—	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	
t _{DS}	Data Setup Time	30	—	35	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	
t _{OEW}	Output Enable Time from R/W	5	—	5	—	5	—	
t _{ODW}	Output Disable Time from R/W	—	25	—	30	—	35	

AC Test Conditions

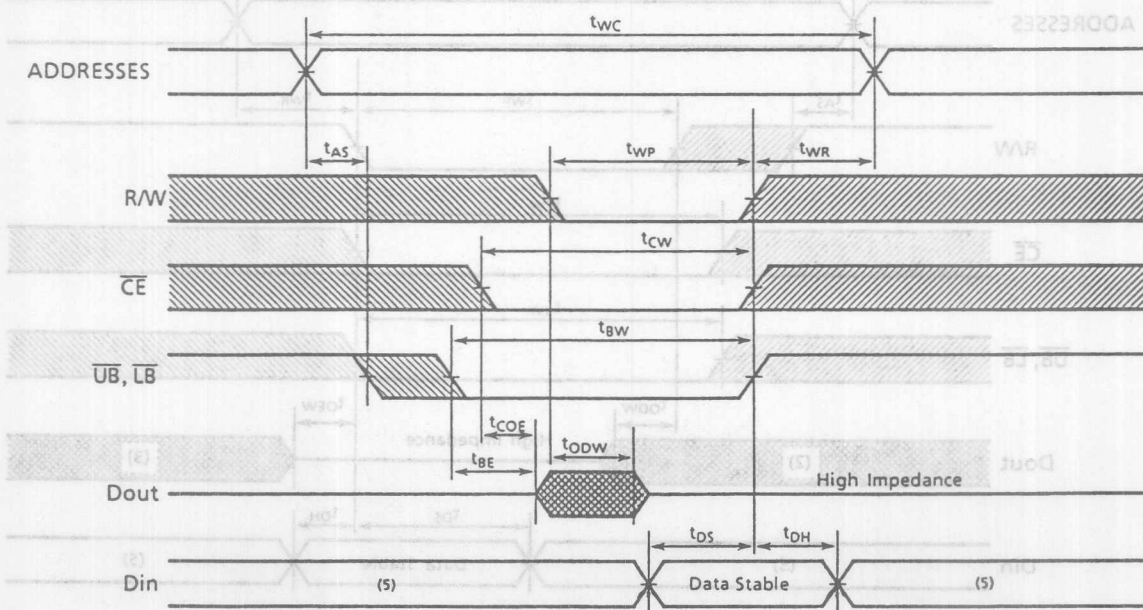
Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and C _L = 100pF

Timing Waveforms

Read Cycle ⁽¹⁾Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)

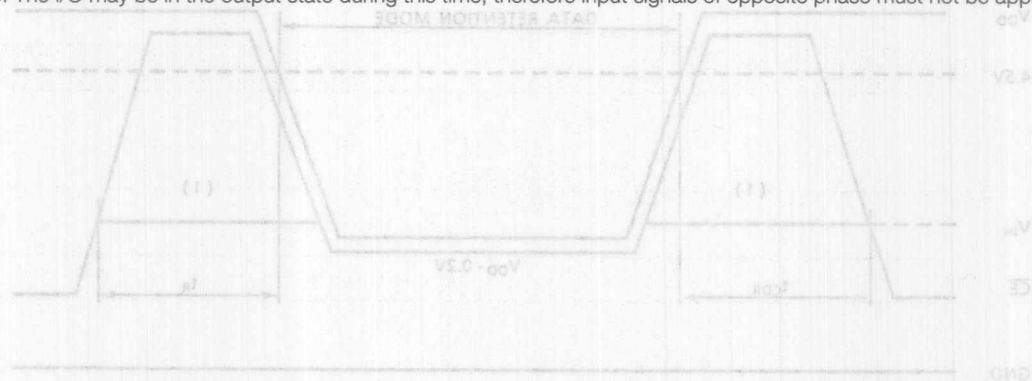


Write Cycle 3 ⁽⁴⁾ ($\overline{UB}, \overline{LB}$ Controlled Write)



Notes:

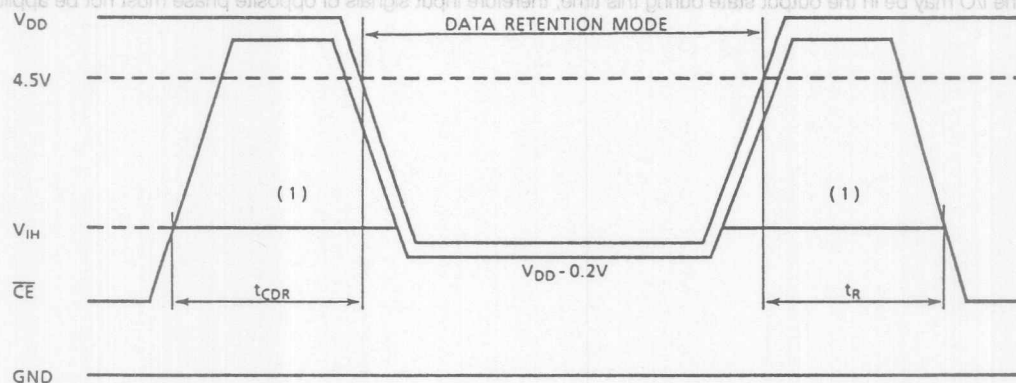
1. R/W is high for read cycles.
2. If the \overline{CE} low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the \overline{CE} high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.



Note: If the V_{DD} of \overline{CE} is 2.5V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.5V, I_{DDQ} current flows.

Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DDS2}	Standby Current	$V_{DH} = 3.0V$	—	30*	μA
		$V_{DH} = 5.5V$	—	60	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	ns
t_R	Recovery Time	5	—	—	ms

*6 μA (max.) Ta = 0 ~ 40°C **\overline{CE} Controlled Data Retention Mode**

Note:

1. If the V_{IH} of \overline{CE} is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

High Speed Static RAM

Part Number	Density	Organization	Package	Speed (ns)	Features	Page
TC56101	4M	1M x 4	P-1	20, 25, 30		B-151
TC56102	4M	4M x 1/1M x 4	P-1	20, 25, 30		B-145
TC56180	1.125M	64K x 18	P-1	10, 15, 18	3.3V Operation	B-137
TC56180	1M	64K x 18	P-1	10, 15, 18		B-129
TC56180	1M	64K x 18	P-1	10, 15, 18	3.3V Operation	B-121
TC56180	1M	128K x 8	P-1	15, 20, 25		B-115
TC56180	1M	256K x 4	P-1	15, 18, 20		B-108
TC56180	1M	512K x 2	P-1	20, 25, 30		B-102
TC56320	256K	32K x 8	P-1	15, 20, 25, 30		B-95
TC56320	256K	32K x 8	P-1	15, 20, 25, 30		B-87
TC56320	256K	32K x 8	P-1	15, 20, 25, 30	3.3V Operation	B-79
TC56320	256K	32K x 8	P-1	15, 20, 25, 30		B-73
TC56320	256K	32K x 8	P-1	15, 20, 25, 30		B-65
TC56320	256K	32K x 8	P-1	15, 20, 25, 30		B-57
TC56320	256K	32K x 8	P-1	15, 20, 25, 30		B-49
TC56320	256K	32K x 8	P-1	15, 20, 25, 30		B-41
TC56320	256K	32K x 8	P-1	15, 20, 25, 30		B-33
TC56320	256K	32K x 8	P-1	15, 20, 25, 30		B-25
TC56320	256K	32K x 8	P-1	15, 20, 25, 30		B-17
TC56320	256K	32K x 8	P-1	15, 20, 25, 30		B-9
TC56320	256K	32K x 8	P-1	15, 20, 25, 30		B-1

High Speed SRAM

Package: P = Plastic DIP, J = SOJ, FT = Forward bend TSOP

High Speed Static RAM

	Density	Organization	Package	Speed (ns)	Features	Page
TC5588	64K	8K x 8	P, J	15, 20, 25, 35		B-1
TC55B88	64K	8K x 8	P, J	10, 12		B-9
TC5589	72K	8K x 9	P, J	15, 20, 25, 35		B-17
TC55464A	256K	64K x 4	P, J	15, 20, 25, 35		B-25
TC55B464	256K	64K x 4	P, J	10, 12		B-33
TC55465A	256K	64K x 4	P, J	15, 20, 25, 35	TC55464A w/ \overline{OE}	B-41
TC55B465	256K	64K x 4	P, J	10, 12	TC55B464 w/ \overline{OE}	B-49
TC55328A	256K	32K x 8	P, J	15, 20, 25, 35		B-57
TC55B328	256K	32K x 8	P, J	10, 12		B-65
TC55V328	256K	32K x 8	J	20, 25, 35	3.3V Operation	B-73
TC55329A	288K	32K x 9	P, J	15, 20, 25, 35		B-79
TC55B329	288K	32K x 9	P, J	10, 12		B-87
TC551632	512K	32K x 16	J	20, 25, 35		B-95
TC55B4256	1M	256K x 4	J	12, 15, 20		B-103
TC55B4257	1M	256K x 4	J	12, 15, 20	TC55B4256 w/ \overline{OE}	B-109
TC55B8128	1M	128K x 8	P, J	12, 15, 20		B-115
TC551664	1M	64K x 16	J	15, 20, 25		B-121
TC55V1664	1M	64K x 16	J, FT	10, 12, 15	3.3V Operation	B-129
TC55V1864	1.125M	64K x 18	J, FT	10, 12, 15	3.3V Operation	B-137
TC551402	4M	4M x 1/1M x 4	J	20, 25, 30		B-145
TC554101	4M	1M x 4	J	20, 25, 30		B-151

Package: P = Plastic DIP, J = SOJ, FT = Forward bend TSOP

TC5588P/J-15/20/25/35

SILICON GATE CMOS

8,192 WORD x 8 BIT CMOS STATIC RAM

Description

The TC5588P/J is a 65,536 bit high speed CMOS static random access memory organized as 8,192 words by 8 bits and operated from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

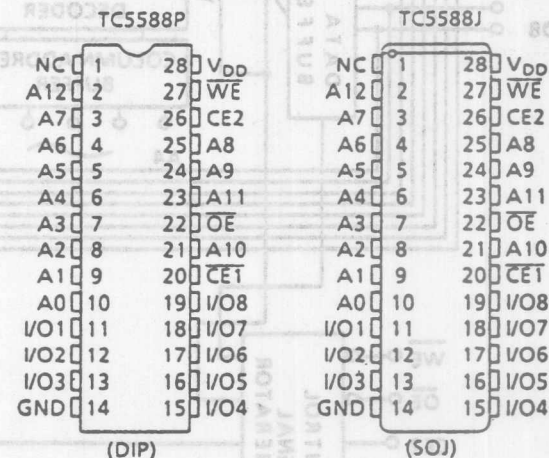
The TC5588P/J features low power dissipation when the device is deselected using chip enable (CE1, CE2) and has an output enable input (OE) for fast memory access. Also, the device power between memory accesses is reduced by an automatic power down circuit.

The TC5588P/J is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible. The TC5588P/J is available in a 300mil width, 28-pin DIP and SOJ suitable for high density surface assembly.

Features

- Fast access time
 - TC5588P/J-15 15ns (max.)
 - TC5588P/J-20 20ns (max.)
 - TC5588P/J-25 25ns (max.)
 - TC5588P/J-35 35ns (max.)
- Low power dissipation
 - Operation:
 - TC5588P/J-15 135mA (max.)
 - TC5588P/J-20 115mA (max.)
 - TC5588P/J-25 115mA (max.)
 - TC5588P/J-35 115mA (max.)
 - Standby: 1mA (max.)
- Single 5V power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Package:
 - TC5588P: DIP28-P-300B
 - TC5588J: SOJ28-P-300A

Pin Connection (Top View)

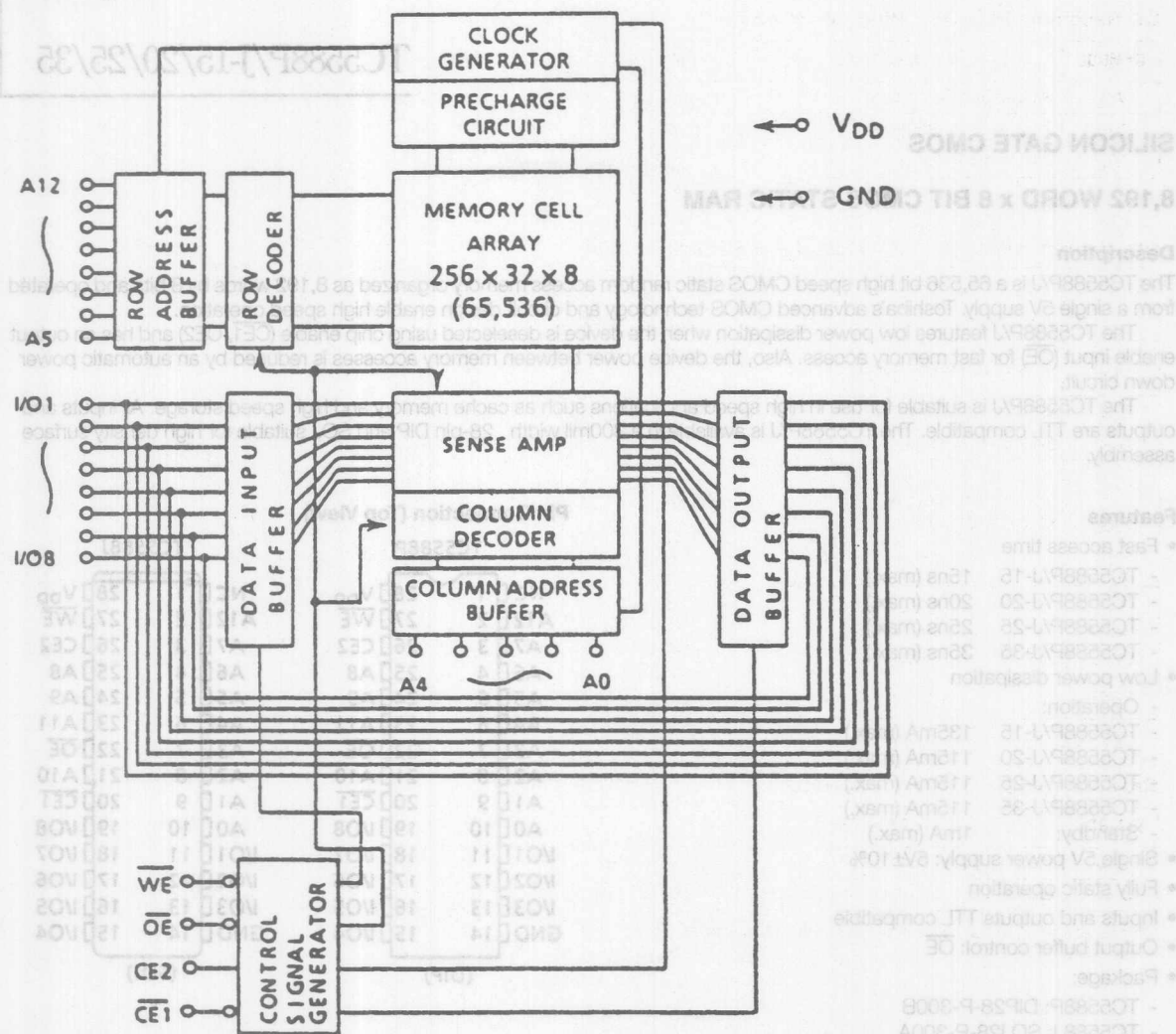


Pin Names

A0 ~ A12	Address Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
CE1, CE2	Chip Enable Inputs
WE	Write Enable Input
OE	Output Enable Input
VDD	Power (+5V)
GND	Ground
NC	No Connection

UNIT	RATING	ITEM	SYMBOL
V	-0.5 ~ 7.0	Power Supply Voltage	V _{DD}
V	-0.5 ~ 7.0	Input Voltage	V _{IN}
V	-0.5 ~ V _{DD} + 0.5	Input/Output Voltage	V _{IO}
W	1.0	Power Dissipation	P _D
°C	25 ~ 100	Operating Temperature	T _{OP}
°C	-55 ~ 150	Storage Temperature	T _{STG}
°C	-10 ~ 85	Maximum Ratings	

Block Diagram



Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0 ~ 7.0	V
V_{IO}	Input/Output Voltage	-0.5 ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

* -3V with a pulse width of 10ns

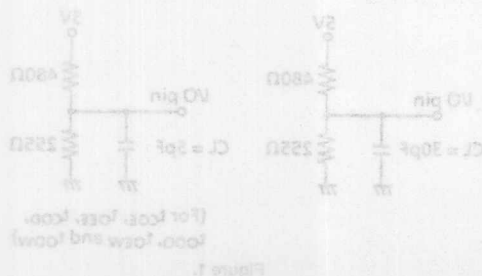
DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1	μA
I_{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	8	—	—	mA
I_{DDO}	Operating Current	$V_{DD} = 5.5V$ $t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$ Other Inputs = V_{IH}/V_{IL} $I_{OUT} = 0\text{mA}$	-15	—	135	mA
			-20	—	—	
			-25	—	115	
			-35	—	—	
I_{DD1}	Standby Current	$V_{DD} = 5.5V$ $t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ Other Inputs = V_{IH}/V_{IL}	—	—	25	mA
I_{DD2}^*		$\overline{CE1} = V_{DD} - 0.2V$ or $CE2 = 0.2V$ Other Inputs = $V_{DD} - 0.2V$ or $0.2V$	—	—	1	

* If $\overline{CE1} \geq V_{DD} - 0.2V$, the specified limits are guaranteed under the condition $CE2 \geq V_{DD} - 0.2V$ or $CE2 \leq 0.2V$.Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	7	pF

*This parameter is periodically sampled and is not 100% tested.



Output Load	Fig. 1	2.0V/0.8V	2.5V/0.8V	2.5V/0.8V	2.5V/0.8V
Output Timing Measurement Reference Levels		2.5V/0.8V	2.5V/0.8V	2.5V/0.8V	2.5V/0.8V
Input Timing Measurement Reference Levels		2.5V/0.8V	2.5V/0.8V	2.5V/0.8V	2.5V/0.8V
Input Pulse Rise and Fall Time		2ns	2ns	2ns	2ns
Input Pulse Levels		2.0V/0.8V	2.0V/0.8V	2.0V/0.8V	2.0V/0.8V

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

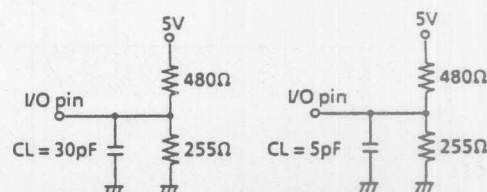
SYMBOL	PARAMETER	TC5588P/J-15		TC5588P/J-20		TC5588P/J-25		TC5588P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	
t_{ACC}	Address Access Time	—	15	—	20	—	25	—	35	
t_{CO1}	$\overline{CE}1$ Access Time	—	15	—	20	—	25	—	35	
t_{CO2}	$\overline{CE}2$ Access Time	—	15	—	20	—	25	—	35	
t_{OE}	\overline{OE} Access Time	—	9	—	10	—	12	—	12	
t_{OH}	Output Data Hold Time from Address Change	5	—	5	—	5	—	5	—	ns
t_{COE}	Output Enable Time from $\overline{CE}1$ or $\overline{CE}2$	5	—	5	—	5	—	5	—	
t_{COD}	Output Disable Time from $\overline{CE}1$ or $\overline{CE}2$	—	6	—	6	—	6	—	6	
t_{OEE}	Output Enable Time from \overline{OE}	0	—	0	—	0	—	0	—	
t_{ODO}	Output Disable Time from \overline{OE}	—	5	—	5	—	5	—	5	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	15	—	20	—	25	—	35	

Write Cycle

SYMBOL	PARAMETER	TC5588P/J-15		TC5588P/J-20		TC5588P/J-25		TC5588P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	—	20	—	25	—	35	—	
t_{CW}	Chip Enable to End of Write	12	—	13	—	15	—	15	—	
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	
t_{WP}	Write Pulse Width	12	—	13	—	15	—	15	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DS}	Data Setup Time	9	—	10	—	12	—	12	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	
t_{OEw}	Output Enable Time from \overline{WE}	0	—	0	—	0	—	0	—	
t_{ODw}	Output Disable Time from \overline{WE}	—	6	—	6	—	6	—	6	

AC Test Conditions

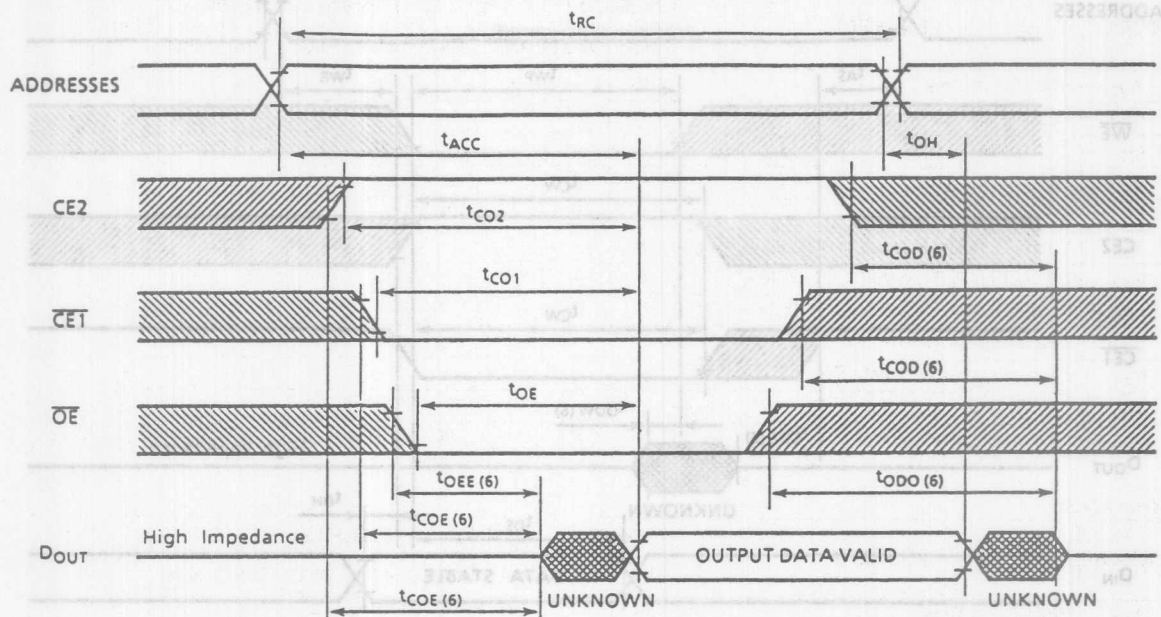
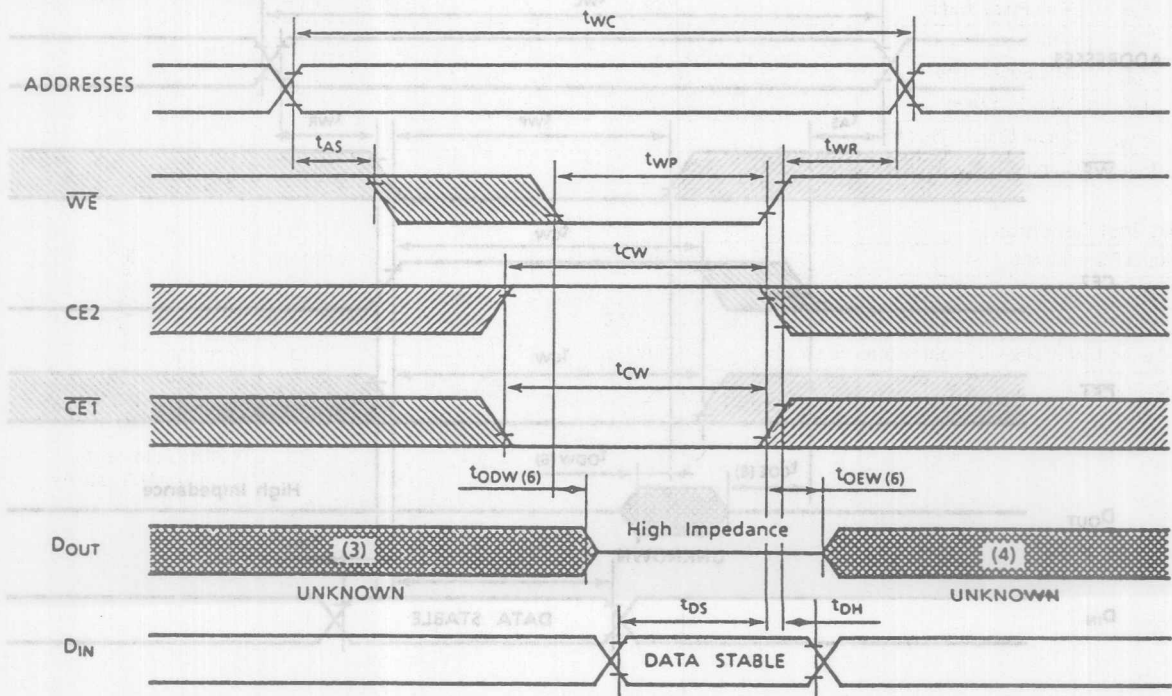
Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

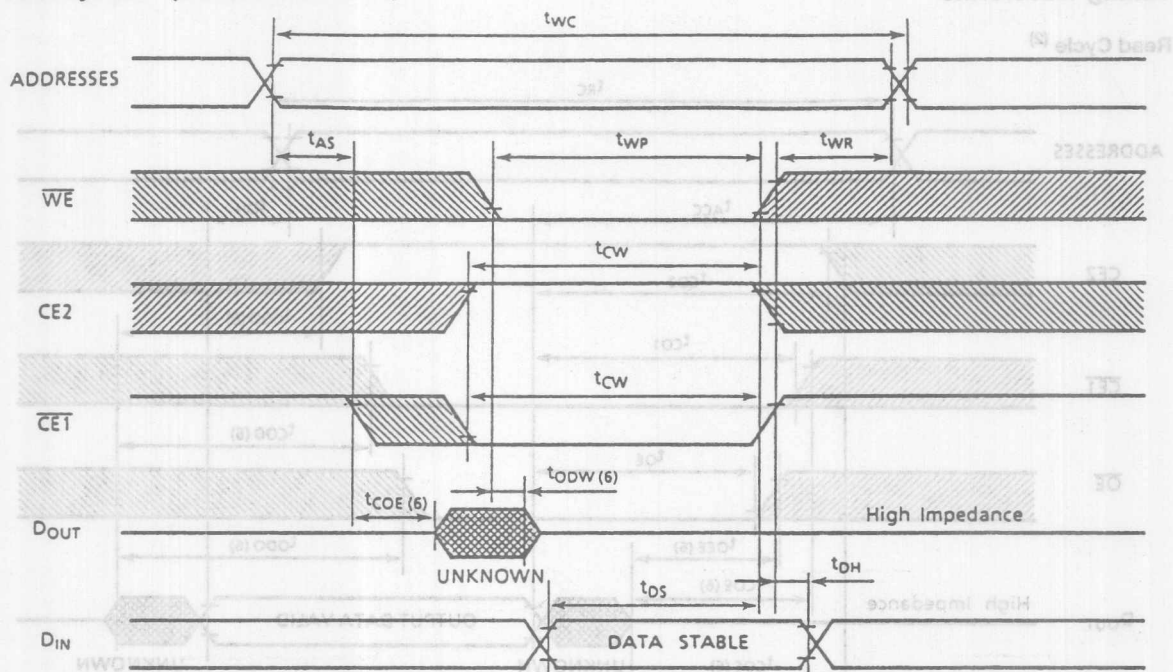
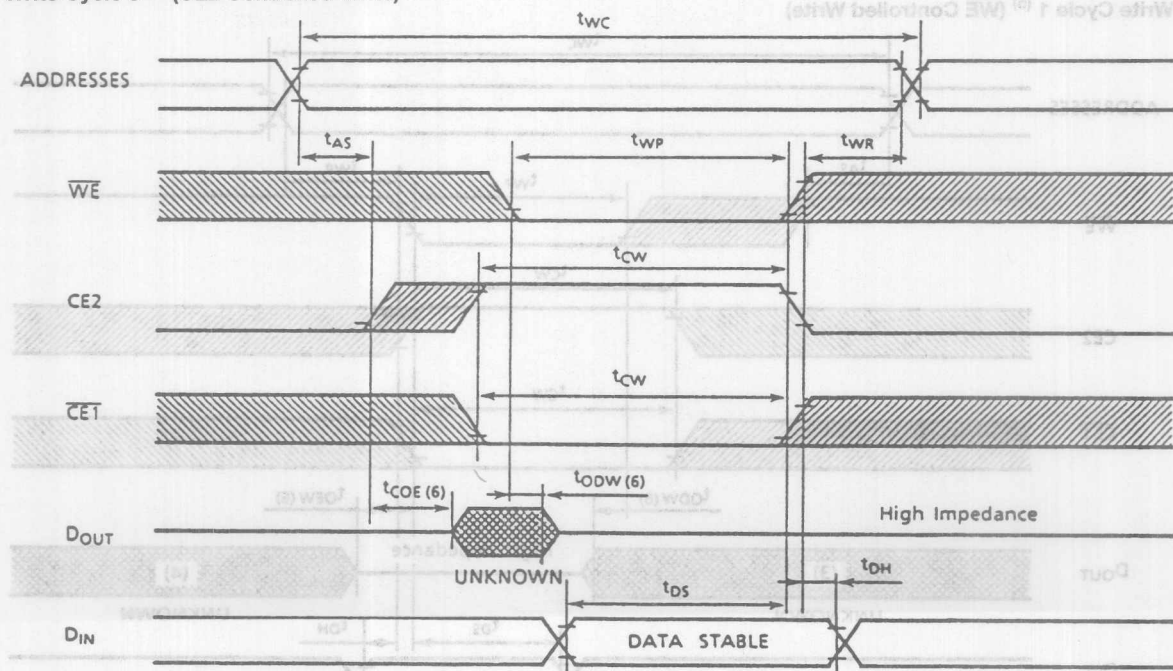


(For t_{COE} , t_{OEE} , t_{COD} , t_{ODO} , t_{OEw} and t_{ODw})

Figure 1.

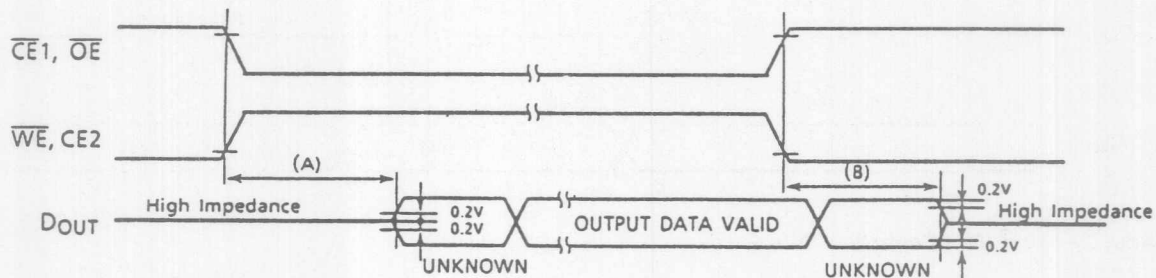
Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled Write)

Write Cycle 2⁽⁵⁾ ($\overline{\text{CE1}}$ Controlled Write)Write Cycle 3⁽⁵⁾ (CE2 Controlled Write)

Notes:

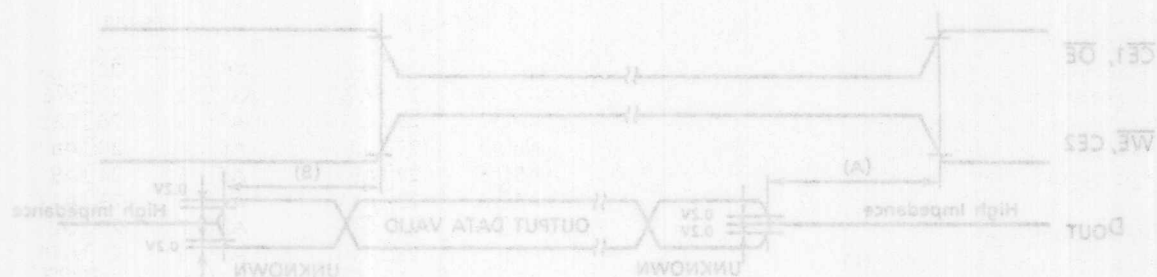
1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the $\overline{CE1}$ low transition or $CE2$ high transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the $\overline{CE1}$ high transition or $CE2$ low transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{COE} , t_{OEE} , $t_{OE\overline{W}}$ Output Enable Time
 - (B) t_{COD} , t_{ODO} , $t_{OD\overline{W}}$ Output Disable Time



Notes

Notes:

1. The operating temperature (T_o) is guaranteed with transfer air flow exceeding 100 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the $\overline{CE1}$ low transition or $\overline{CE2}$ high transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the $\overline{CE1}$ high transition or $\overline{CE2}$ low transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 (A) $t_{OE}^{\text{low-to-low}}$... Output Enable Time
 (B) $t_{OD}^{\text{low-to-low}}$... Output Disable Time



TC55B88P/J-10/12

SILICON GATE BiCMOS

8,192 WORD x 8 BIT BiCMOS STATIC RAM

Description

The TC55B88P/J is a 65,536 bit high speed BiCMOS static random access memory organized as 8,192 words by 8 bits and operated from a single 5V supply. Toshiba's BiCMOS technology and advanced circuit design enable high speed operation.

The TC55B88P/J features low power dissipation when the device is deselected using chip enable ($\overline{CE1}$, $\overline{CE2}$) and has an output enable input (\overline{OE}) for fast memory access.

The TC55B88P/J is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC55B88P/J is available in a 300mil width, 28-pin DIP and SOJ suitable for high density surface assembly.

Features

- Fast access time
 - TC55B88P/J-10 10ns (max.)
 - TC55B88P/J-12 12ns (max.)
- Low power dissipation
 - Operation: 155mA (max.)
 - Standby: 10mA (max.)
- Single 5V power supply: 5V \pm 5% (-10)
5V \pm 10% (-12)
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Package:
 - TC55B88P: DIP28-P-300B
 - TC55B88J: SOJ28-P-300A

Pin Names

A0 ~ A12	Address Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
$\overline{CE1}$, $\overline{CE2}$	Chip Enable Inputs
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V _{DD}	Power (+5V)
GND	Ground
NC	No Connection

Pin Connection (Top View)

TC55B88P

NC	1	28	V _{DD}
A12	2	27	\overline{WE}
A7	3	26	$\overline{CE2}$
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	\overline{OE}
A2	8	21	A10
A1	9	20	$\overline{CE1}$
A0	10	19	I/O8
I/O1	11	18	I/O7
I/O2	12	17	I/O6
I/O3	13	16	I/O5
GND	14	15	I/O4

(DIP)

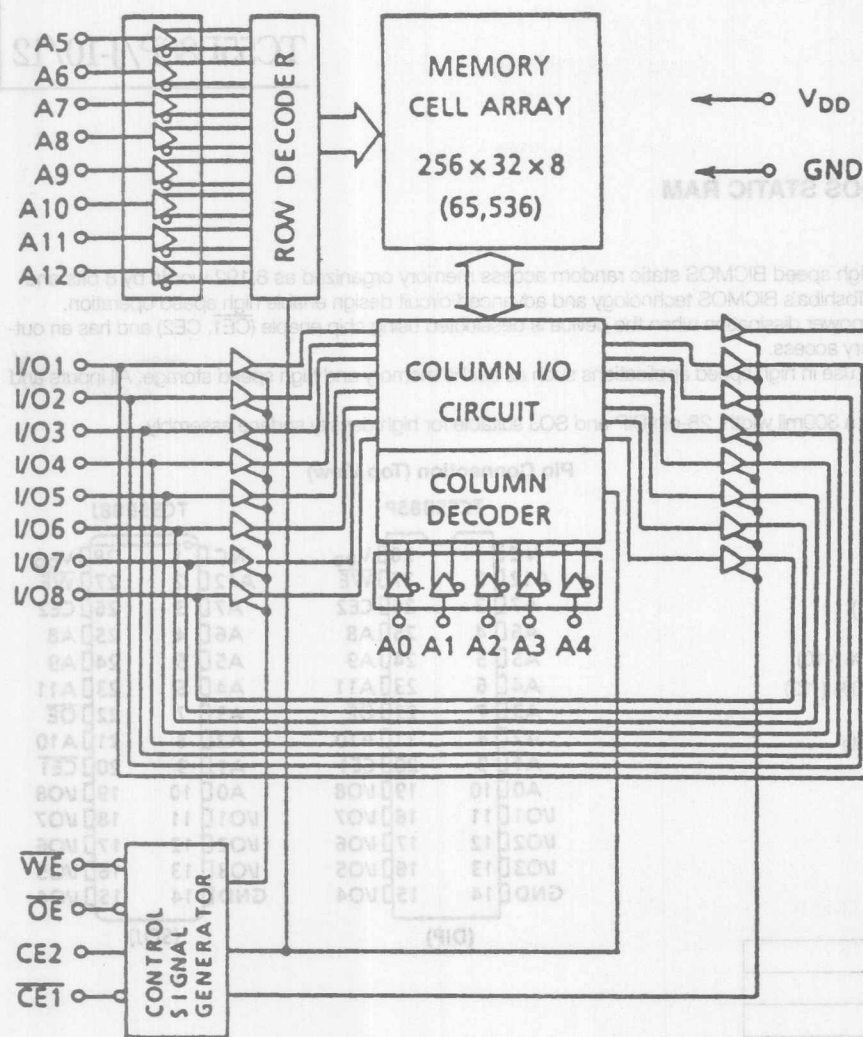
TC55B88J

NC	1	28	V _{DD}
A12	2	27	\overline{WE}
A7	3	26	$\overline{CE2}$
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	\overline{OE}
A2	8	21	A10
A1	9	20	$\overline{CE1}$
A0	10	19	I/O8
I/O1	11	18	I/O7
I/O2	12	17	I/O6
I/O3	13	16	I/O5
GND	14	15	I/O4

(SOJ)

UNIT	RATING	ITEM	SYMBOL
V	-0.5 - 7.0	Power Supply Voltage	V _{DD}
V	5.0 - 7.0	Input Voltage	V _{IN}
V	-0.5 - V _{DD} + 0.5	Input/Output Voltage	V _{IO}
W	1.0	Power Dissipation	P _D
°C • sec	260 • 10	Soldering Temperature • Time	T _{solder}
°C	-55 - 125	Storage Temperature	T _{stg}
°C	-10 - 85	Operating Temperature	T _{OP}

Block Diagram



Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0 ~ 7.0	V
V_{IO}	Input/Output Voltage	-0.5 ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	-10	4.75	5.0	V
		-12	4.5	5.0	
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

* -3V with a pulse width of 10ns

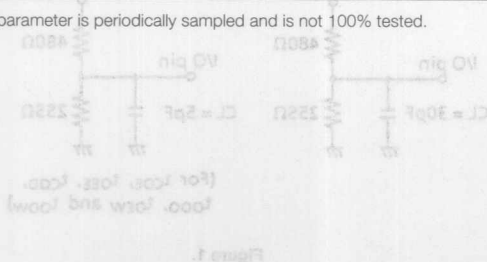
DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, -10: $V_{DD} = 5V \pm 5\%$, -12: $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{WE} = V_{IL}$ or $OE = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	8	—	—	mA
I_{DDC}	Operating Current	$t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$ Other Inputs = V_{IH}/V_{IL} $I_{OUT} = 0\text{mA}$ $V_{DD} = 5.25\text{V}$	-10	—	—	—
		$t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$ Other Inputs = V_{IH}/V_{IL} $I_{OUT} = 0\text{mA}$ $V_{DD} = 5.5\text{V}$	-12	—	—	155
I_{DDS1}	Standby Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ Other Inputs = V_{IH}/V_{IL} $V_{DD} = 5.25\text{V}$	-10	—	—	30
		$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ Other Inputs = V_{IH}/V_{IL} $V_{DD} = 5.5\text{V}$	-12	—	—	—
I_{DDS2}	Standby Current	$\overline{CE1} = V_{DD} - 0.2\text{V}$ or $CE2 = 0.2\text{V}$ Other Inputs = $V_{DD} - 0.2\text{V}$ or 0.2V	—	—	10	—

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	7	pF

*This parameter is periodically sampled and is not 100% tested.



AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, -10: $V_{DD} = 5V \pm 5\%$, -12: $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55B88P/J-10		TC55B88P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	—	12	—	
t_{ACC}	Address Access Time	—	10	—	12	
t_{CO1}	$\overline{CE1}$ Access Time	—	10	—	12	
t_{CO2}	$\overline{CE2}$ Access Time	—	10	—	12	
t_{OE}	\overline{OE} Access Time	—	6	—	7	
t_{OH}	Output Data Hold Time from Address Change	3	—	3	—	ns
t_{COE}	Output Enable Time from $\overline{CE1}$ or $\overline{CE2}$	3	—	3	—	
t_{COD}	Output Disable Time from $\overline{CE1}$ or $\overline{CE2}$	—	5	—	6	
t_{OEE}	Output Enable Time from \overline{OE}	1	—	1	—	
t_{ODO}	Output Disable Time from \overline{OE}	—	5	—	6	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	10	—	12	

Write Cycle

SYMBOL	PARAMETER	TC55B88P/J-10		TC55B88P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	—	12	—	
t_{CW}	Chip Enable to End of Write	7	—	8	—	
t_{AS}	Address Setup Time	0	—	0	—	
t_{AW}	Address Valid to End of Write	7	—	8	—	
t_{WP}	Write Pulse Width	6	—	7	—	ns
t_{WR}	Write Recovery Time	1	—	1	—	
t_{DS}	Data Setup Time	6	—	7	—	
t_{DH}	Data Hold Time	0	—	0	—	
t_{OEw}	Output Enable Time from \overline{WE}	1	—	1	—	
t_{ODw}	Output Disable Time from \overline{WE}	—	5	—	6	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

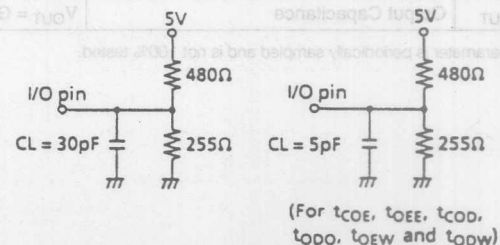
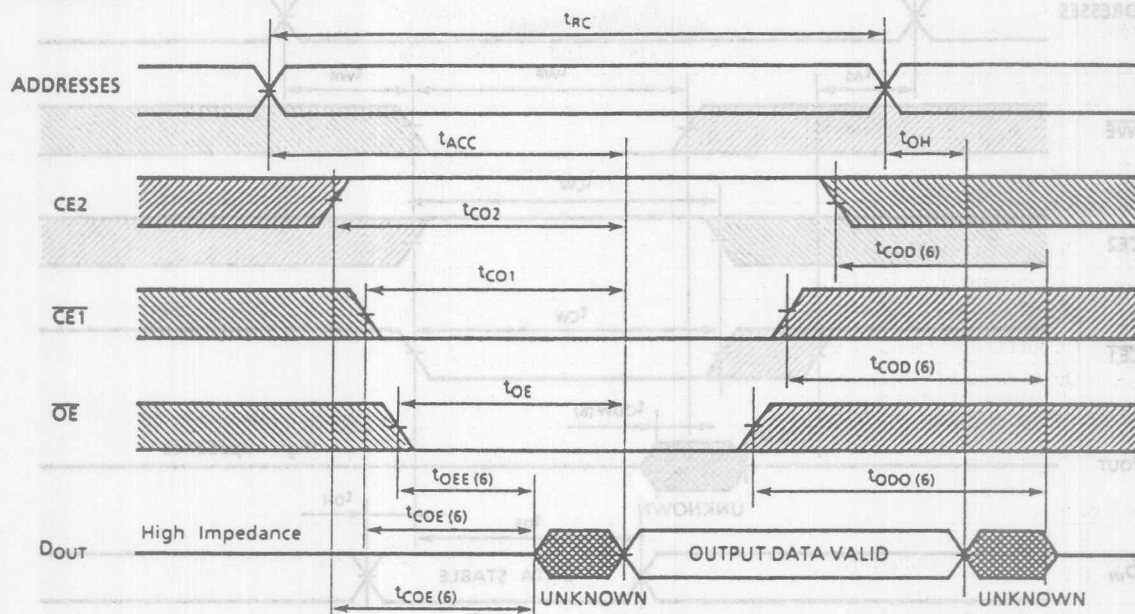
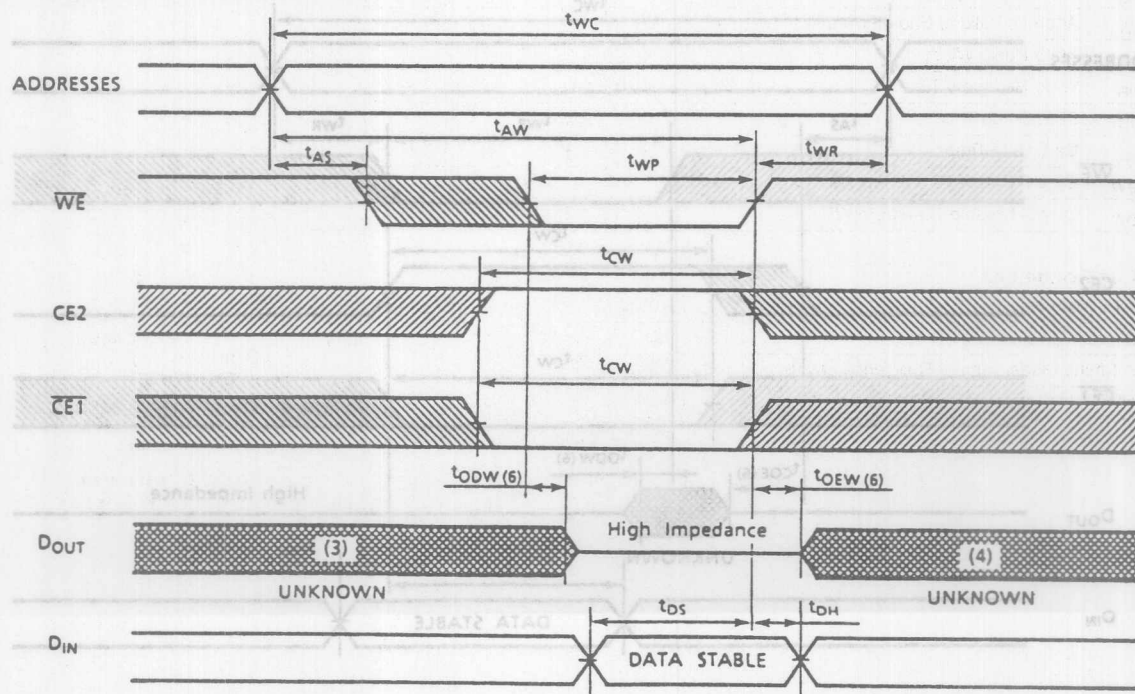
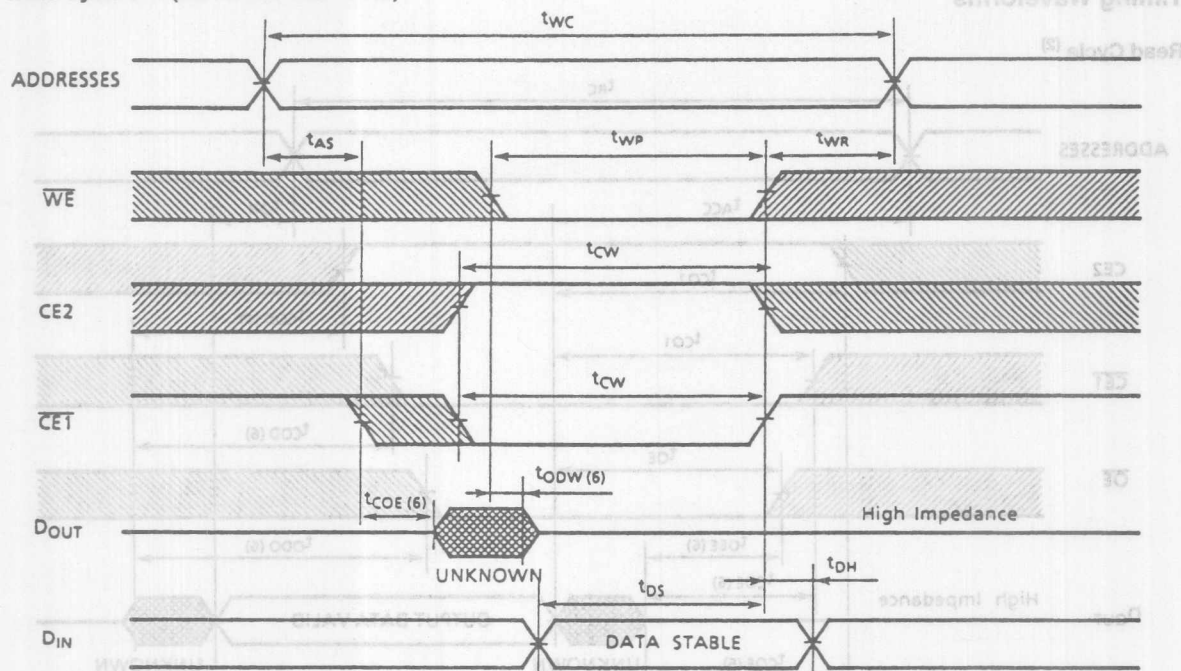
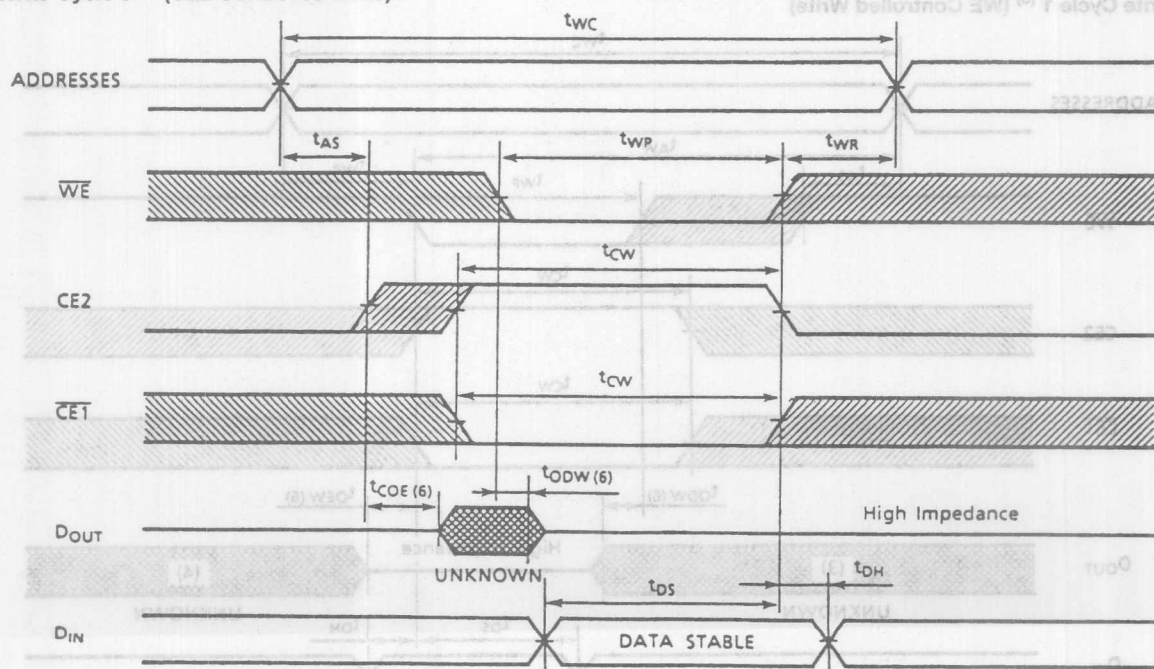


Figure 1.

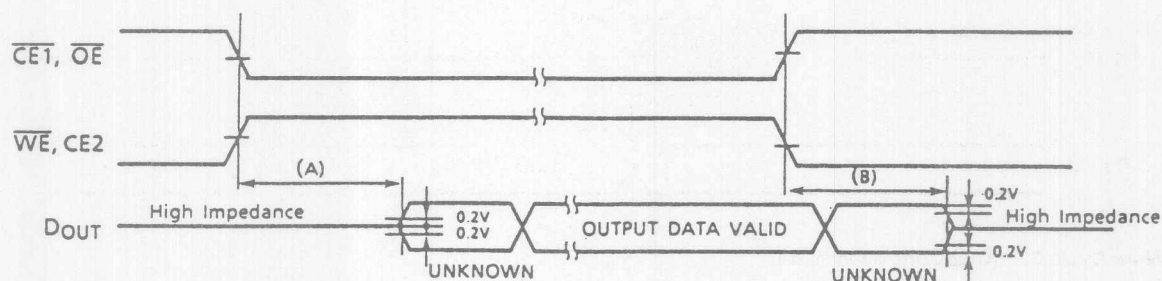
Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled Write)

Write Cycle 2 ⁽⁵⁾ ($\overline{\text{CE1}}$ Controlled Write)Write Cycle 3 ⁽⁵⁾ (CE2 Controlled Write)

Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the $\overline{CE1}$ low transition or $CE2$ high transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the $\overline{CE1}$ high transition or $CE2$ low transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{OE} , t_{OEE} , t_{OEw} Output Enable Time
 - (B) t_{OD} , t_{ODO} , t_{ODw} Output Disable Time



SILICON GATE CMOS

8,192 WORD x 9 BIT CMOS STATIC RAM

Description

The TC5589P/J is a 73,728 bit high speed CMOS static random access memory organized as 8,192 words by 9 bits and operated from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC5589P/J features low power dissipation when the device is deselected using chip enable ($\overline{CE1}$, $\overline{CE2}$) and has an output enable input (\overline{OE}) for fast memory access. Also, the device power between memory accesses is reduced by an automatic power down circuit.

The TC5589P/J is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC5589P/J is available in a 300mil width, 28-pin DIP and SOJ suitable for high density surface assembly.

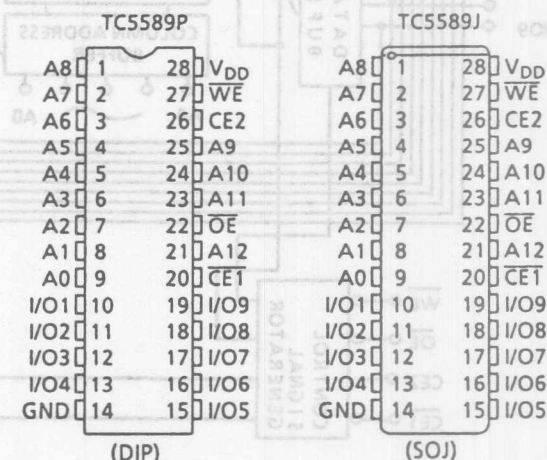
Features

- Fast access time
 - TC5589P/J-15 15ns (max.)
 - TC5589P/J-20 20ns (max.)
 - TC5589P/J-25 25ns (max.)
 - TC5589P/J-35 35ns (max.)
- Low power dissipation
 - Operation:
 - TC5589P/J-15 135mA (max.)
 - TC5589P/J-20 115mA (max.)
 - TC5589P/J-25 115mA (max.)
 - TC5589P/J-35 115mA (max.)
 - Standby: 1mA (max.)
- Single 5V power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Package:
 - TC5589P: DIP28-P-300B
 - TC5589J: SOJ28-P-300A

Pin Names

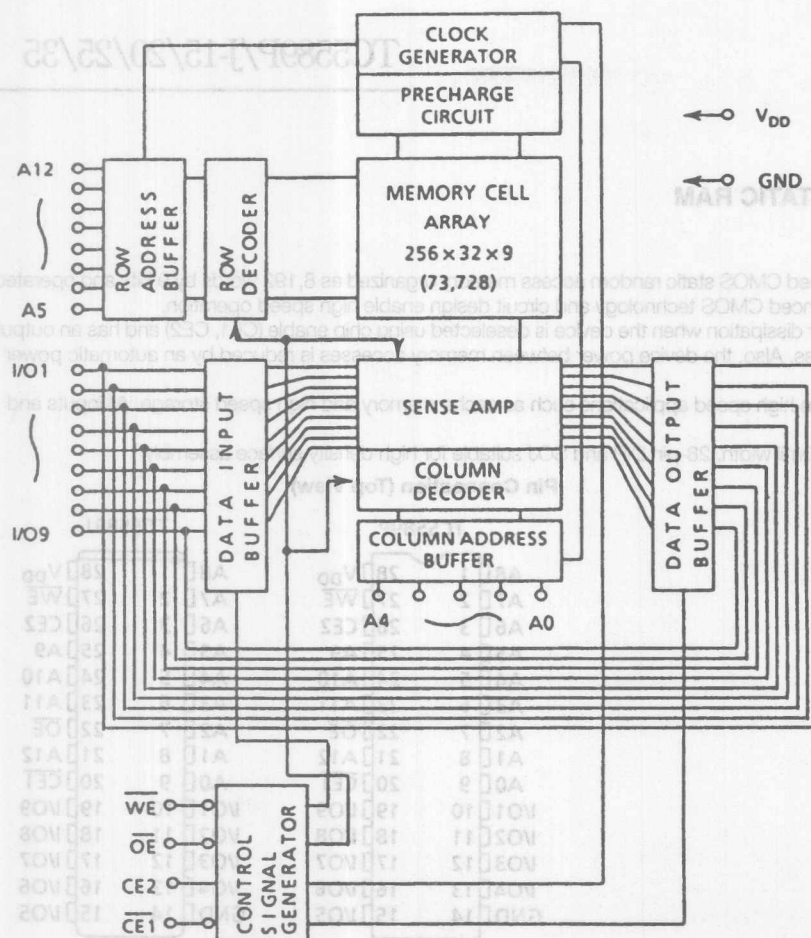
A0 ~ A12	Address Inputs
I/O1 ~ I/O9	Data Inputs/Outputs
$\overline{CE1}$, $\overline{CE2}$	Chip Enable Inputs
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground

Pin Connection (Top View)



UNIT	RATING	ITEM	SYMBOL
V	0.5 - 7.0	Power Supply Voltage	V_{DD}
V	0.5 - 7.0	Input Voltage	V_{IH}
V	0.5 - $V_{DD} + 0.5$	Input/Output Voltage	V_{IO}
W	1.0	Power Dissipation	P_D
$^{\circ}C \cdot sec$	500 - 10	Soldering Temperature - Time	T_{SOLDER}
$^{\circ}C$	-55 - 150	Storage Temperature	T_{STG}
$^{\circ}C$	-55 - 85	Operating Temperature	T_{OP}

Block Diagram



Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V _{IN}	Input Voltage	-2.0 ~ 7.0	V
V _{I/O}	Input/Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-65 ~ 150	°C
T _{OPR}	Operating Temperature	-10 ~ 85	°C

- Fast access time
 - TC5589P/J-15 15ns (max)
 - TC5589P/J-20 20ns (max)
 - TC5589P/J-25 25ns (max)
 - TC5589P/J-35 35ns (max)
- Low power dissipation
 - Operation
 - TC5589P/J-15 150mW (max)
 - TC5589P/J-20 115mW (max)
 - TC5589P/J-25 115mW (max)
 - TC5589P/J-35 115mW (max)
 - Standby
 - 1mW (max)
- Single 5V power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: OE
- Package:
 - TC5589P: DIP28-P-300B
 - TC5589J: SOL28-P-300A

Pin Names

A0 - A12	Address inputs
I/O0 - I/O9	Data Input/Outputs
CE1, CE2	Chip Enable inputs
WE	Write Enable input
OE	Output Enable input
V _{DD} (+5V)	Power (+5V)
GND	Ground

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

* -3V with a pulse width of 10ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1	μA
I_{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	8	—	—	mA
I_{DDO}	Operating Current	$V_{DD} = 5.5V$ $t_{\text{cycle}} = \text{Min cycle}$	-15	—	135	mA
		$\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$	-20	—	—	
		Other Inputs = V_{IH}/V_{IL}	-25	—	115	
		$I_{OUT} = 0\text{mA}$	-35	—	—	
I_{DDs1}	Standby Current	$V_{DD} = 5.5V$ $t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ Other Inputs = V_{IH}/V_{IL}	—	—	25	mA
I_{DDs2}^*		$\overline{CE1} = V_{DD} - 0.2V$ or $CE2 = 0.2V$ Other Inputs = $V_{DD} - 0.2V$ or $0.2V$	—	—	1	μA

* If $\overline{CE1} \geq V_{DD} - 0.2V$, the specified limits are guaranteed under the condition $CE2 \geq V_{DD} - 0.2V$ or $CE2 \leq 0.2V$.

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	7	pF

*This parameter is periodically sampled and is not 100% tested.

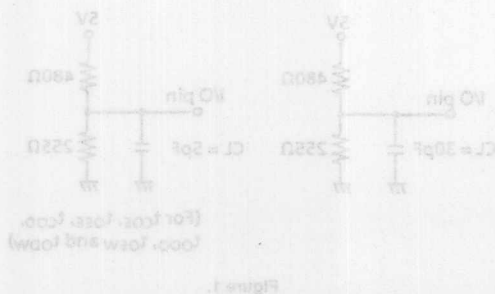


Fig. 1	Output Load	Output Timing Measurement Reference Level	Input Timing Measurement Reference Level	Input Pulse Rise and Fall Time	Input Pulse Levels	AC Test Conditions
		2.0V/0.8V	2.3V/0.8V	2.3V/0.8V	2.3V/0.8V	
		2.0V/0.8V	2.3V/0.8V	2.3V/0.8V	2.3V/0.8V	
		2.0V/0.8V	2.3V/0.8V	2.3V/0.8V	2.3V/0.8V	

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC5589P/J-15		TC5589P/J-20		TC5589P/J-25		TC5589P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	
t_{ACC}	Address Access Time	—	15	—	20	—	25	—	35	
t_{CO1}	$\overline{CE1}$ Access Time	—	15	—	20	—	25	—	35	
t_{CO2}	$\overline{CE2}$ Access Time	—	15	—	20	—	25	—	35	
t_{OE}	\overline{OE} Access Time	—	9	—	10	—	12	—	12	
t_{OH}	Output Data Hold Time from Address Change	5	—	5	—	5	—	5	—	ns
t_{COE}	Output Enable Time from $\overline{CE1}$ or $\overline{CE2}$	5	—	5	—	5	—	5	—	
t_{COD}	Output Disable Time from $\overline{CE1}$ or $\overline{CE2}$	—	6	—	6	—	6	—	6	
t_{OEE}	Output Enable Time from \overline{OE}	0	—	0	—	0	—	0	—	
t_{ODO}	Output Disable Time from \overline{OE}	—	5	—	5	—	5	—	5	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	15	—	20	—	25	—	35	

Write Cycle

SYMBOL	PARAMETER	TC5589P/J-15		TC5589P/J-20		TC5589P/J-25		TC5589P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	—	20	—	25	—	35	—	
t_{CW}	Chip Enable to End of Write	12	—	13	—	15	—	15	—	
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	
t_{WP}	Write Pulse Width	12	—	13	—	15	—	15	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DS}	Data Setup Time	9	—	10	—	12	—	12	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	
t_{OEw}	Output Enable Time from \overline{WE}	0	—	0	—	0	—	0	—	
t_{ODw}	Output Disable Time from \overline{WE}	—	6	—	6	—	6	—	6	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

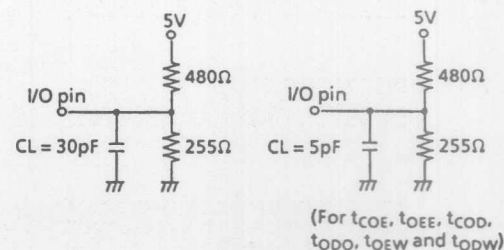
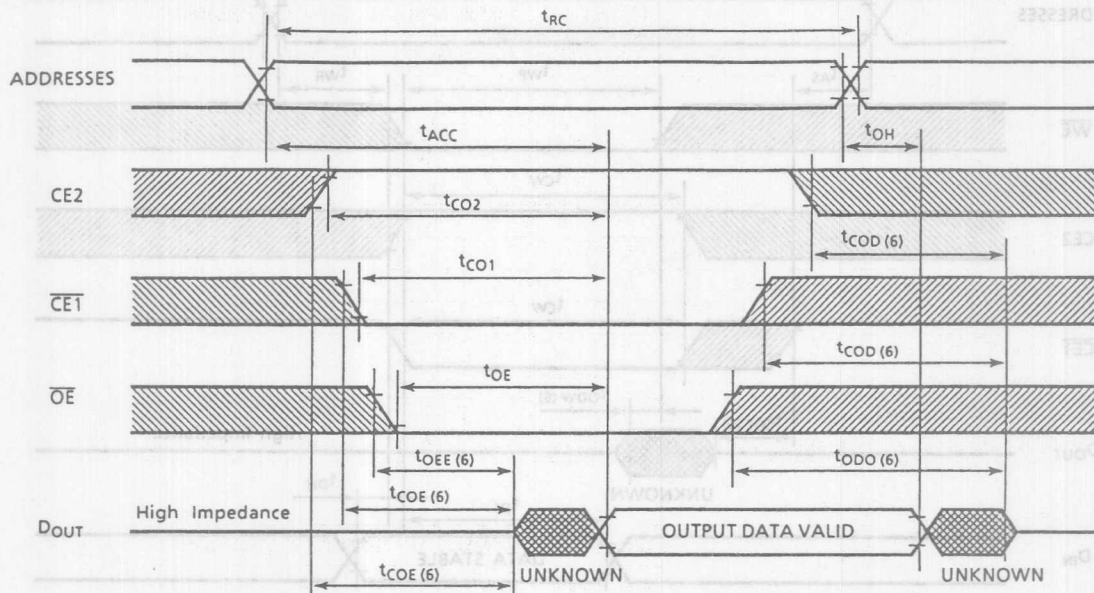
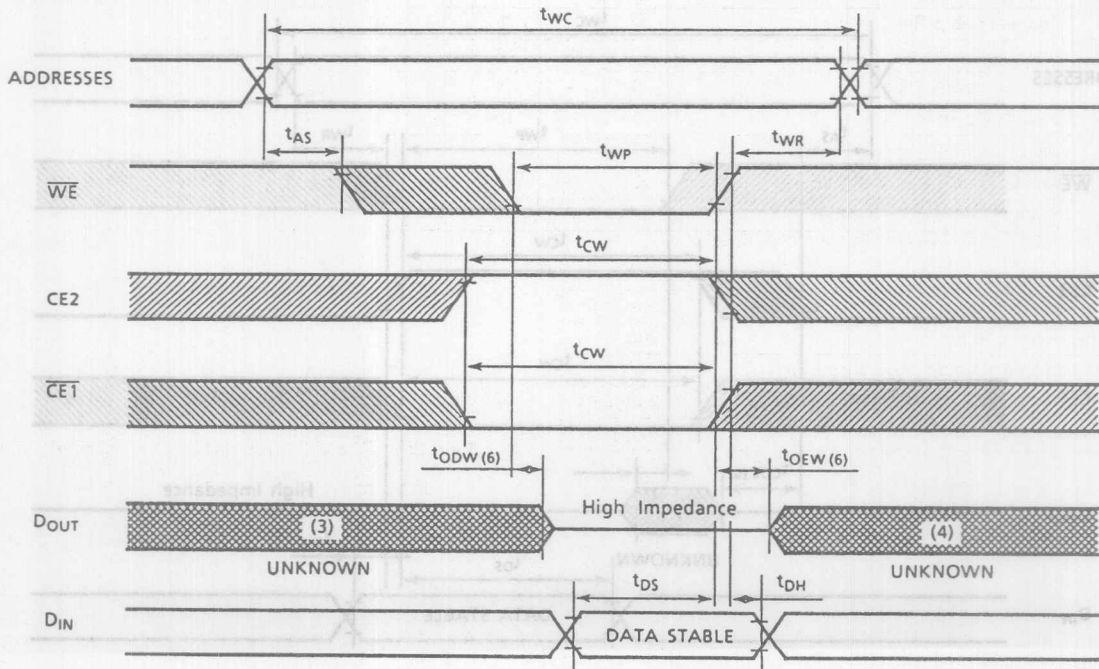
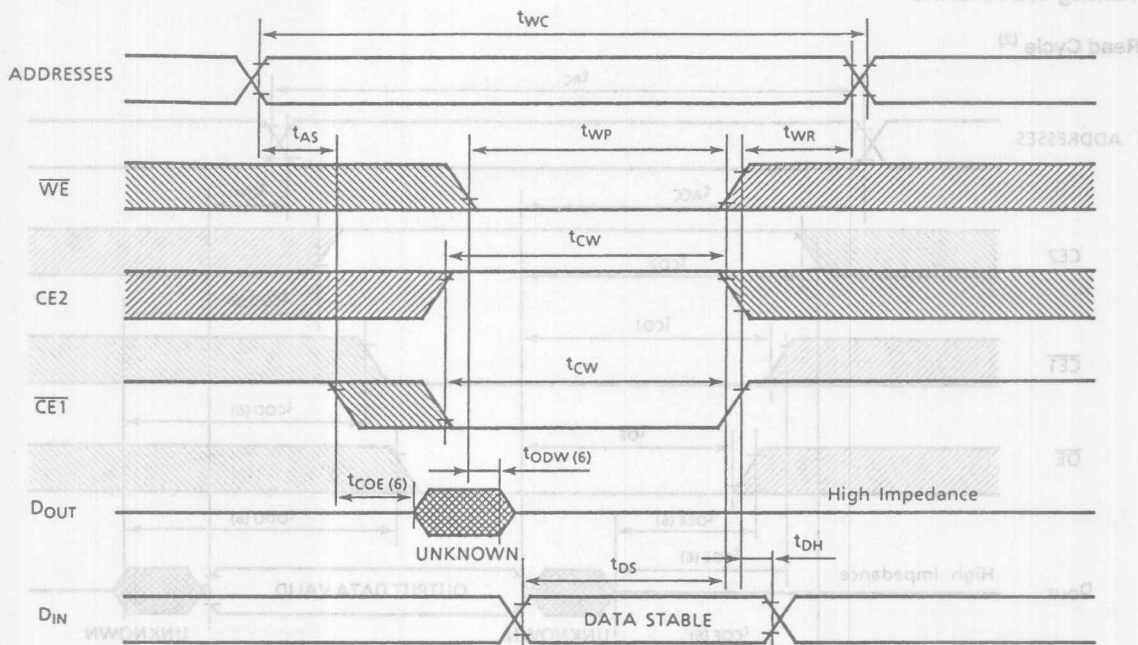
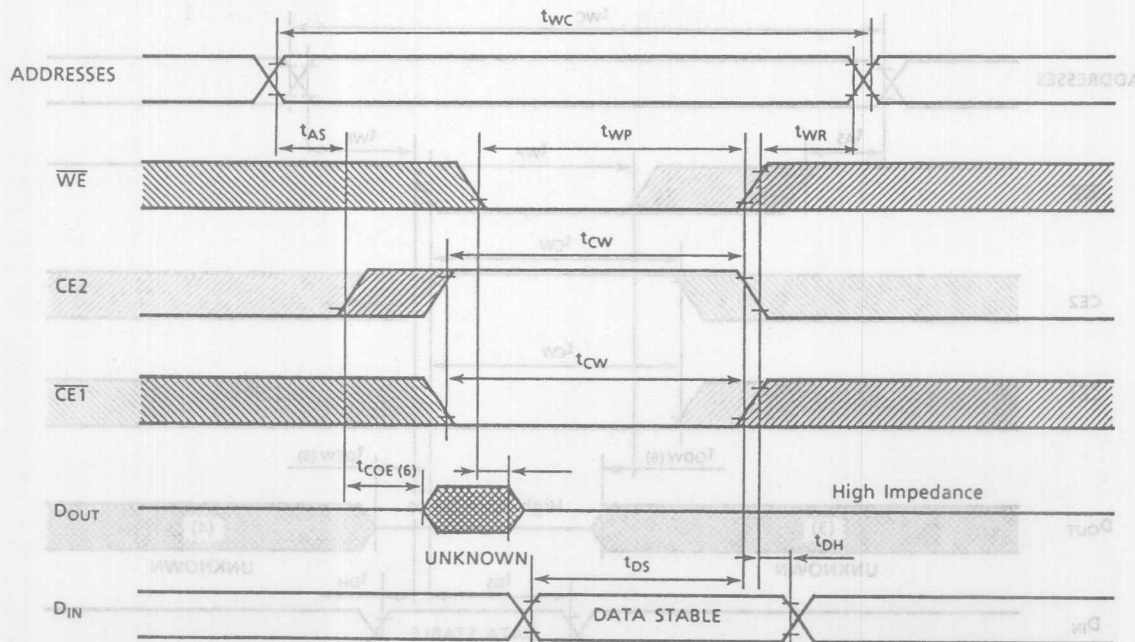


Figure 1.

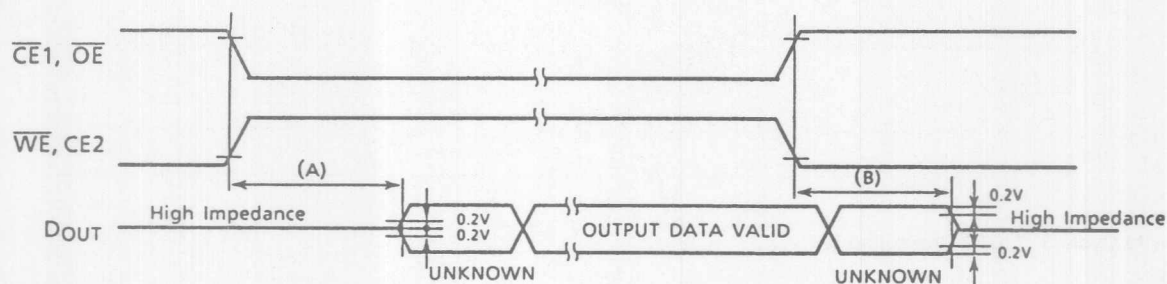
Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled Write)

Write Cycle 2 ⁽⁵⁾ ($\overline{\text{CE1}}$ Controlled Write)Write Cycle 3 ⁽⁵⁾ (CE2 Controlled Write)

Notes:

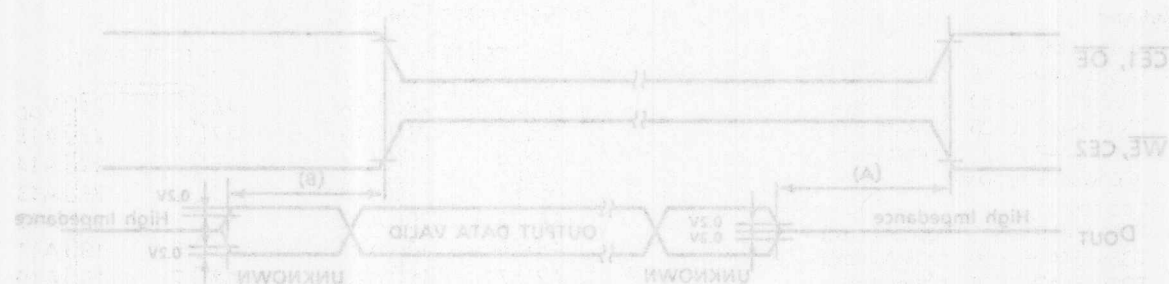
1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the $\overline{CE1}$ low transition or $CE2$ high transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the $\overline{CE1}$ high transition or $CE2$ low transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{COE} , t_{OEE} , $t_{OE\overline{W}}$ Output Enable Time
 - (B) t_{COD} , t_{ODO} , $t_{OD\overline{W}}$ Output Disable Time



Notes

Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 100 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the $\overline{CE1}$ low transition or $\overline{CE2}$ high transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the $\overline{CE1}$ high transition or $\overline{CE2}$ low transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{OE} : low to low Output Enable Time
 - (B) t_{OD} : low to low Output Disable Time



TC55464AP/AJ-15/20/25/35

SILICON GATE CMOS

65,536 WORD x 4 BIT CMOS STATIC RAM

Description

The TC55464AP/AJ is a 262,144 bit high speed CMOS static random access memory organized as 65,536 words by 4 bits and operated from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC55464AP/AJ features low power dissipation when the device is deselected using chip enable (\overline{CE}). Also, the device power between memory accesses is reduced by an automatic power down circuit.

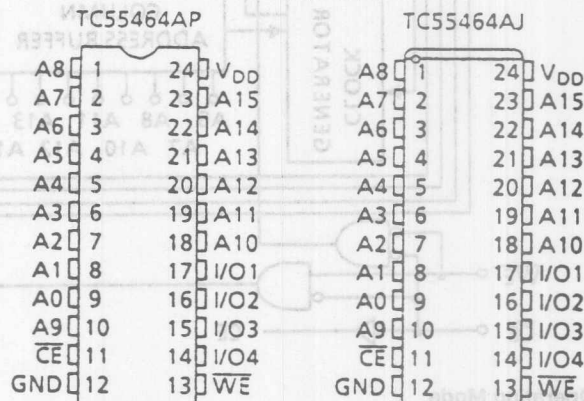
The TC55464AP/AJ is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC55464AP/AJ is available in a 300mil width, 24-pin DIP and SOJ suitable for high density surface assembly.

Features

- Fast access time
 - TC55464AP/AJ-15 15ns (max.)
 - TC55464AP/AJ-20 20ns (max.)
 - TC55464AP/AJ-25 25ns (max.)
 - TC55464AP/AJ-35 35ns (max.)
- Low power dissipation
 - Operation:
 - TC55464AP/AJ-10 120mA (max.)
 - TC55464AP/AJ-20 120mA (max.)
 - TC55464AP/AJ-25 120mA (max.)
 - TC55464AP/AJ-35 100mA (max.)
 - Standby: 1mA (max.)
- Single 5V power supply: $5V \pm 10\%$
- Fully static operation
- Inputs and outputs TTL compatible
- Package:
 - TC55464AP: DIP24-P-300B
 - TC55464AJ: SOJ24-P-300A

Pin Connection (Top View)



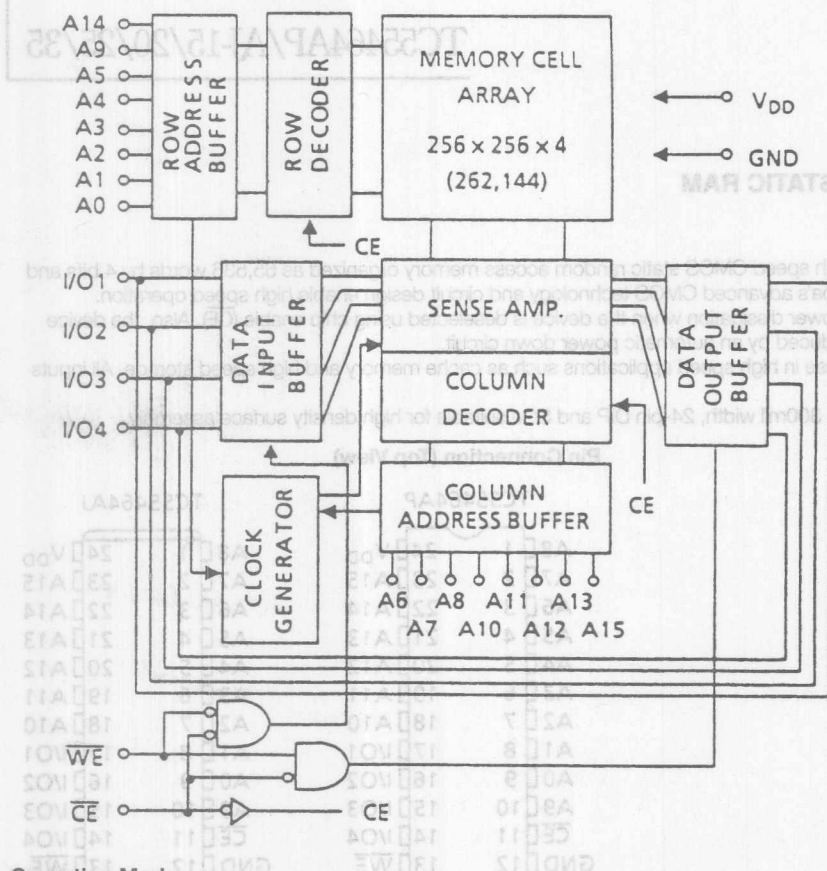
Pin Names

A0 ~ A15	Address Inputs
I/O1 ~ I/O4	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
WE	Write Enable Input
V _{DD}	Power (+5V)
GND	Ground

MODE	CE	WE	POWER
Standby	H	H	Low Impedance
Write	L	L	Input
Read	L	H	Output
Power	H	H	Low Impedance

SYMBOL	ITEM	UNIT
V _{DD}	Power Supply Voltage	V
V _{IN}	Input Voltage	V
V _{IO}	Input/Output Voltage	V
P _D	Power Dissipation	W
T _{SDR}	Storage Temperature	°C
T _{OP}	Operating Temperature	°C

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{WE}	I/O1 ~ I/O4	POWER
Read		L	H	Output	I_{DDO}
Write		L	L	Input	I_{DDO}
Standby		H	*	High Impedance	I_{DDs}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

* -3V with a pulse width of 10ns

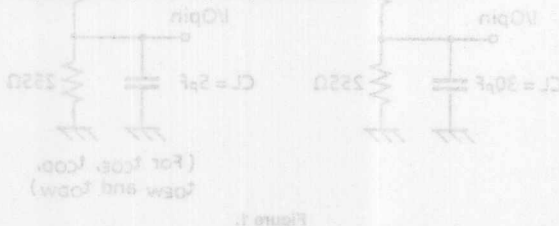
DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	8	—	—	mA
I_{DDO}	Operating Current	$t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE} = V_{IL}$ Other Inputs = V_{IH}/V_{IL}	-15	—	—	120
			-20	—	—	120
			-25	—	—	120
			-35	—	—	100
I_{DDS1}	Standby Current	$t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE} = V_{IH}$ Other Inputs = V_{IH}/V_{IL}	-15	—	—	20
			-20	—	—	20
			-25	—	—	20
			-35	—	—	20
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2V$ Other Inputs = $V_{DD} - 0.2V$ or $0.2V$	—	—	—	1

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
C_{IO}	Input/Output Capacitance	$V_{IO} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.



AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55464AP/AJ-15		TC55464AP/AJ-20		TC55464AP/AJ-25		TC55464AP/AJ-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	ns
t_{ACC}	Address Access Time	—	15	—	20	—	25	—	35	ns
t_{CO}	\overline{CE} Access Time	—	15	—	20	—	25	—	35	ns
t_{OH}	Output Data Hold Time from Address Change	5	—	5	—	5	—	5	—	ns
t_{COE}	Output Enable Time from \overline{CE}	5	—	5	—	5	—	5	—	ns
t_{COD}	Output Disable Time from \overline{CE}	—	8	—	8	—	10	—	15	ns

Write Cycle

SYMBOL	PARAMETER	TC55464AP/AJ-15		TC55464AP/AJ-20		TC55464AP/AJ-25		TC55464AP/AJ-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	—	20	—	25	—	35	—	ns
t_{WP}	Write Pulse Width	10	—	11	—	13	—	18	—	ns
t_{AW}	Address Valid to End of Write	12	—	13	—	15	—	20	—	ns
t_{CW}	Chip Enable to End of Write	12	—	13	—	15	—	20	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DS}	Data Setup Time	8	—	10	—	12	—	15	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{OEw}	Output Enable Time from \overline{WE}	1	—	1	—	1	—	1	—	ns
t_{ODw}	Output Disable Time from \overline{WE}	—	8	—	8	—	10	—	15	ns

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

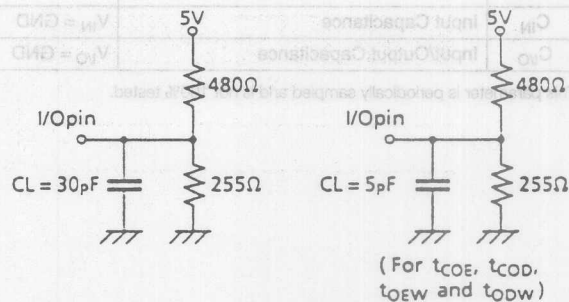
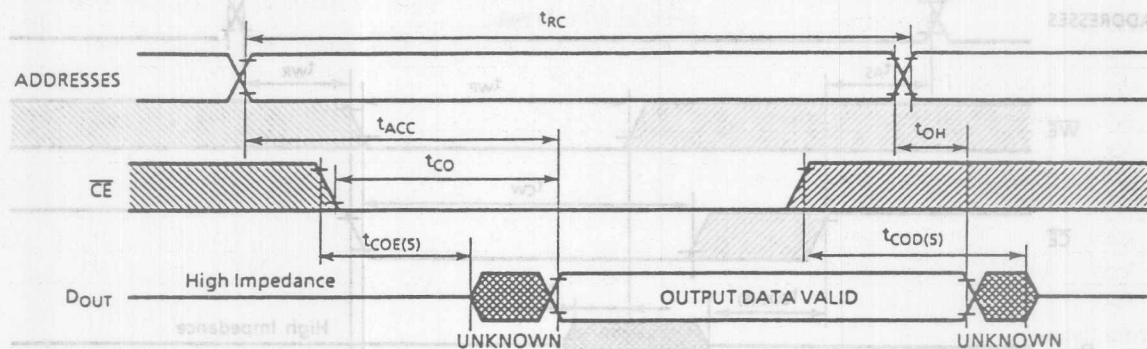
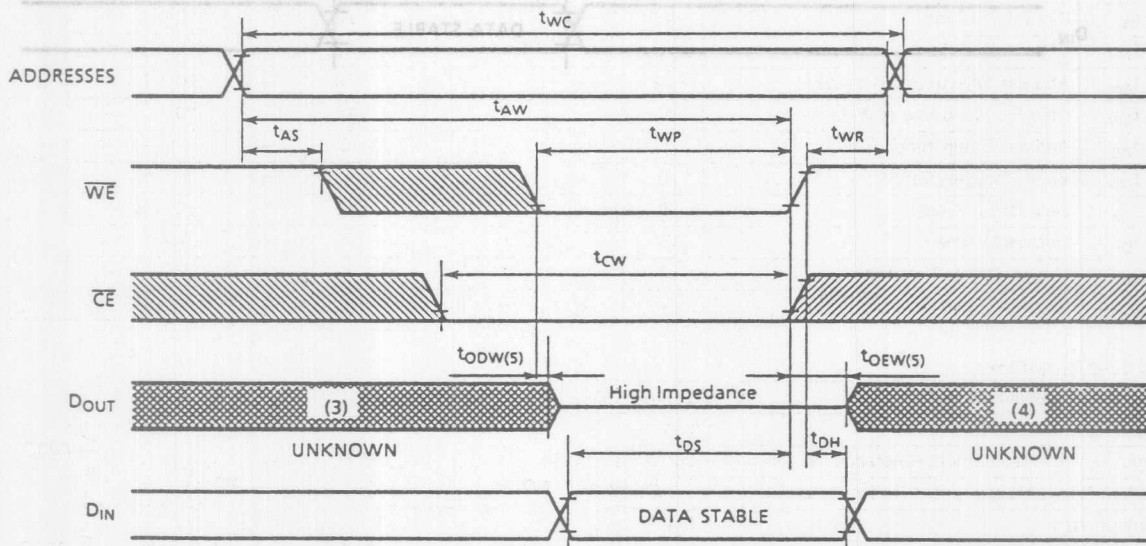
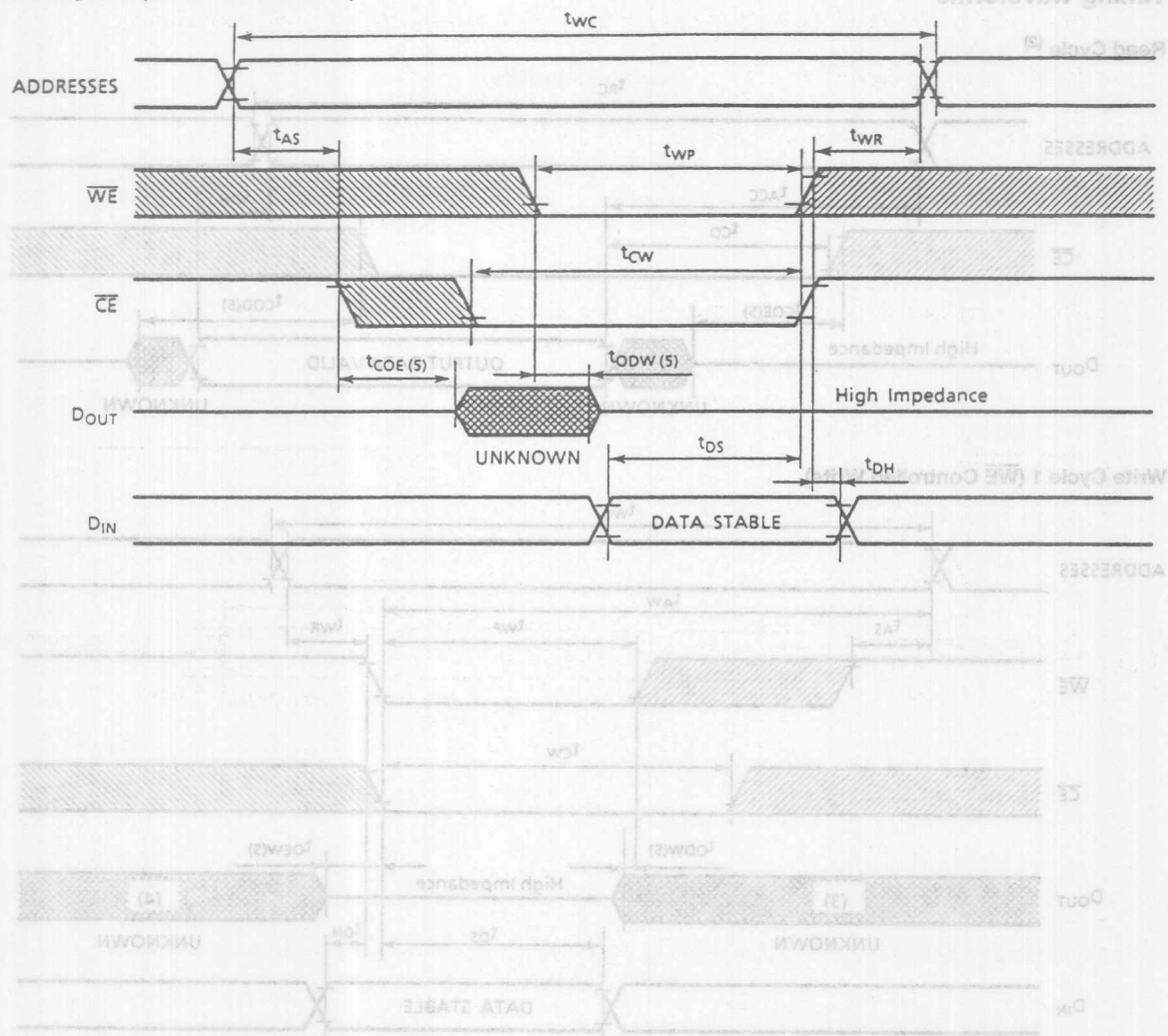


Figure 1.

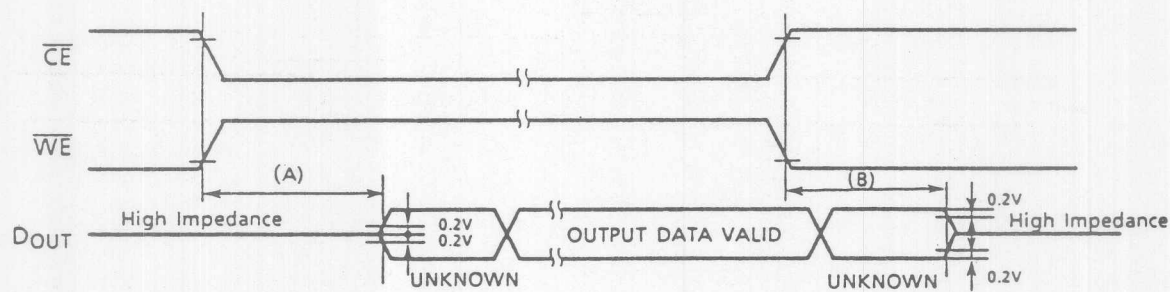
Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 (\overline{WE} Controlled Write)

Write Cycle 2 (\overline{CE} Controlled Write)

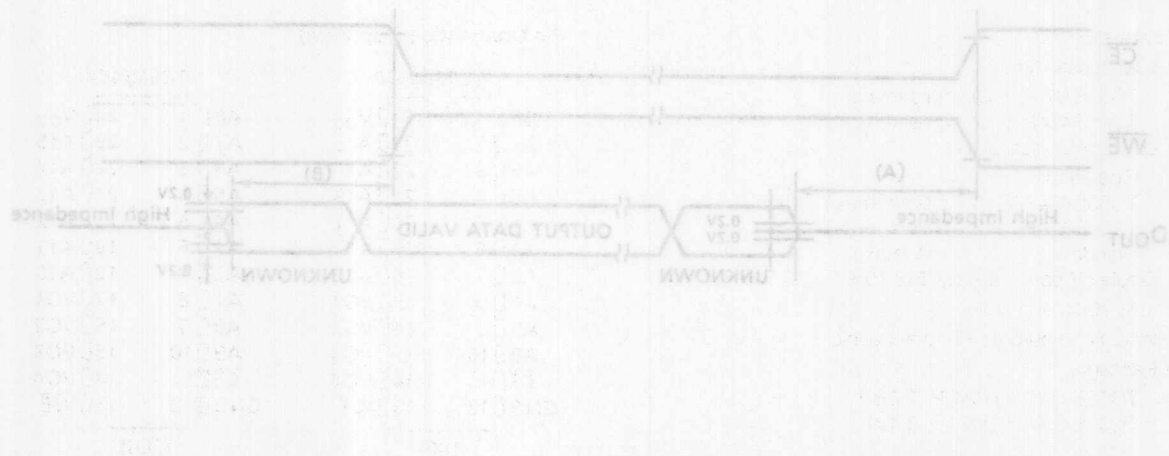
Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{COE} , $t_{OE\overline{W}}$ Output Enable Time
 - (B) t_{COD} , $t_{OD\overline{W}}$ Output Disable Time



Notes

1. The operating temperature (T_s) is guaranteed with turnover air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{OE} (low) Output Enable Time
 - (B) t_{OD} (low) Output Disable Time



TC55B464P/J-10/12

SILICON GATE BiCMOS

65,536 WORD x 4 BIT BiCMOS STATIC RAM

Description

The TC55B464P/J is a 262,144 bit high speed BiCMOS static random access memory organized as 65,536 words by 4 bits and operated from a single 5V supply. Toshiba's BiCMOS technology and advanced circuit design enable high speed operation.

The TC55B464P/J features low power dissipation when the device is deselected using chip enable (CE).

The TC55B464P/J is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC55B464P/J is available in a 300mil width, 24-pin DIP and SOJ suitable for high density surface assembly.

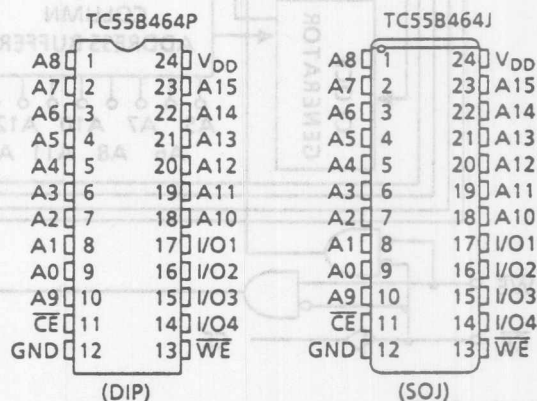
Features

- Fast access time
 - TC55B464P/J-10 10ns (max.)
 - TC55B464P/J-12 12ns (max.)
- Low power dissipation
 - Operation:
 - TC55B464P/J-10 140mA (max.)
 - TC55B464P/J-12 140mA (max.)
 - Standby: 15mA (max.)
- Single 5V power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Package:
 - TC55B464P: DIP24-P-300B
 - TC55B464J: SOJ24-P-300A

Pin Names

A0 ~ A15	Address Inputs
I/O1 ~ I/O4	Data Inputs/Outputs
CE	Chip Enable Input
WE	Write Enable Input
V _{DD}	Power (+5V)
GND	Ground

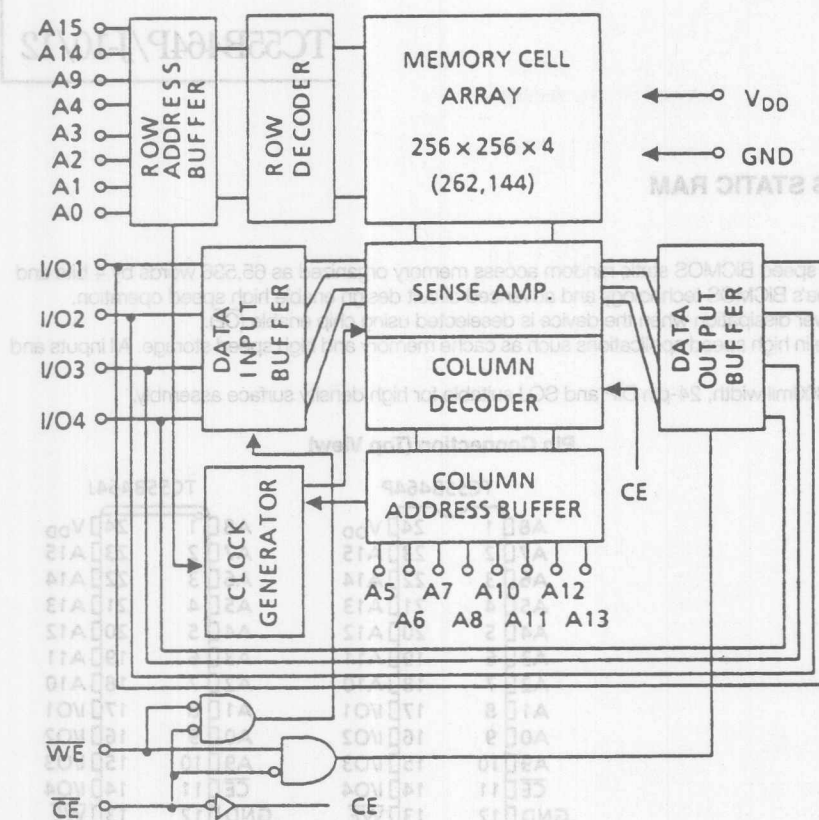
Pin Connection (Top View)



MODE	CE	WE	I/O1 - I/O4	POWER
Read	L	H	Output	1000
Write	L	L	Input	1000
Standby	H	-	High Impedance	1000

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V _{IN}	Input Voltage	-0.5 ~ 7.0	V
V _{IO}	Input/Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0	W
T _{SO}	Soldering Temperature - Time	260 ± 10	°C • sec
T _{STG}	Storage Temperature	-65 ~ 150	°C
T _{OP}	Operating Temperature	-10 ~ 85	°C

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{WE}	I/O1 ~ I/O4	POWER
Read		L	H	Output	I_{DDO}
Write		L	L	Input	I_{DDO}
Standby		H	*	High Impedance	I_{DDS}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0 ~ 7.0	V
V_{IO}	Input/Output Voltage	-0.5 ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

* -3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

* -3V with a pulse width of 10ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	8	—	—	mA
I_{DDO}	Operating Current	$t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE} = V_{IL}$ Other Inputs = V_{IH}/V_{IL} , $I_{OUT} = 0\text{mA}$	—	—	140	mA
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$ Other Inputs = V_{IH}/V_{IL}	—	—	30	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2\text{V}$ Other Inputs = $V_{DD} - 0.2\text{V}$ or 0.2V	—	—	15	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
C_{IO}	Input/Output Capacitance	$V_{IO} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.



Figure 1.
(For C_{IN} , C_{IO} , t_{cycle} and t_{setup})

Fig. 1	Output Timing Measurement Reference Levels
1.5V	Input Timing Measurement Reference Levels
1.5V	Input Pulse Rise and Fall Time
3ns	Input Pulse Levels
3.0V/0.0V	

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55B464P/J-10		TC55B464P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	—	12	—	ns
t_{ACC}	Address Access Time	—	10	—	12	ns
t_{CO}	\overline{CE} Access Time	—	10	—	12	ns
t_{OH}	Output Data Hold Time from Address Change	3	—	3	—	ns
t_{COE}	Output Enable Time from \overline{CE}	3	—	3	—	ns
t_{COD}	Output Disable Time from \overline{CE}	—	5	—	6	ns
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	ns
t_{PD}	Chip Deselection to Power Down Time	—	10	—	12	ns

Write Cycle

SYMBOL	PARAMETER	TC55B464P/J-10		TC55B464P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	—	12	—	ns
t_{CW}	Chip Enable to End of Write	7	—	8	—	ns
t_{AS}	Address Setup Time	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	7	—	8	—	ns
t_{WP}	Write Pulse Width	6	—	7	—	ns
t_{WR}	Write Recovery Time	1	—	1	—	ns
t_{DS}	Data Setup Time	6	—	7	—	ns
t_{DH}	Data Hold Time	0	—	0	—	ns
$t_{OE\overline{W}}$	Output Enable Time from \overline{WE}	1	—	1	—	ns
$t_{OD\overline{W}}$	Output Disable Time from \overline{WE}	—	5	—	6	ns

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

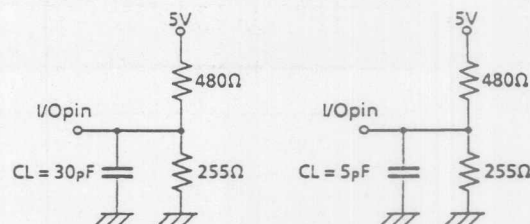
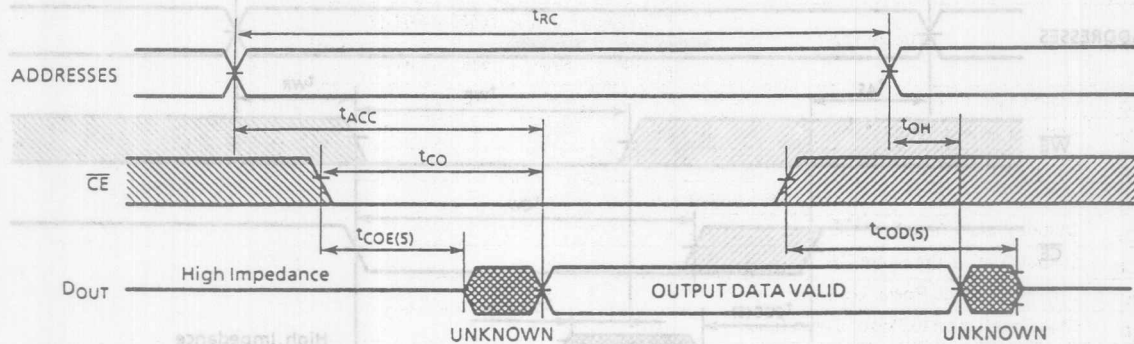
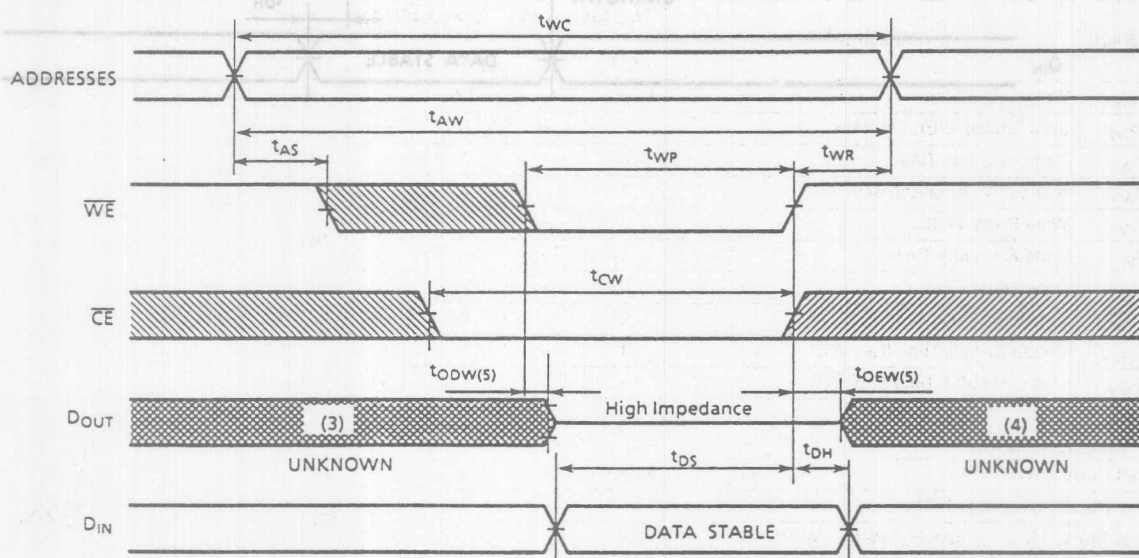
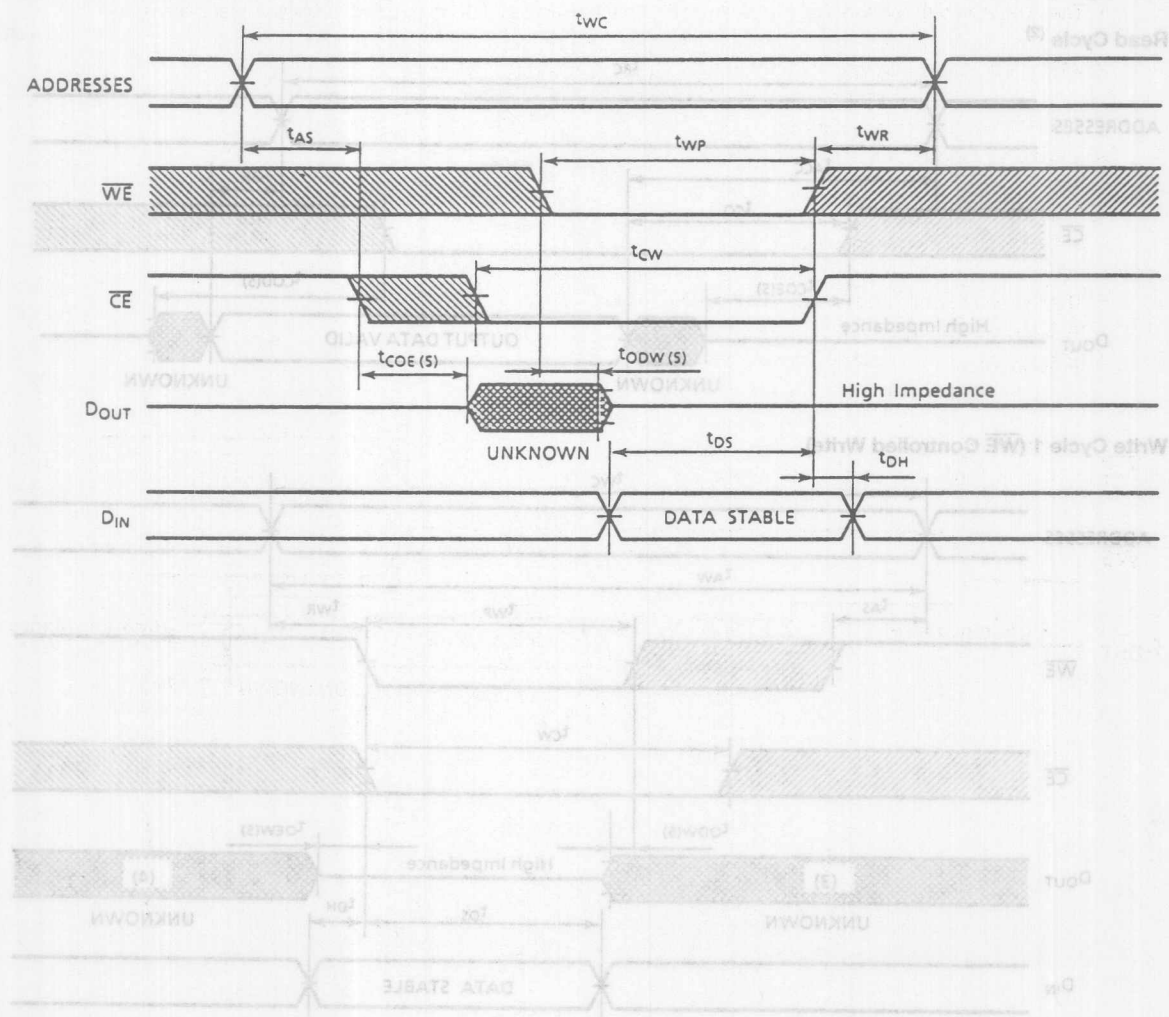
(For t_{COE} , t_{COD} , $t_{OE\overline{W}}$ and $t_{OD\overline{W}}$)

Figure 1.

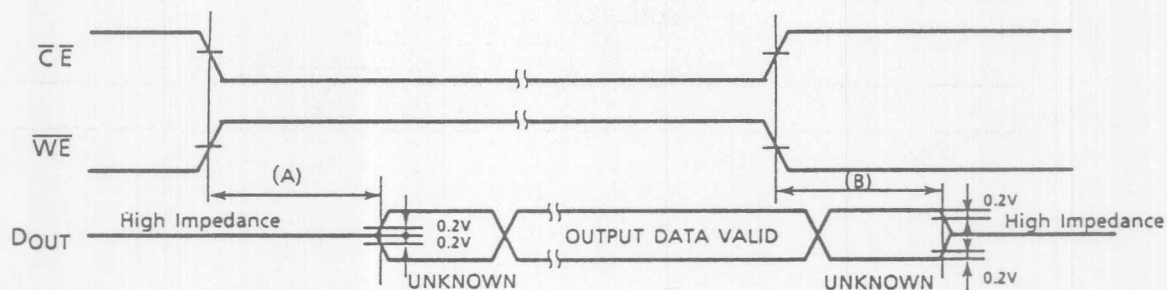
Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 (\overline{WE} Controlled Write)

Write Cycle 2 ($\overline{\text{CE}}$ Controlled Write)

Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{COE} , $t_{OE\overline{W}}$ Output Enable Time
 - (B) t_{COD} , $t_{OD\overline{W}}$ Output Disable Time



Notes

Notes:

1. The operating temperature (T_A) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. \overline{WE} is high for read cycles.

3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs

remain in a high impedance state.

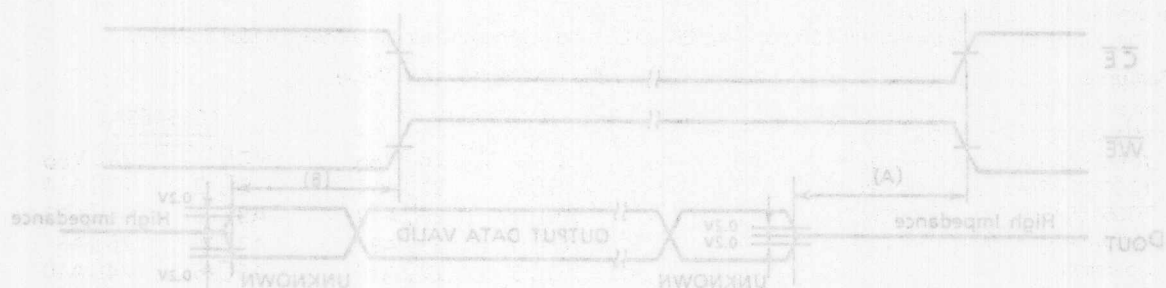
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs

remain in a high impedance state.

5. The following parameters are measured using the load shown in Fig. 1.

(A) t_{OE} low ... Output Enable Time

(B) t_{OD} low ... Output Disable Time



TC55465AP/AJ-15/20/25/35

SILICON GATE CMOS

65,536 WORD x 4 BIT CMOS STATIC RAM

Description

The TC55465AP/AJ is a 262,144 bit high speed CMOS static random access memory organized as 65,536 words by 4 bits and operated from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC55465AP/AJ features low power dissipation when the device is deselected using chip enable (\overline{CE}) and has an output enable input (\overline{OE}) for fast memory access. Also, the device power between memory accesses is reduced by an automatic power down circuit.

The TC55465AP/AJ is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC55465AP/AJ is available in a 300mil width, 28-pin DIP and SOJ suitable for high density surface assembly.

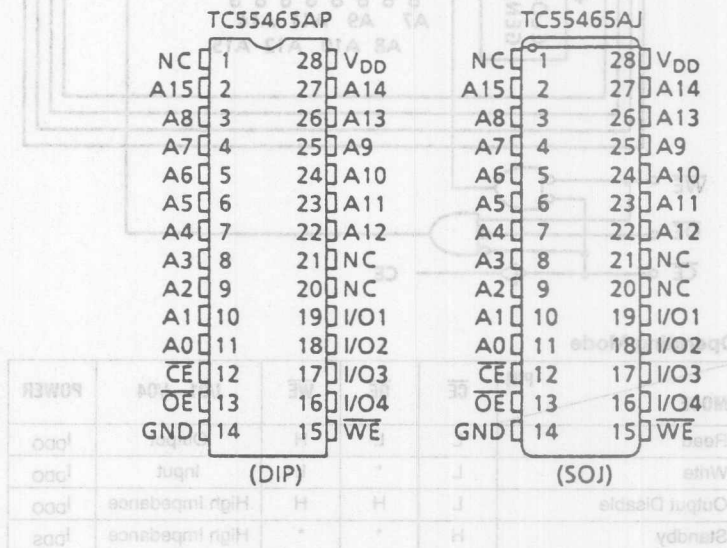
Features

- Fast access time
 - TC55465AP/AJ-15 15ns (max.)
 - TC55465AP/AJ-20 20ns (max.)
 - TC55465AP/AJ-25 25ns (max.)
 - TC55465AP/AJ-35 35ns (max.)
- Low power dissipation
 - Operation:
 - TC55465AP/AJ-15 120mA (max.)
 - TC55465AP/AJ-20 120mA (max.)
 - TC55465AP/AJ-25 120mA (max.)
 - TC55465AP/AJ-35 100mA (max.)
 - Standby: 1mA (max.)
- Single 5V power supply: $5V \pm 10\%$
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Package:
 - TC55465AP: DIP28-P-300B
 - TC55465AJ: SOJ28-P-300A

Pin Names

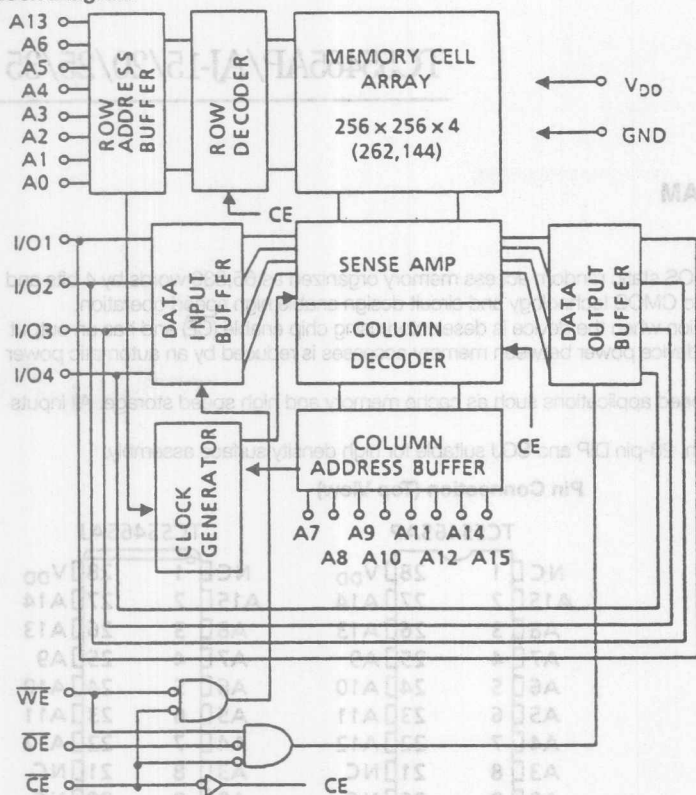
A0 ~ A15	Address Inputs
I/O1 ~ I/O4	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
NC	No Connection

Pin Connection (Top View)



SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{in}	Input Voltage	-0.5 ~ 7.0	V
V_{out}	Output Voltage	-0.5 ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{SDR}	Soldering Temperature - Time	260 ± 10	$^{\circ}C \cdot sec$
T_{STG}	Storage Temperature	-65 ~ 100	$^{\circ}C$
T_{OPR}	Operating Temperature	-10 ~ 65	$^{\circ}C$

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	\overline{WE}	I/O1 ~ I/O4	POWER
Read		L	L	H	Output	I_{DDO}
Write		L	*	L	Input	I_{DDO}
Output Disable		L	H	H	High Impedance	I_{DDO}
Standby		H	*	*	High Impedance	I_{DDs}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

* -3V with a pulse width of 10ns

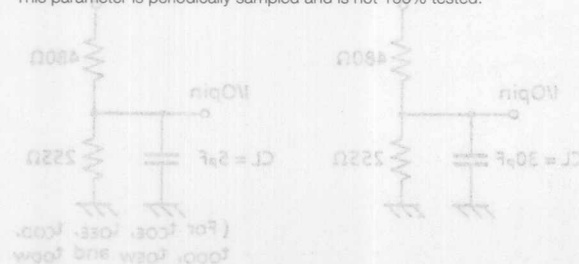
DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	8	—	—	mA
I_{DDO}	Operating Current	$t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE} = V_{IL}$ Other Inputs = V_{IH}/V_{IL}	-15	—	—	mA
			-20	—	—	
			-25	—	—	
			-35	—	—	
I_{DSD1}	Standby Current	$t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE} = V_{IH}$ Other Inputs = V_{IH}/V_{IL}	-15	—	—	mA
			-20	—	—	
			-25	—	—	
			-35	—	—	
I_{DSD2}		$\overline{CE} = V_{DD} - 0.2V$ Other Inputs = $V_{DD} - 0.2V$ or $0.2V$	—	—	1	mA

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
C_{IO}	Input/Output Capacitance	$V_{IO} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.



AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55465AP/AJ-15		TC55465AP/AJ-20		TC55465AP/AJ-25		TC55465AP/AJ-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	ns
t_{ACC}	Address Access Time	—	15	—	20	—	25	—	35	ns
t_{CO}	\overline{CE} Access Time	—	15	—	20	—	25	—	35	ns
t_{OE}	\overline{OE} Access Time	—	8	—	10	—	12	—	15	ns
t_{OH}	Output Data Hold Time from Address Change	5	—	5	—	5	—	5	—	ns
t_{COE}	Output Enable Time from \overline{CE}	5	—	5	—	5	—	5	—	ns
t_{COD}	Output Disable Time from \overline{CE}	—	8	—	8	—	10	—	15	ns
t_{OEE}	Output Enable Time from \overline{OE}	1	—	1	—	1	—	1	—	ns
t_{ODO}	Output Disable Time from \overline{OE}	—	8	—	8	—	10	—	15	ns

Write Cycle

SYMBOL	PARAMETER	TC55465AP/AJ-15		TC55465AP/AJ-20		TC55465AP/AJ-25		TC55465AP/AJ-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	—	20	—	25	—	35	—	ns
t_{WP}	Write Pulse Width	10	—	11	—	13	—	18	—	ns
t_{AW}	Address Valid to End of Write	12	—	13	—	15	—	20	—	ns
t_{CW}	Chip Enable to End of Write	12	—	13	—	15	—	20	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DS}	Data Setup Time	8	—	10	—	12	—	15	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{OEW}	Output Enable Time from \overline{WE}	1	—	1	—	1	—	1	—	ns
t_{ODW}	Output Disable Time from \overline{WE}	—	8	—	8	—	10	—	15	ns

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

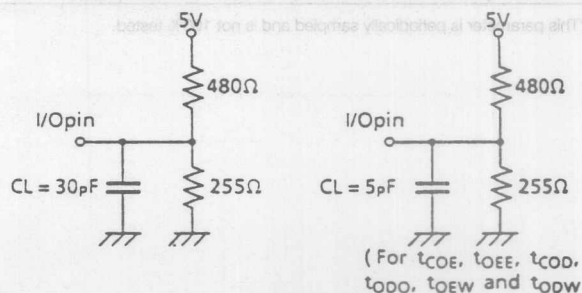
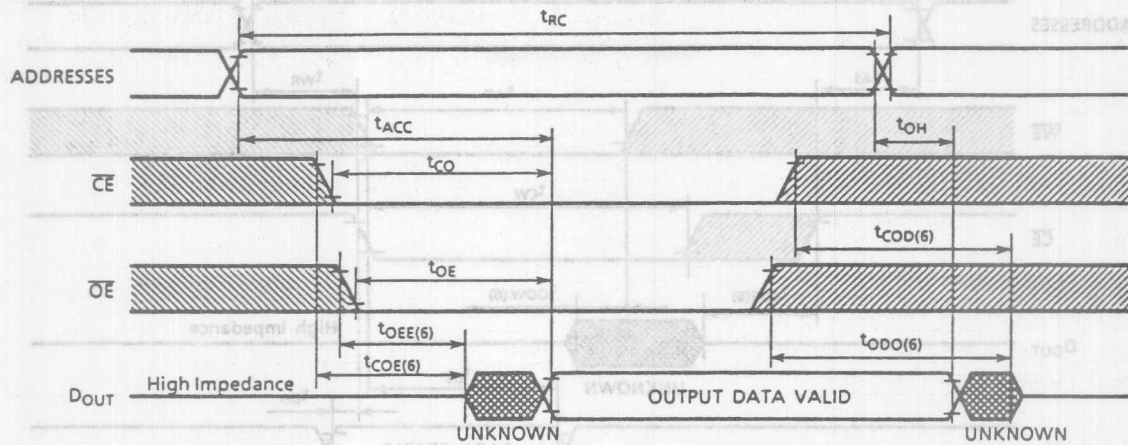
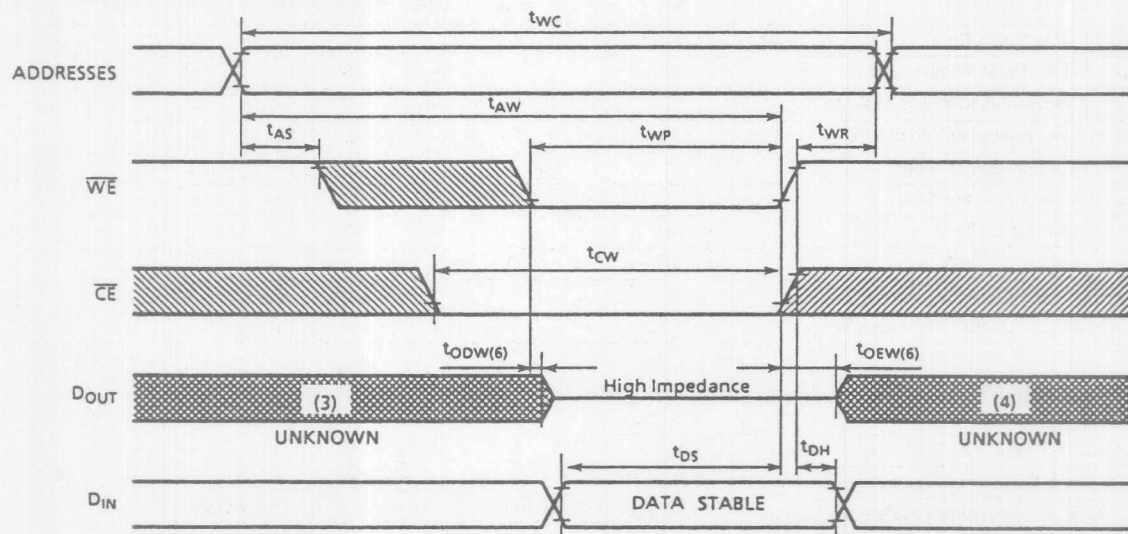
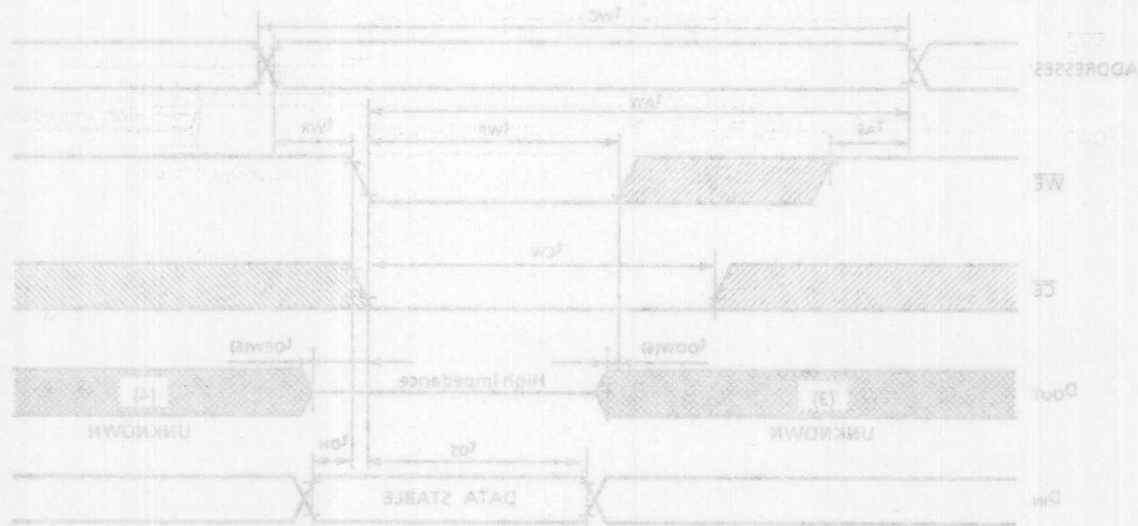
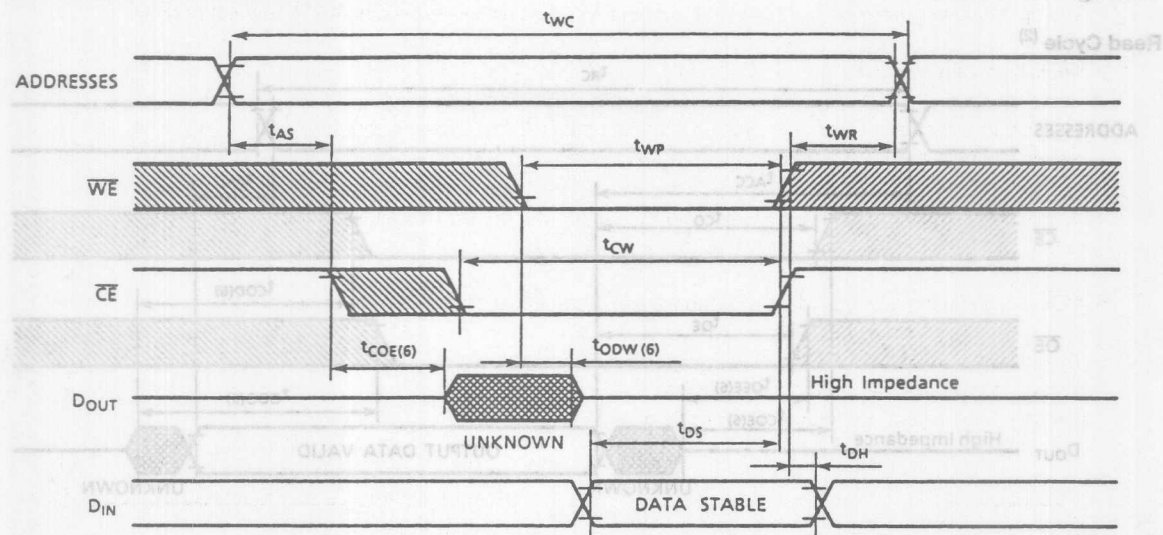


Figure 1.

Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled Write)

Write Cycle 2 ⁽⁵⁾ (\overline{CE} Controlled Write)



Notes

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. \overline{WE} is high for read cycles.

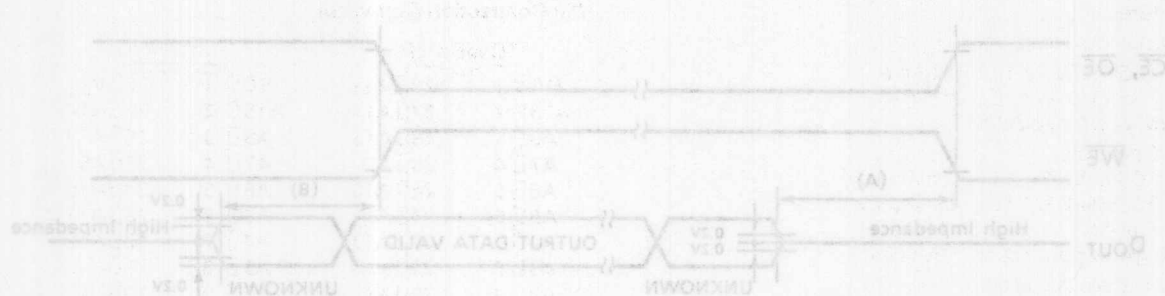
3. If the \overline{OE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.

4. If the \overline{OE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.

5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.

6. The following parameters are measured using the load shown in Fig. 1.

(A) $t_{OE} \text{ low} \rightarrow \text{high}$ Output Enable Time
(B) $t_{OE} \text{ high} \rightarrow \text{low}$ Output Disable Time



TC55B465P/J-10/12

SILICON GATE BiCMOS

65,536 WORD x 4 BIT BiCMOS STATIC RAM

Description

The TC55B465P/J is a 262,144 bit high speed BiCMOS static random access memory organized as 65,536 words by 4 bits and operated from a single 5V supply. Toshiba's BiCMOS technology and advanced circuit design enable high speed operation.

The TC55B465P/J features low power dissipation when the device is deselected using chip enable (CE) and has an output enable input (OE) for fast memory access.

The TC55B465P/J is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC55B465P/J is available in a 300mil width, 28-pin DIP and SOJ suitable for high density surface assembly.

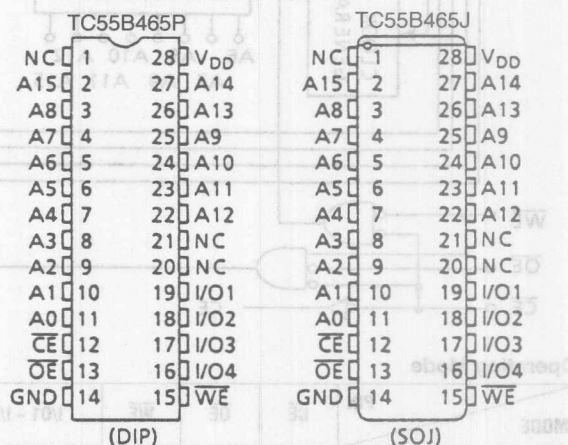
Features

- Fast access time
 - TC55B465P/J-10 10ns (max.)
 - TC55B465P/J-12 12ns (max.)
- Low power dissipation
 - Operation:
 - TC55B465P/J-10 140mA (max.)
 - TC55B465P/J-12 140mA (max.)
 - Standby: 15mA (max.)
- Single 5V power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Package:
 - TC55B465P: DIP28-P-300B
 - TC55B465J: SOJ28-P-300A

Pin Names

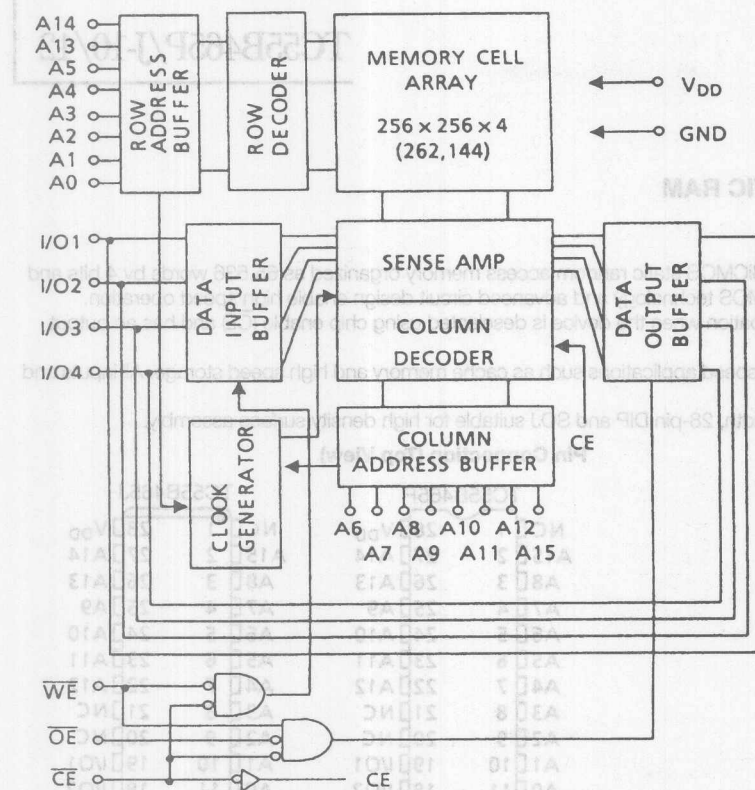
A0 ~ A15	Address Inputs
I/O1 ~ I/O4	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
NC	No Connection

Pin Connection (Top View)



SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 - 7.0	V
V_{IN}	Input Voltage	-0.5 - 7.0	V
V_{IO}	Input/Output Voltage	-0.5 - $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T solder	Soldering Temperature - Time	260 ± 10	°C - sec
T stor	Storage Temperature	-65 - 120	°C
T op	Operating Temperature	-10 - 85	°C

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	\overline{WE}	I/O1 - I/O4	POWER
Read		L	L	H	Output	I_{DDO}
Write		L	*	L	Input	I_{DDO}
Output Disable		L	H	H	High Impedance	I_{DDO}
Standby		H	*	*	High Impedance	I_{DD}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0 ~ 7.0	V
V_{IO}	Input/Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

* -3V with a pulse width of 10ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	—	—	-4	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	8	—	—	mA
I_{DDO}	Operating Current	$t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE} = V_{IL}$ Other Inputs = V_{IH}/V_{IL} , $I_{OUT} = 0\text{mA}$	—	—	140	mA
I_{DDs1}	Standby Current	$\overline{CE} = V_{IH}$ Other Inputs = V_{IH}/V_{IL}	—	—	30	mA
I_{DDs2}		$\overline{CE} = V_{DD} - 0.2\text{V}$ Other Inputs = $V_{DD} - 0.2\text{V}$ or 0.2V	—	—	15	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.

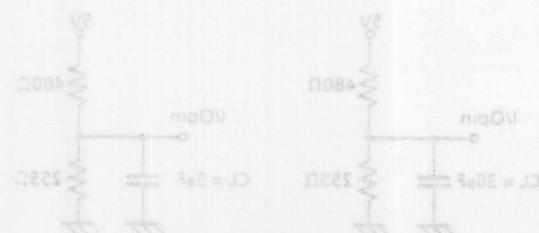


Figure 1

Fig. 1	Output Timing Measurement Reference Levels
1.5V	Input Timing Measurement Reference Levels
1.5V	Input Pulse Rise and Fall Time
2ns	Input Pulse Levels
3.0V/0.0V	AC Test Conditions

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55B465P/J-10		TC55B465P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	—	12	—	ns
t_{ACC}	Address Access Time	—	10	—	12	ns
t_{CO}	\overline{CE} Access Time	—	10	—	12	ns
t_{OE}	\overline{OE} Access Time	—	5	—	6	ns
t_{OH}	Output Data Hold Time from Address Change	3	—	3	—	ns
t_{COE}	Output Enable Time from \overline{CE}	3	—	3	—	ns
t_{COD}	Output Disable Time from \overline{CE}	—	5	—	6	ns
t_{OEE}	Output Enable Time from \overline{OE}	1	—	1	—	ns
t_{ODO}	Output Disable Time from \overline{OE}	—	5	—	6	ns
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	ns
t_{PD}	Chip Deselection to Power Down Time	—	10	—	12	ns

Write Cycle

SYMBOL	PARAMETER	TC55B465P/J-10		TC55B465P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	—	12	—	ns
t_{CW}	Chip Enable to End of Write	7	—	8	—	ns
t_{AS}	Address Setup Time	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	7	—	8	—	ns
t_{WP}	Write Pulse Width	6	—	7	—	ns
t_{WR}	Write Recovery Time	1	—	1	—	ns
t_{DS}	Data Setup Time	6	—	7	—	ns
t_{DH}	Data Hold Time	0	—	0	—	ns
t_{OEW}	Output Enable Time from \overline{WE}	1	—	1	—	ns
t_{ODW}	Output Disable Time from \overline{WE}	—	5	—	6	ns

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

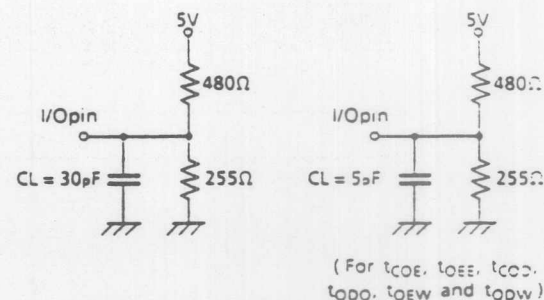
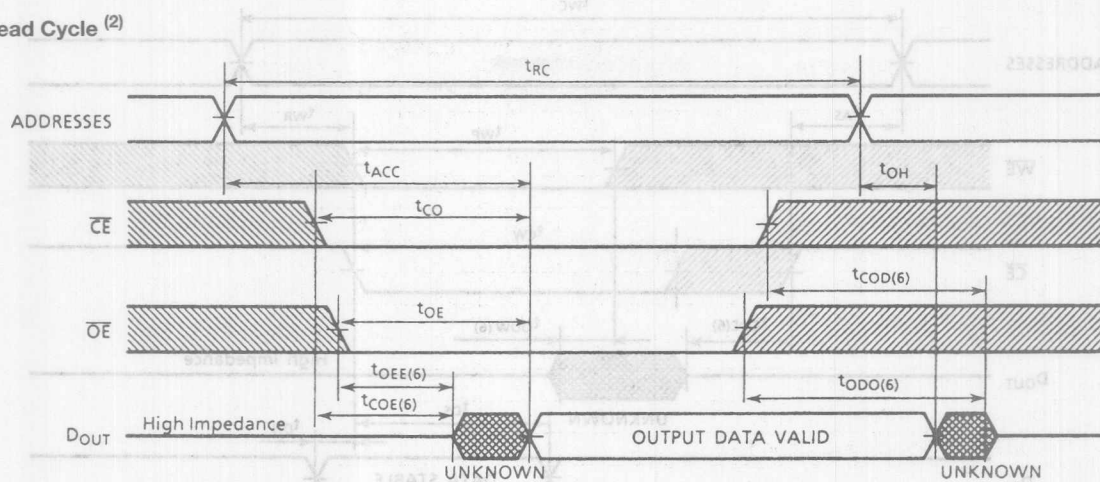
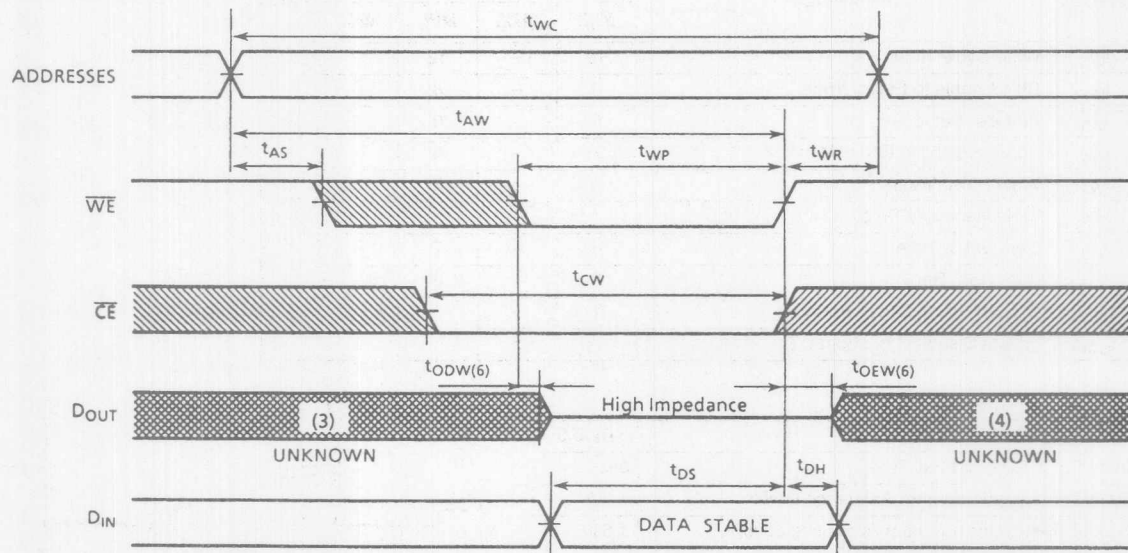
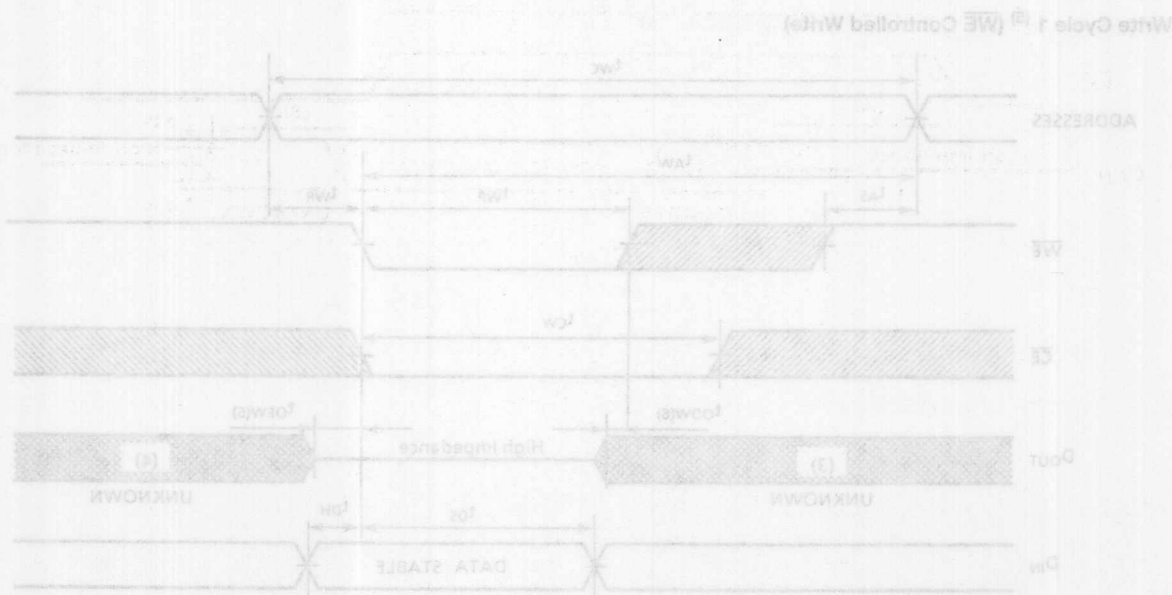
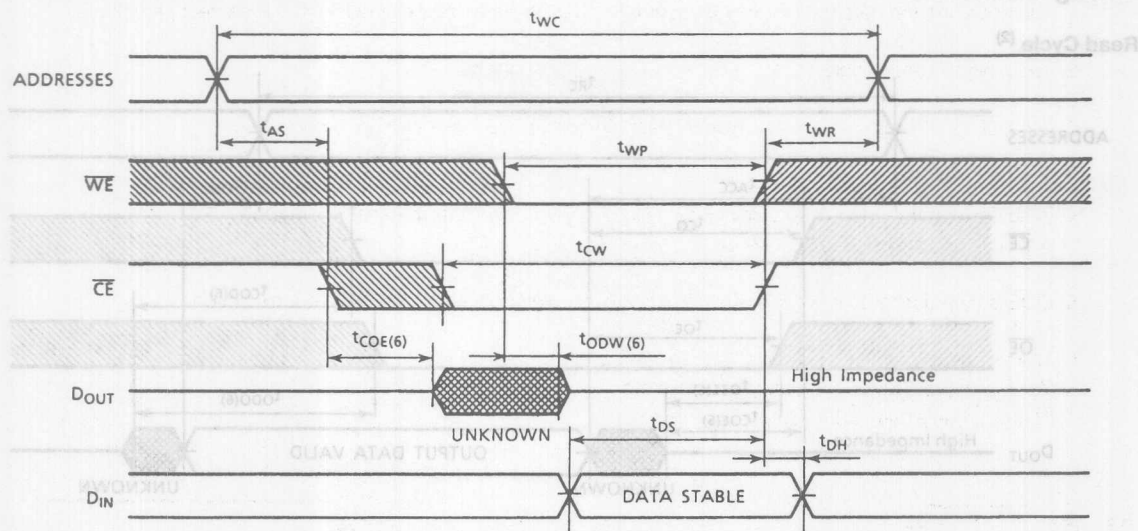


Figure 1.

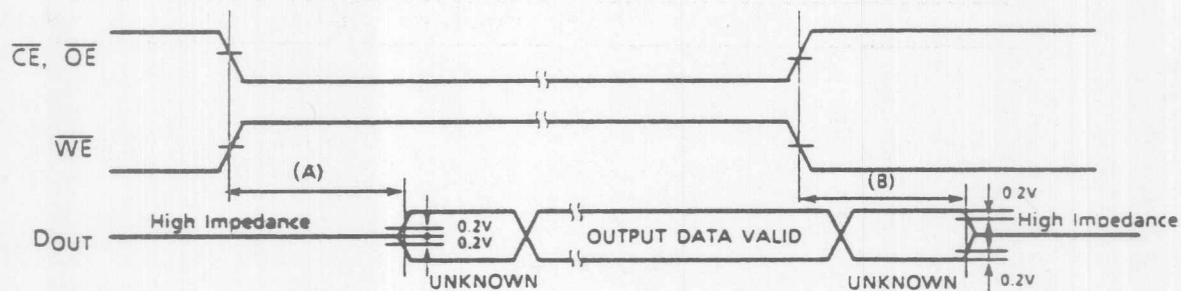
Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled Write)

Write Cycle 2 ⁽⁵⁾ ($\overline{\text{CE}}$ Controlled Write)

Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{COE} , t_{OEE} , $t_{OE\overline{W}}$ Output Enable Time
 - (B) t_{COD} , t_{ODO} , $t_{OD\overline{W}}$ Output Disable Time



Notes

Notes:

1. The operating temperature (T_A) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. \overline{WE} is high for read cycles.

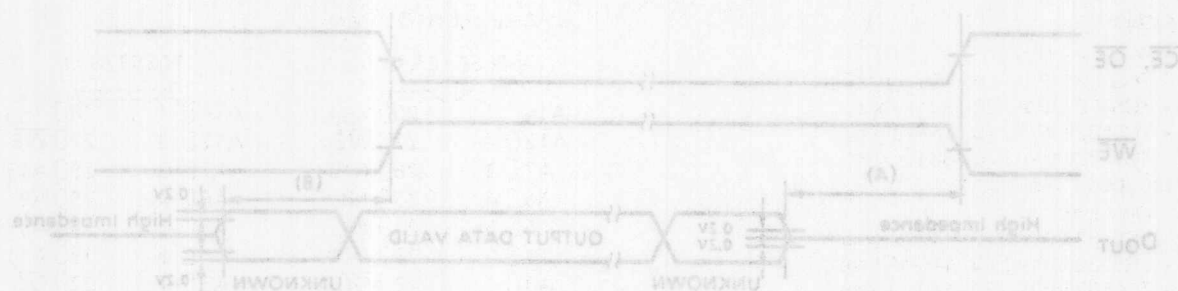
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.

4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.

5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.

6. The following parameters are measured using the load shown in Fig. 1.

(A) t_{OE} low-to-low, Output Enable Time
(B) t_{OD} low-to-low, Output Disable Time



TC55328AP/AJ-15/20/25/35

SILICON GATE CMOS

32,768 WORD x 8 BIT CMOS STATIC RAM

Description

The TC55328AP/AJ is a 262,144 bit high speed CMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC55328AP/AJ features low power dissipation when the device is deselected using chip enable (\overline{CE}) and has an output enable input (\overline{OE}) for fast memory access. Also, the device power between memory accesses is reduced by an automatic power down circuit.

The TC55328AP/AJ is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC55328AP/AJ is available in a 300mil width, 28-pin DIP and SOJ suitable for high density surface assembly.

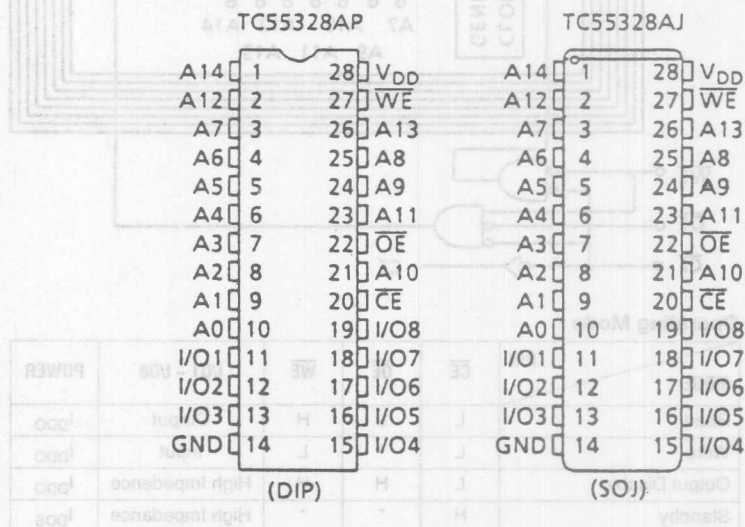
Features

- Fast access time
 - TC55328AP/AJ-15 15ns (max.)
 - TC55328AP/AJ-20 20ns (max.)
 - TC55328AP/AJ-25 25ns (max.)
 - TC55328AP/AJ-35 35ns (max.)
- Low power dissipation
 - Operation:
 - TC55328AP/AJ-15 140mA (max.)
 - TC55328AP/AJ-20 140mA (max.)
 - TC55328AP/AJ-25 140mA (max.)
 - TC55328AP/AJ-35 120mA (max.)
 - Standby: 1mA (max.)
- Single 5V power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Package:
 - TC55328AP: DIP28-P-300B
 - TC55328AJ: SOJ28-P-300A

Pin Names

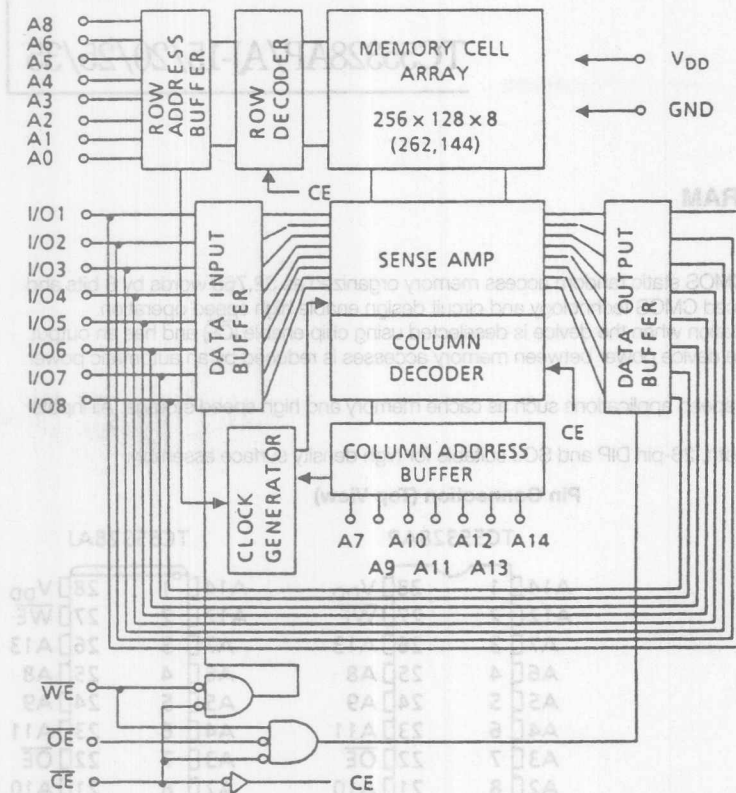
A0 ~ A14	Address Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V _{DD}	Power (+5V)
GND	Ground

Pin Connection (Top View)



SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 - 7.0	V
V _{IN}	Input Voltage	-2.0 - 7.0	V
V _{IO}	Input/Output Voltage	-0.5 - V _{DD} + 0.5	V
P _D	Power Dissipation	1.0	W
T _{STG}	Storage Temperature	-55 - 150	°C
T _{OP}	Operating Temperature	-10 - 65	°C

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	\overline{WE}	I/O1 ~ I/O8	POWER
Read		L	L	H	Output	I_{DDO}
Write		L	*	L	Input	I_{DDO}
Output Disable		L	H	H	High Impedance	I_{DDO}
Standby		H	*	*	High Impedance	I_{DPS}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0 ~ 7.0	V
V_{IO}	Input/Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

* -3V with a pulse width of 10ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1	μA
I_{OH}	Output High Voltage	$V_{OH} = 2.4V$	-4	—	—	mA
I_{OL}	Output Low Voltage	$V_{OL} = 0.4V$	8	—	—	mA
I_{DDO}	Operating Current	$t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE} = V_{IL}$ Other Inputs = V_{IH}/V_{IL}	-15	—	—	mA
			-20	—	—	
			-25	—	—	
			-35	—	—	
I_{DDs1}	Standby Current	$t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE} = V_{IH}$ Other Inputs = V_{IH}/V_{IL}	-15	—	—	mA
			-20	—	—	
			-25	—	—	
			-35	—	—	
I_{DDs2}		$\overline{CE} = V_{DD} - 0.2V$ Other Inputs = $V_{DD} - 0.2V$ or $0.2V$	—	—	—	1

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55328AP/AJ-15		TC55328AP/AJ-20		TC55328AP/AJ-25		TC55328AP/AJ-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	
t_{ACC}	Address Access Time	—	15	—	20	—	25	—	35	
t_{CO}	\overline{CE} Access Time	—	15	—	20	—	25	—	35	
t_{OE}	\overline{OE} Access Time	—	8	—	10	—	12	—	15	
t_{OH}	Output Data Hold Time from Address Change	5	—	5	—	5	—	5	—	ns
t_{COE}	Output Enable Time from \overline{CE}	5	—	5	—	5	—	5	—	
t_{COD}	Output Disable Time from \overline{CE}	—	8	—	8	—	10	—	15	
t_{OEE}	Output Enable Time from \overline{OE}	1	—	1	—	1	—	1	—	
t_{ODO}	Output Disable Time from \overline{OE}	—	8	—	8	—	10	—	15	

Write Cycle

SYMBOL	PARAMETER	TC55328AP/AJ-15		TC55328AP/AJ-20		TC55328AP/AJ-25		TC55328AP/AJ-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	—	20	—	25	—	35	—	
t_{WP}	Write Pulse Width	10	—	11	—	13	—	18	—	
t_{AW}	Address Valid to End of Write	12	—	13	—	15	—	20	—	
t_{CW}	Chip Enable to End of Write	12	—	13	—	15	—	20	—	
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	
t_{DS}	Data Setup Time	8	—	10	—	12	—	15	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	
t_{OEW}	Output Enable Time from \overline{WE}	1	—	1	—	1	—	1	—	
t_{ODW}	Output Disable Time from \overline{WE}	—	8	—	8	—	10	—	15	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

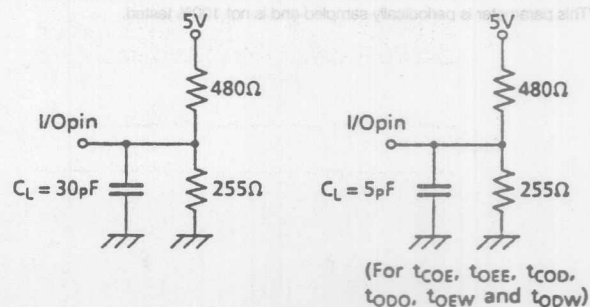
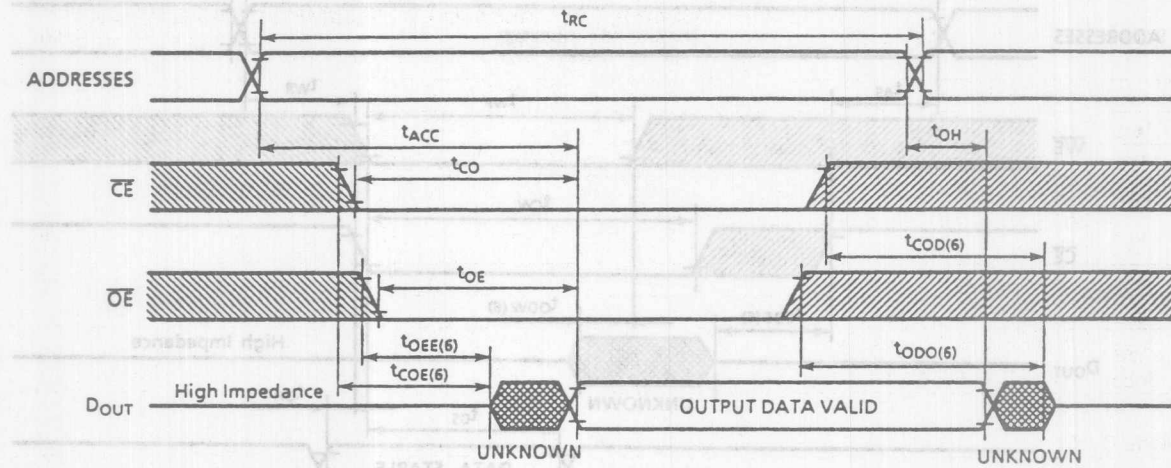
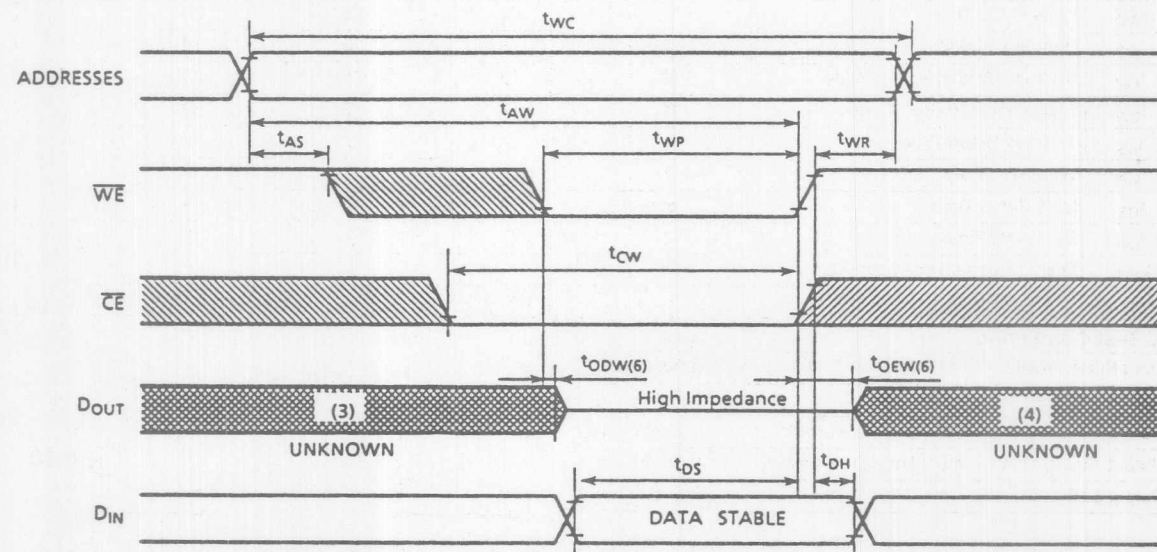
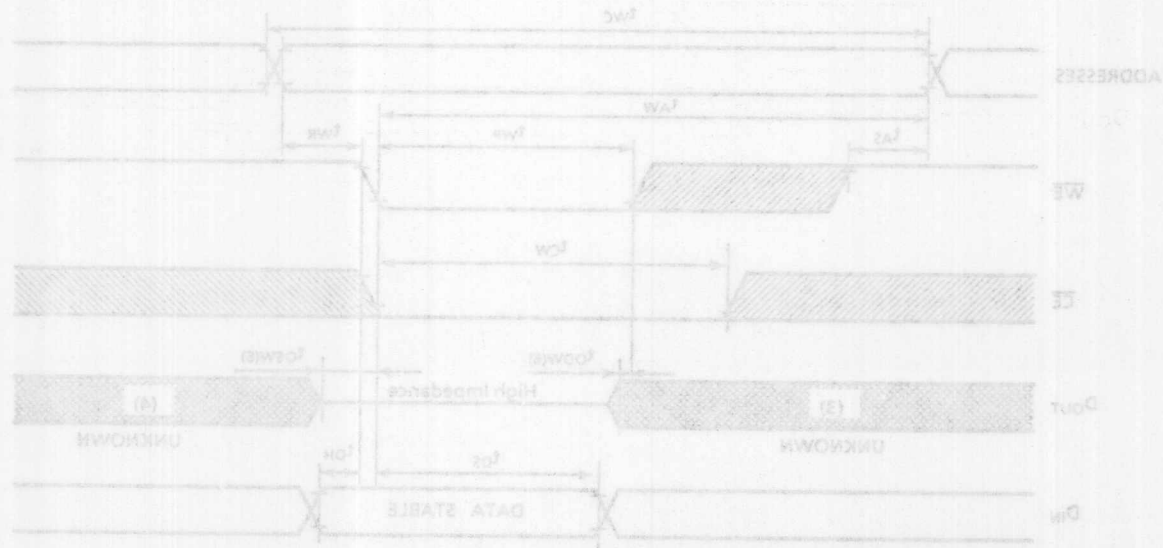
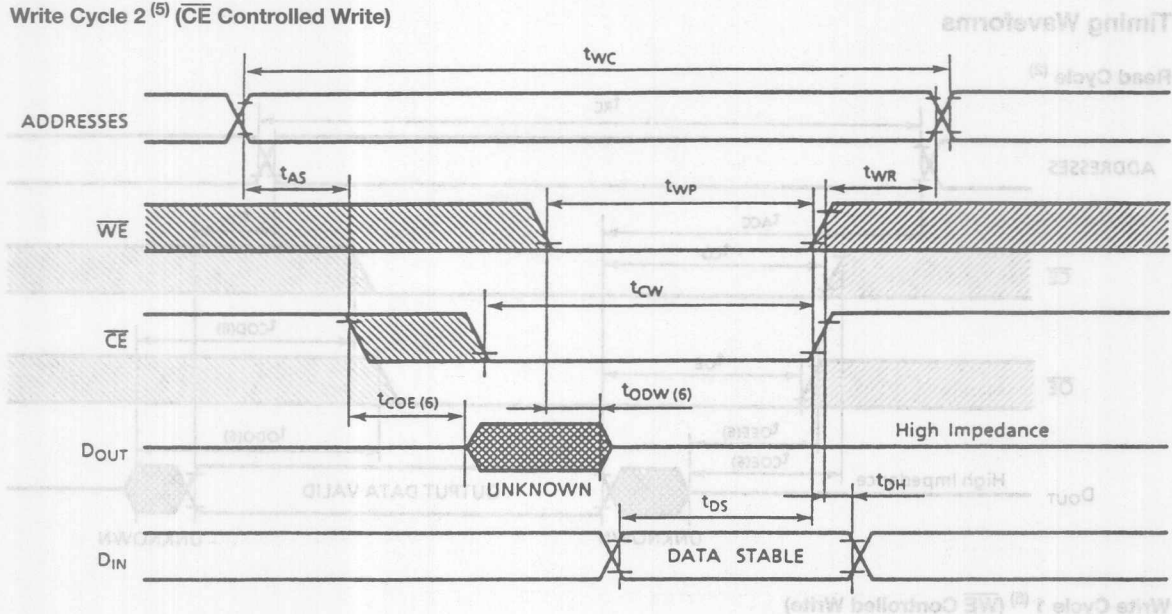


Figure 1.

Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled Write)

Write Cycle 2⁽⁵⁾ ($\overline{\text{CE}}$ Controlled Write)

Notes

1. The operating temperature (T_A) is guaranteed with turnover at flow exceeding 400 linear feet per minute.

2. \overline{WE} is high for read cycles.

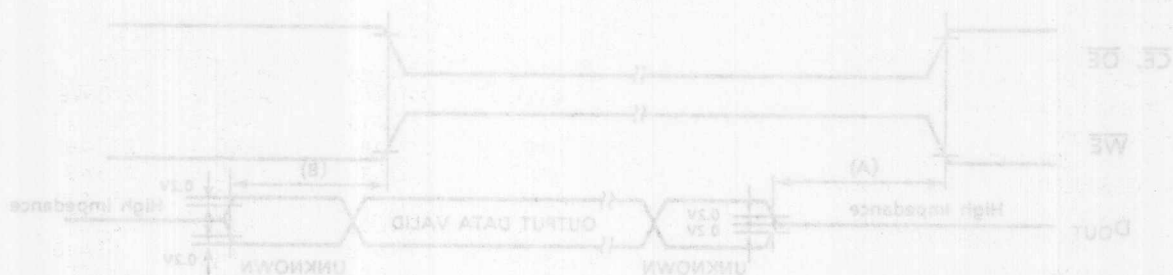
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.

4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.

5. If \overline{CE} is high during a write cycle, the outputs are in a high impedance state during the period.

6. The following parameters are measured using the load shown in Fig. 1.

(A) Access Time: Output Enable Time
(B) Output Disable Time: Output Disable Time



TC55B328P/J-10/12

SILICON GATE BiCMOS

32,768 WORD x 8 BIT BiCMOS STATIC RAM

Description

The TC55B328P/J is a 262,144 bit high speed BiCMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V supply. Toshiba's BiCMOS technology and advanced circuit design enable high speed operation.

The TC55B328P/J features low power dissipation when the device is deselected using chip enable (\overline{CE}) and has an output enable input (\overline{OE}) for fast memory access.

The TC55B328P/J is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC55B328P/J is available in a 300mil width, 28-pin DIP and SOJ suitable for high density surface assembly.

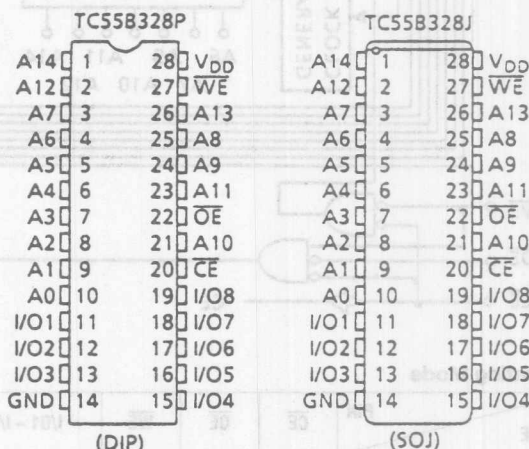
Features

- Fast access time
 - TC55B328P/J-10 10ns (max.)
 - TC55B328P/J-12 12ns (max.)
- Low power dissipation
 - Operation:
 - TC55B328P/J-10 170mA (max.)
 - TC55B328P/J-12 170mA (max.)
 - Standby: 15mA (max.)
- Single 5V power supply: 5V \pm 10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Package:
 - TC55B328P: DIP28-P-300B
 - TC55B328J: SOJ28-P-300A

Pin Names

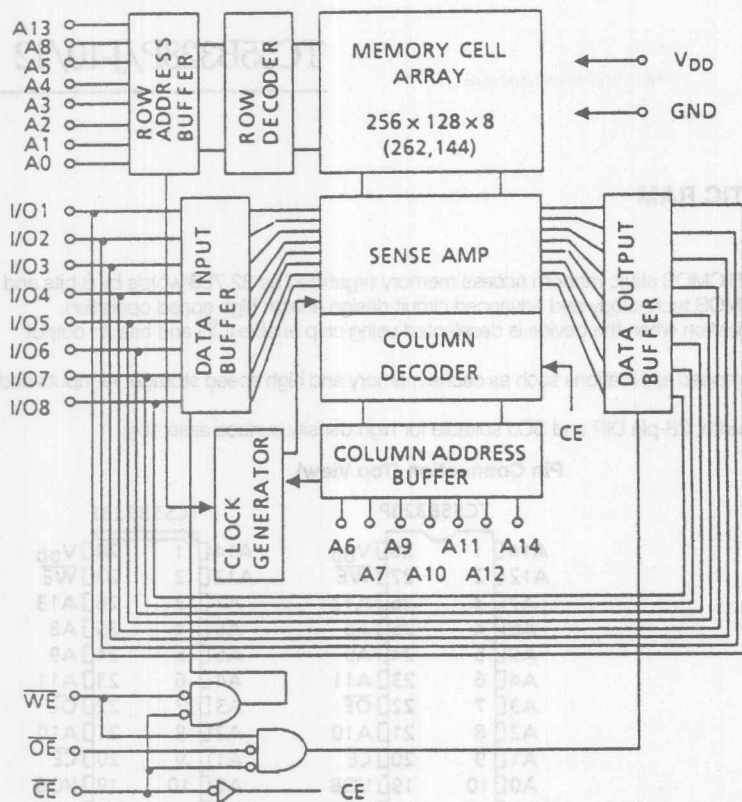
A0 ~ A14	Address Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V _{DD}	Power (+5V)
GND	Ground

Pin Connection (Top View)



UNIT	RATING	ITEM	SYMBOL
V	0.3 - 7.0	Power Supply Voltage	V _{DD}
V	5.0 - 7.0	Input Voltage	V _{IN}
V	-0.5* - V _{DD} + 0.5	Input/Output Voltage	V _{IO}
W	1.0	Power Dissipation	P _D
°C	55 - 150	Storage Temperature	T _{STG}
°C	-10 - 85	Operating Temperature	T _{OP}

Block Diagram



Operating Mode

MODE \ PIN	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O1 ~ I/O8	POWER
Read	L	L	H	Output	I _{DDO}
Write	L	*	L	Input	I _{DDO}
Output Disable	L	H	H	High Impedance	I _{DDO}
Standby	H	*	*	High Impedance	I _{DDs}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V _{IN}	Input Voltage	-2.0 ~ 7.0	V
V _{I/O}	Input/Output Voltage	-0.5* ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-65 ~ 150	°C
T _{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

* -3V with a pulse width of 10ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	8	—	—	mA
I_{DDO}	Operating Current	$t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE} = V_{IL}$ Other Inputs = V_{IH}/V_{IL} , $I_{OUT} = 0\text{mA}$	—	—	170	mA
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$ Other Inputs = V_{IH}/V_{IL}	—	—	30	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2\text{V}$ Other Inputs = $V_{DD} - 0.2\text{V}$ or 0.2V	—	—	15	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
C_{IO}	Input/Output Capacitance	$V_{IO} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.



Figure 1

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55B328P/J-10		TC55B328P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	—	12	—	
t_{ACC}	Address Access Time	—	10	—	12	
t_{CO}	\overline{CE} Access Time	—	10	—	12	
t_{OE}	\overline{OE} Access Time	—	5	—	6	
t_{OH}	Output Data Hold Time from Address Change	3	—	3	—	
t_{COE}	Output Enable Time from \overline{CE}	3	—	3	—	ns
t_{COD}	Output Disable Time from \overline{CE}	—	5	—	6	
t_{OEE}	Output Enable Time from \overline{OE}	1	—	1	—	
t_{ODO}	Output Disable Time from \overline{OE}	—	5	—	6	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	10	—	12	

Write Cycle

SYMBOL	PARAMETER	TC55B328P/J-10		TC55B328P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	—	12	—	
t_{CW}	Chip Enable to End of Write	7	—	8	—	
t_{AS}	Address Setup Time	0	—	0	—	
t_{AW}	Address Valid to End of Write	7	—	8	—	
t_{WP}	Write Pulse Width	6	—	7	—	ns
t_{WR}	Write Recovery Time	1	—	1	—	
t_{DS}	Data Setup Time	6	—	7	—	
t_{DH}	Data Hold Time	0	—	0	—	
t_{OEw}	Output Enable Time from \overline{WE}	1	—	1	—	
t_{ODw}	Output Disable Time from \overline{WE}	—	5	—	6	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

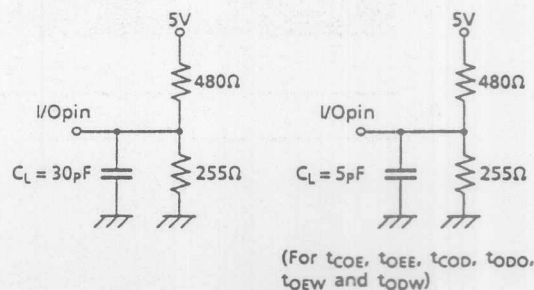
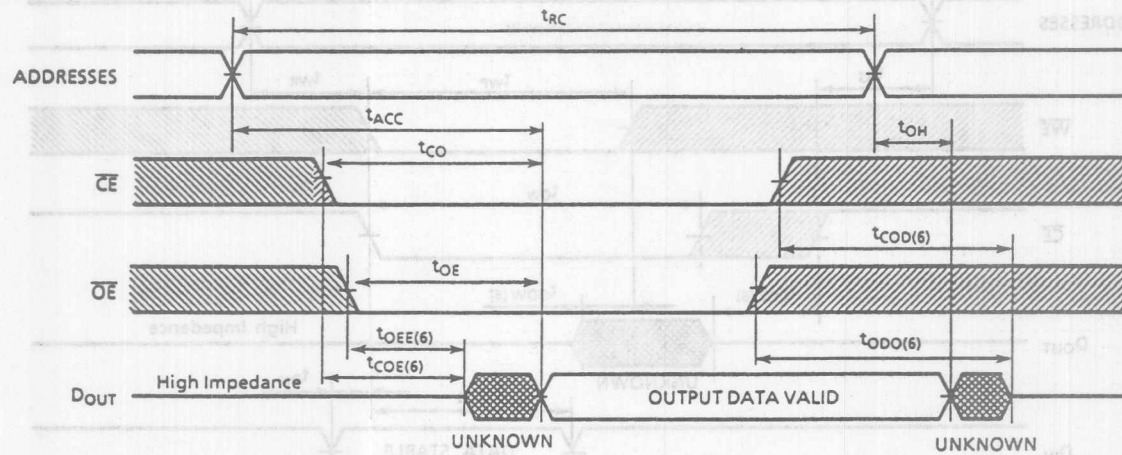
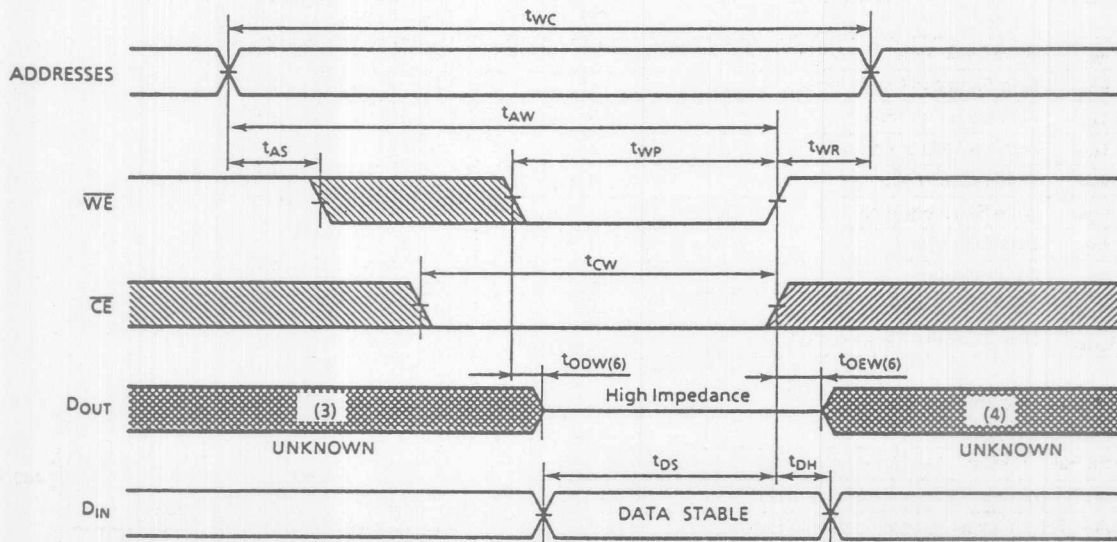
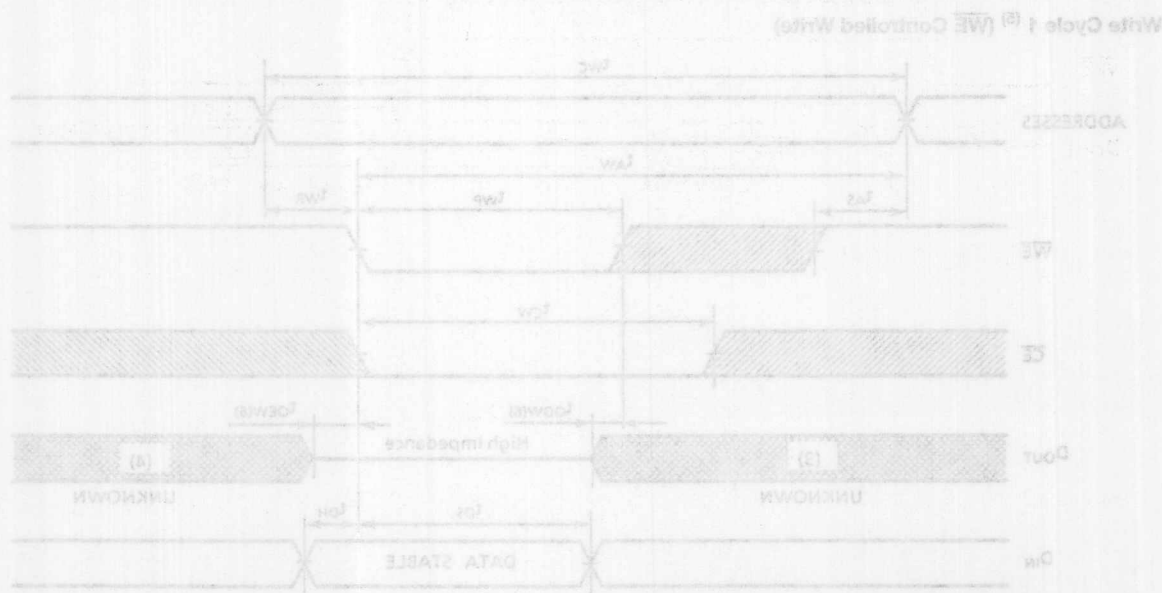
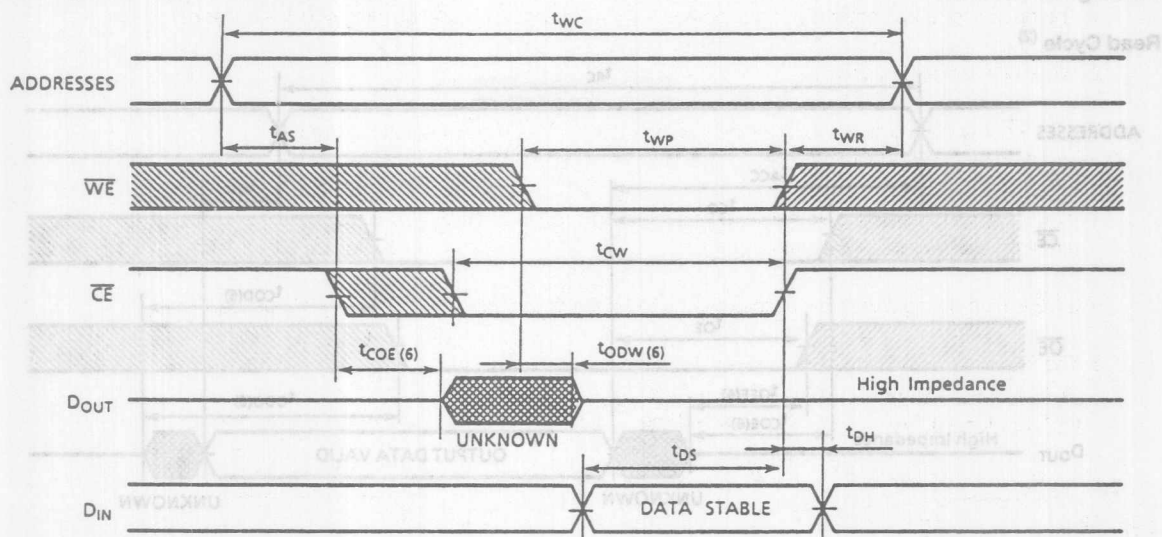


Figure 1.

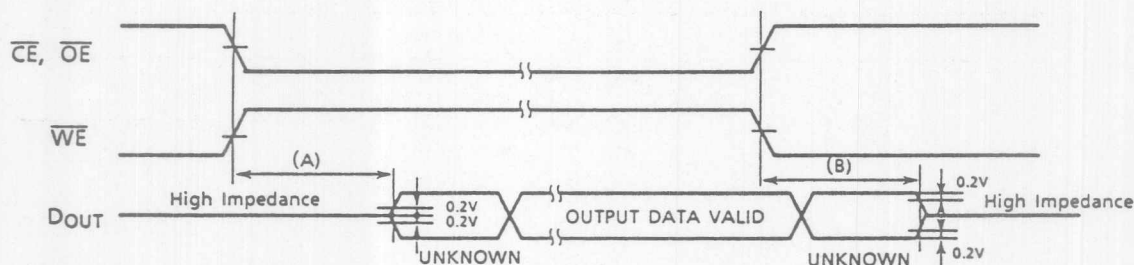
Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled Write)

Write Cycle 2 ⁽⁵⁾ ($\overline{\text{CE}}$ Controlled Write)

Notes:

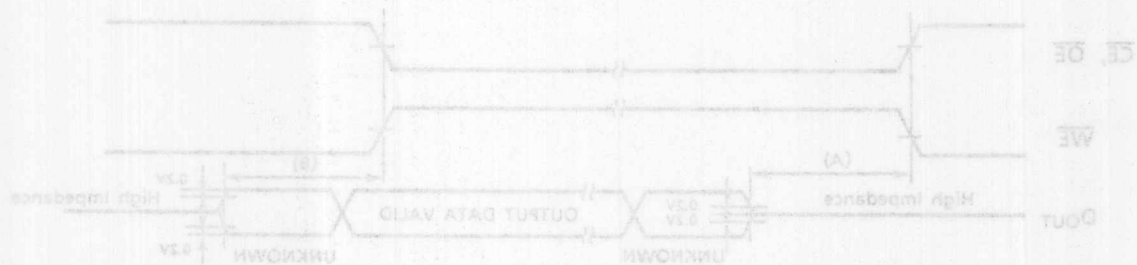
1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{COE} , t_{OEE} , $t_{OE\overline{W}}$ Output Enable Time
 - (B) t_{COD} , t_{ODO} , $t_{OD\overline{W}}$ Output Disable Time



Notes

Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 100 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{CE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 (A) t_{OE} low-to-low ... Output Enable Time
 (B) t_{OD} low-to-low ... Output Disable Time



TC55V328J-20/25/35

PRELIMINARY

SILICON GATE CMOS

32,768 WORD x 8 BIT CMOS STATIC RAM

Description

The TC55V328J is a 262,144 bit CMOS high speed static random access memory organized as 32,768 words by 8 bits and designed to operate from a single 3.3V supply. Toshiba's advanced CMOS technology and circuit design enable high speed, low voltage operation.

The TC55V328J features low power dissipation when the SRAM is deselected using chip enable (\overline{CE}) and has an output enable input (\overline{OE}) for fast memory access. It is suitable for use in high speed applications such as cache memory. All inputs and outputs are LVTTL (low voltage TTL) compatible.

The TC55V328J is available in a 28-pin, 300mil SOJ package suitable for high density assembly.

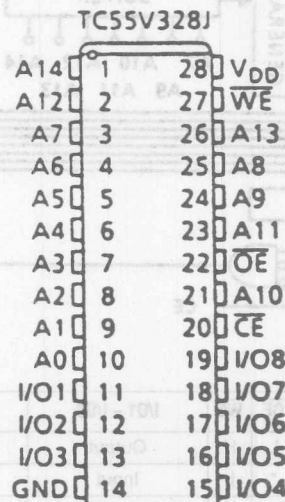
Features

- Fast access time
 - TC55V328J-20 20ns (max.)
 - TC55V328J-25 25ns (max.)
 - TC55V328J-35 35ns (max.)
- Low power dissipation
 - Operation:
 - TC55V328J-20 70mA (max.)
 - TC55V328J-25 70mA (max.)
 - TC55V328J-35 70mA (max.)
 - Standby: 300 μ A (max.)
- Fully static operation
- Single power supply: 3.3V \pm 0.3V
- Output buffer control: \overline{OE}
- Inputs and outputs:
 - LVTTL compatible
- Package:
 - TC55V328J: SOJ28-P-300A

Pin Names

A0 ~ A14	Address Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V _{DD}	Power (+3.3V)
GND	Ground

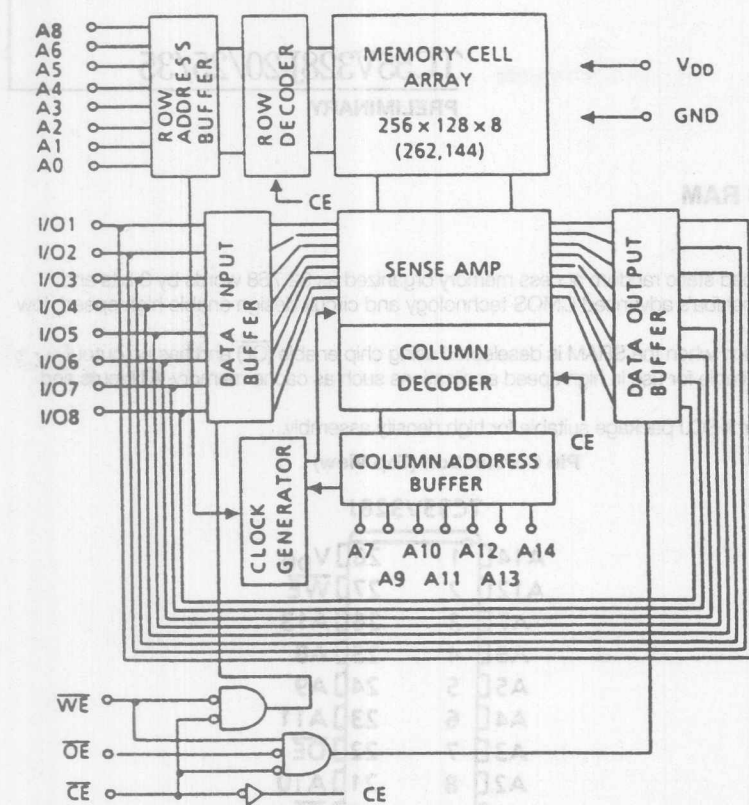
Pin Connection (Top View)



(SOJ)

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ +4.5	V
V _{IN}	Input Voltage	-0.5 ~ +4.5	V
V _{IO}	Input/Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	0.5	W
T _{storage}	Storage Temperature	-55 ~ +125	°C
T _{oper}	Operating Temperature	-10 ~ +85	°C
T _{sol}	Soldering Temperature	260 ~ 300	°C
		10 sec	

Block Diagram



Operating Mode

MODE	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O1 ~ I/O8	POWER
Read	L	L	H	Output	I _{DDO}
Write	L	*	L	Input	I _{DDO}
Output Disable	L	H	H	High Impedance	I _{DDO}
Standby	H	*	*	High Impedance	I _{DDS}

* High or Low

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 4.6	V
V _{IN}	Input Voltage	-0.5* ~ 4.6	V
V _{I/O}	Input/Output Voltage	-0.5* ~ V _{DD} + 0.5**	V
P _D	Power Dissipation	0.5	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-65 ~ 150	°C
T _{OPR}	Operating Temperature	-10 ~ 85	°C

* -2.0V with a pulse width of 10ns

**V_{DD} = 1.5V with a pulse width of 10ns

AS1420T

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V _{IH}	Input High Voltage	2.0	—	V _{DD} + 0.3**	V
V _{IL}	Input Low Voltage	-0.3*	—	0.8	V

* -1.5V with a pulse width of 10ns
**V_{DD} + 1.0V with a pulse width of 10ns

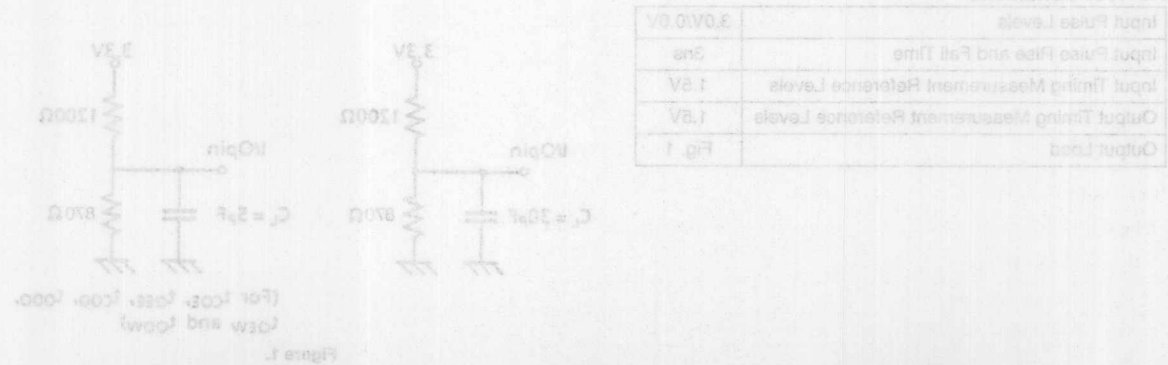
DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 3.3V±0.3V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}	—	—	±1	μA
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, V _{OUT} = 0 ~ V _{DD}	—	—	±1	μA
V _{OH}	Output High Voltage	I _{OH} = -2mA	2.4	—	—	V
		I _{OH} = -20μA	V _{DD} - 0.2	—	—	V
V _{OL}	Output Low Voltage	I _{OL} = 2mA	—	—	0.4	V
		I _{OL} = 20μA	—	—	0.2	V
I _{DDO}	Operating Current	t _{cycle} = Min cycle, $\overline{CE} = V_{IL}$ Other Inputs = V _{IH} /V _{IL} , I _{OUT} = 0 mA	—	—	70	mA
I _{DDs1}	Standby Current	$\overline{CE} = V_{IH}$ Other Inputs = V _{IH} /V _{IL} , t _{cycle} = Min cycle	—	—	20	mA
I _{DDs2}		$\overline{CE} = V_{DD} - 0.2V$ Other Inputs = V _{DD} - 0.2V or 0.2V	—	—	300	μA

Capacitance* (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	6	pF
C _{I/O}	Input/Output Capacitance	V _{I/O} = GND	10	pF

*This parameter is periodically sampled and is not 100% tested.



AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 3.3V±0.3V)

Read Cycle

SYMBOL	PARAMETER	TC55V328J-20		TC55V328J-25		TC55V328J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	20	—	25	—	35	—	
t _{ACC}	Address Access Time	—	20	—	25	—	35	
t _{CO}	$\overline{\text{CE}}$ Access Time	—	20	—	25	—	35	
t _{OE}	$\overline{\text{OE}}$ Access Time	—	10	—	12	—	15	
t _{OH}	Output Data Hold Time from Address Change	5	—	5	—	5	—	ns
t _{COE}	Output Enable Time from $\overline{\text{CE}}$	5	—	5	—	5	—	
t _{COD}	Output Disable Time from $\overline{\text{CE}}$	—	8	—	10	—	15	
t _{OEE}	Output Enable Time from $\overline{\text{OE}}$	1	—	1	—	1	—	
t _{ODD}	Output Disable Time From $\overline{\text{OE}}$	—	8	—	10	—	15	

Write Cycle

SYMBOL	PARAMETER	TC55V328J-20		TC55V328J-25		TC55V328J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	20	—	25	—	35	—	
t _{WP}	Write Pulse Width	13	—	15	—	20	—	
t _{AW}	Address Valid to End of Write	13	—	15	—	20	—	
t _{CW}	Chip Enable to End of Write	13	—	15	—	20	—	
t _{AS}	Address Setup Time	0	—	0	—	0	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	0	—	
t _{DS}	Data Setup Time	10	—	12	—	15	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	
t _{OEw}	Output Enable Time From $\overline{\text{WE}}$	1	—	1	—	1	—	
t _{ODw}	Output Disable Time From $\overline{\text{WE}}$	—	8	—	10	—	15	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

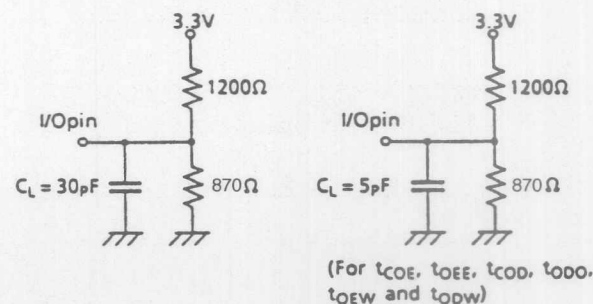
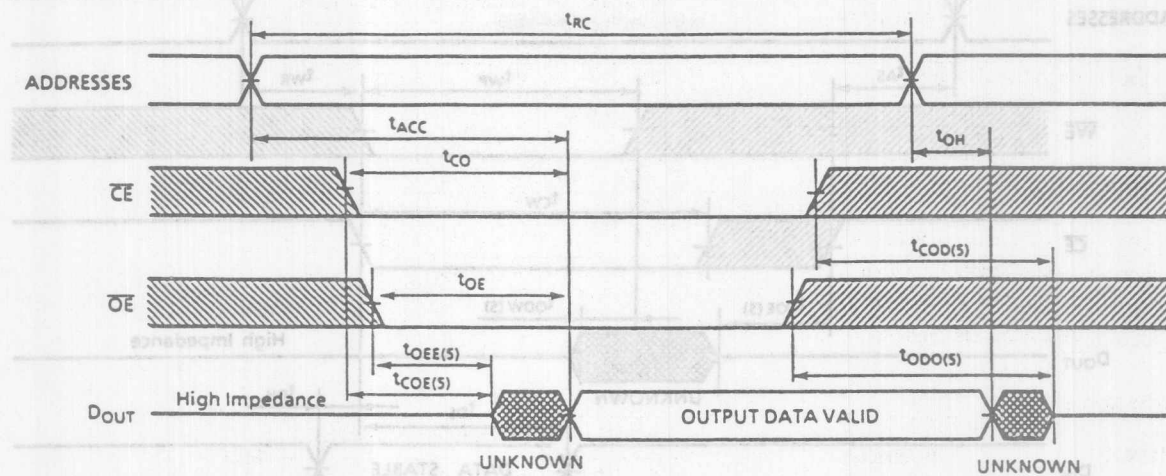
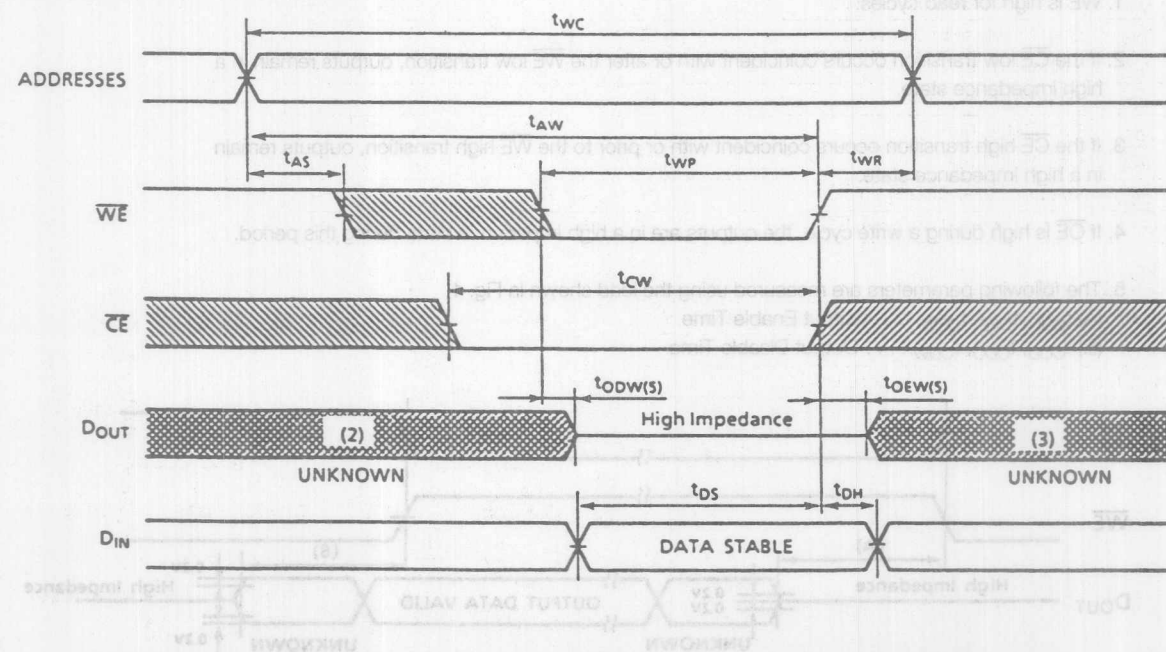
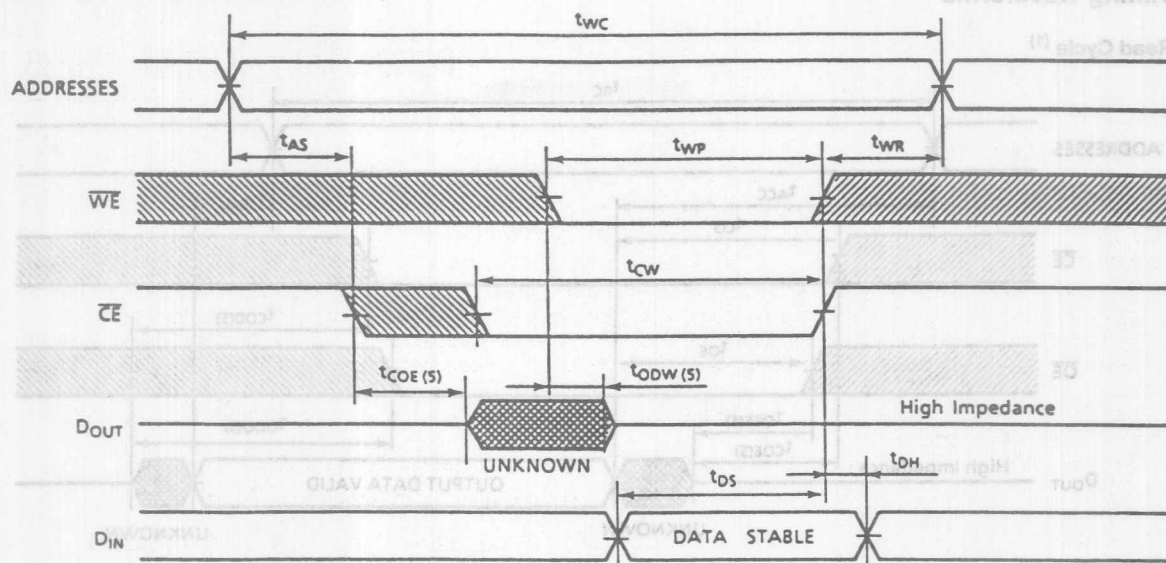


Figure 1.

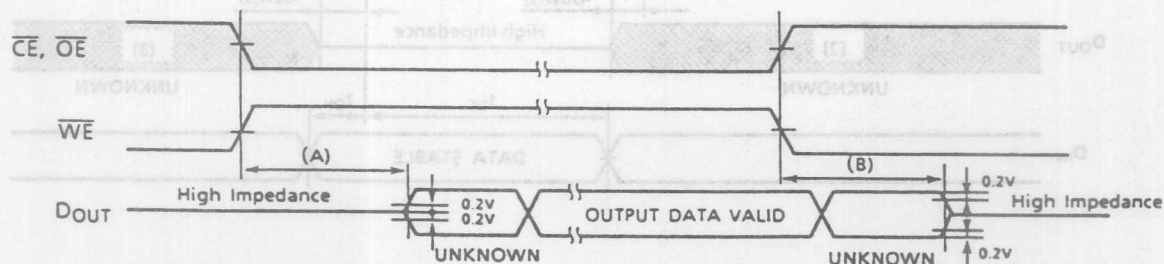
Timing Waveforms

Read Cycle ⁽¹⁾Write Cycle 1 ⁽⁴⁾ (\overline{WE} Controlled Write)

Write Cycle 2 ⁽⁴⁾ (\overline{CE} Controlled Write)

Notes:

1. \overline{WE} is high for read cycles.
2. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
3. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
4. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
5. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{COE} , t_{OEE} , t_{OEWS} Output Enable Time
 - (B) t_{COD} , t_{ODO} , t_{ODWS} Output Disable Time



TC55329AP/AJ-15/20/25/35

SILICON GATE CMOS

32,768 WORD x 9 BIT CMOS STATIC RAM

Description

The TC55329AP/AJ is a 294,912 bit high speed CMOS static random access memory organized as 32,768 words by 9 bits and operated from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC55329AP/AJ features low power dissipation when the device is deselected using chip enable (CE1, CE2) and has an output enable input (OE) for fast memory access. Also, the device power between memory accesses is reduced by an automatic power down circuit.

The TC55329AP/AJ is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC55329AP/AJ is available in a 300mil width, 32-pin DIP and SOJ suitable for high density surface assembly.

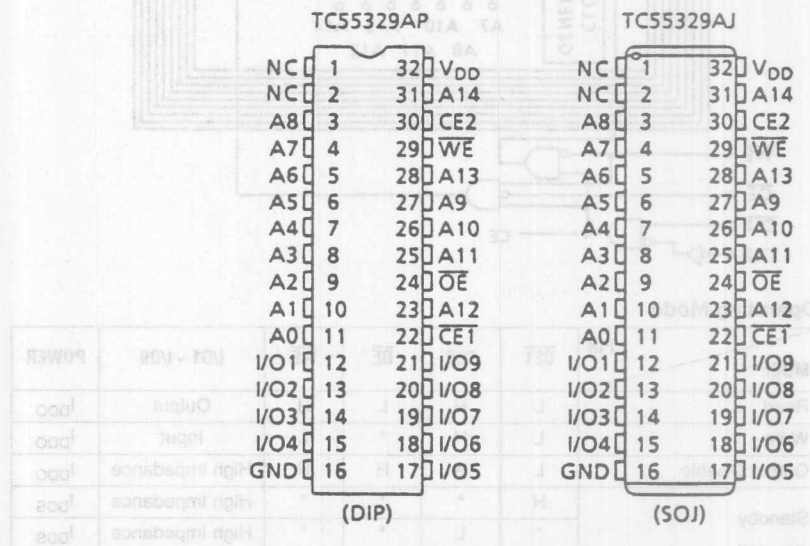
Features

- Fast access time
 - TC55329AP/AJ-15 15ns (max.)
 - TC55329AP/AJ-20 20ns (max.)
 - TC55329AP/AJ-25 25ns (max.)
 - TC55329AP/AJ-35 35ns (max.)
- Low power dissipation
 - Operation:
 - TC55329AP/AJ-15 140mA (max.)
 - TC55329AP/AJ-20 140mA (max.)
 - TC55329AP/AJ-25 140mA (max.)
 - TC55329AP/AJ-35 120mA (max.)
 - Standby: 1mA (max.)
- Single 5V power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: OE
- Package:
 - TC55329AP: DIP32-P-300
 - TC55329AJ: SOJ32-P-300

Pin Names

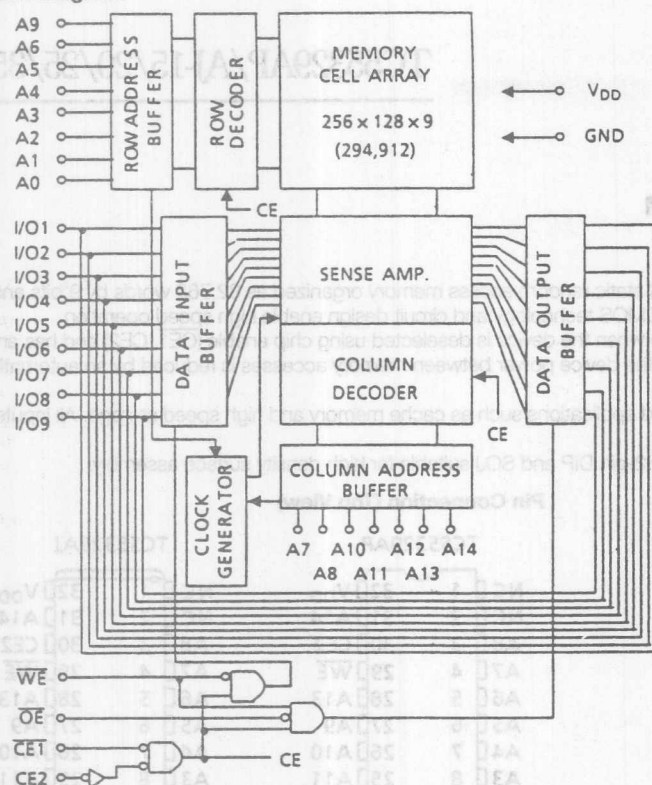
A0 ~ A14	Address Inputs
I/O1 ~ I/O9	Data Inputs/Outputs
CE1, CE2	Chip Enable Inputs
WE	Write Enable Input
OE	Output Enable Input
V _{DD}	Power (+5V)
GND	Ground
NC	No Connection

Pin Connection (Top View)



UNIT	RATING	ITEM	SYMBOL
V	5.0 - 7.0	Power Supply Voltage	V _{DD}
V	5.0 - 7.0	Input Voltage	V _I
V	-0.5 - V _{DD} + 0.5	Input/Output Voltage	V _O
W	1.0	Power Dissipation	P _D
°C	55 - 125	Storage Temperature	T _{STG}
°C	-10 - 85	Operating Temperature	T _{OP}

Block Diagram



Operating Mode

MODE	PIN	CE1	CE2	OE	WE	I/O1 ~ I/O9	POWER
Read		L	H	L	H	Output	I_{DD}
Write		L	H	*	L	Input	I_{DD}
Output Disable		L	H	H	H	High Impedance	I_{DD}
Standby		H	*	*	*	High Impedance	I_{DDs}
		*	L	*	*	High Impedance	I_{DDs}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

* -3V with a pulse width of 10ns

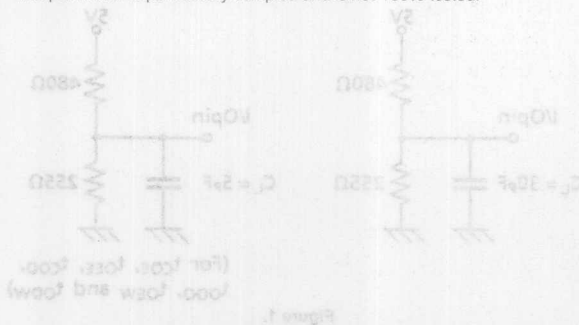
DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1	μA
I_{LO}	Output Leakage Current	$\overline{CE}1 = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	8	—	—	mA
I_{DDO}	Operating Current	$t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE}1 = V_{IL}$ or $CE2 = V_{IH}$ Other Inputs = V_{IH}/V_{IL}	-15	—	—	140
			-20	—	—	140
			-25	—	—	140
			-35	—	—	120
I_{DDS1}	Standby Current	$t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE}1 = V_{IH}$ or $CE2 = V_{IL}$ Other Inputs = V_{IH}/V_{IL}	-15	—	—	20
			-20	—	—	20
			-25	—	—	20
			-35	—	—	20
I_{DDS2}		$\overline{CE}1 = V_{DD} - 0.2\text{V}$ or $CE2 = 0.2\text{V}$ Other Inputs = $V_{DD} - 0.2\text{V}$ or 0.2V	—	—	1	mA

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
C_{IO}	Input/Output Capacitance	$V_{IO} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.



8.0V/0.8	Input Pulse Levels
3ns	Input Pulse Rise and Fall Time
2.5V/0.5V	Input Timing Measurement Reference Levels
8.0V/0.8V	Output Timing Measurement Reference Levels
50 Ω	Output Load

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55329AP/AJ-15		TC55329AP/AJ-20		TC55329AP/AJ-25		TC55329AP/AJ-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	ns
t_{ACC}	Address Access Time	—	15	—	20	—	25	—	35	
t_{CO1}	$\overline{CE1}$ Access Time	—	15	—	20	—	25	—	35	
t_{CO2}	$\overline{CE2}$ Access Time	—	15	—	20	—	25	—	35	
t_{OE}	\overline{OE} Access Time	—	8	—	10	—	12	—	15	
t_{OH}	Output Data Hold Time from Address Change	5	—	5	—	5	—	5	—	
t_{COE}	Output Enable Time from $\overline{CE1}$ or $\overline{CE2}$	5	—	5	—	5	—	5	—	
t_{COD}	Output Disable Time from $\overline{CE1}$ or $\overline{CE2}$	—	8	—	8	—	10	—	15	
t_{OEE}	Output Enable Time from \overline{OE}	1	—	1	—	1	—	1	—	
t_{ODO}	Output Disable Time from \overline{OE}	—	8	—	8	—	10	—	15	

Write Cycle

SYMBOL	PARAMETER	TC55329AP/AJ-15		TC55329AP/AJ-20		TC55329AP/AJ-25		TC55329AP/AJ-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	—	20	—	25	—	35	—	ns
t_{WP}	Write Pulse Width	10	—	11	—	13	—	18	—	
t_{AW}	Address Valid to End of Write	12	—	13	—	15	—	20	—	
t_{CW}	Chip Enable to End of Write	12	—	13	—	15	—	20	—	
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	
t_{DS}	Data Setup Time	8	—	10	—	12	—	15	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	
t_{OEw}	Output Enable Time from \overline{WE}	1	—	1	—	1	—	1	—	
t_{ODw}	Output Disable Time from \overline{WE}	—	8	—	8	—	10	—	15	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

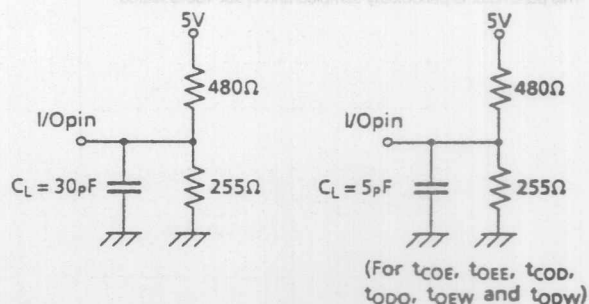
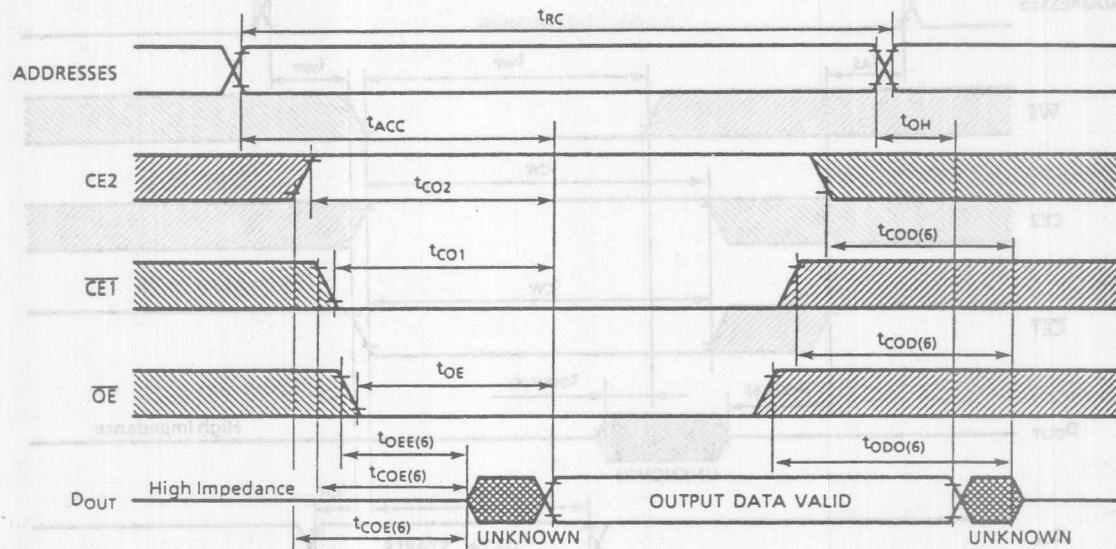
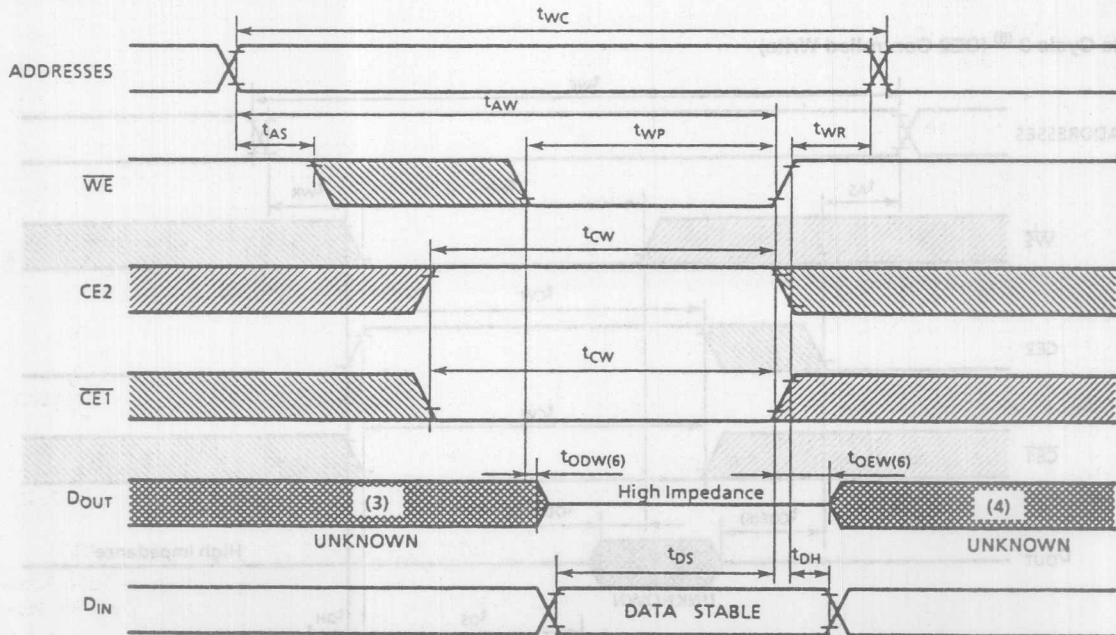
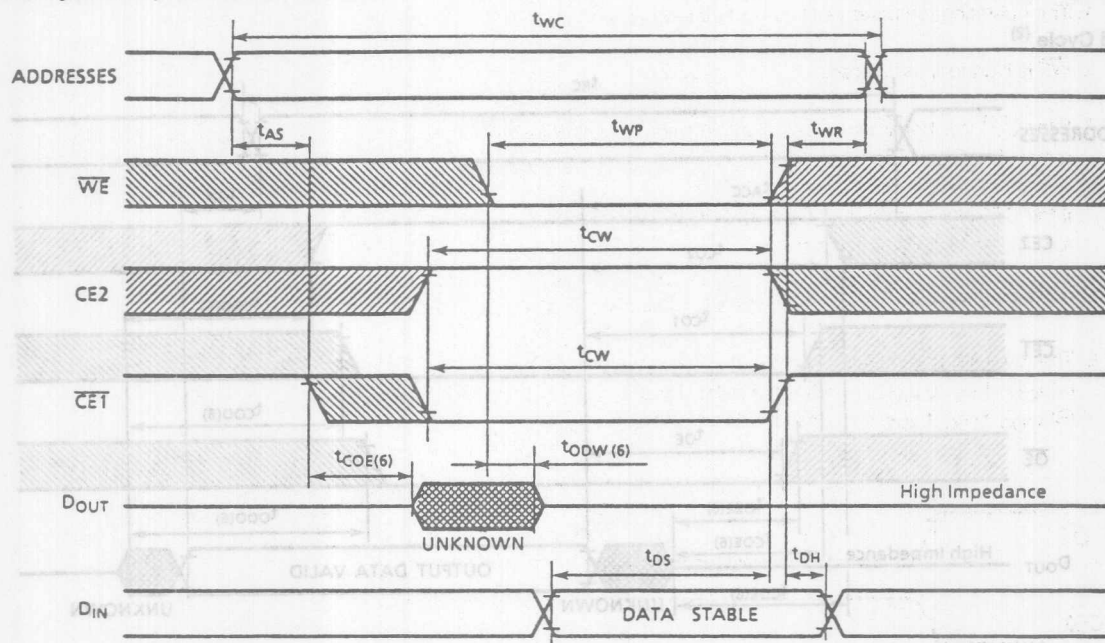
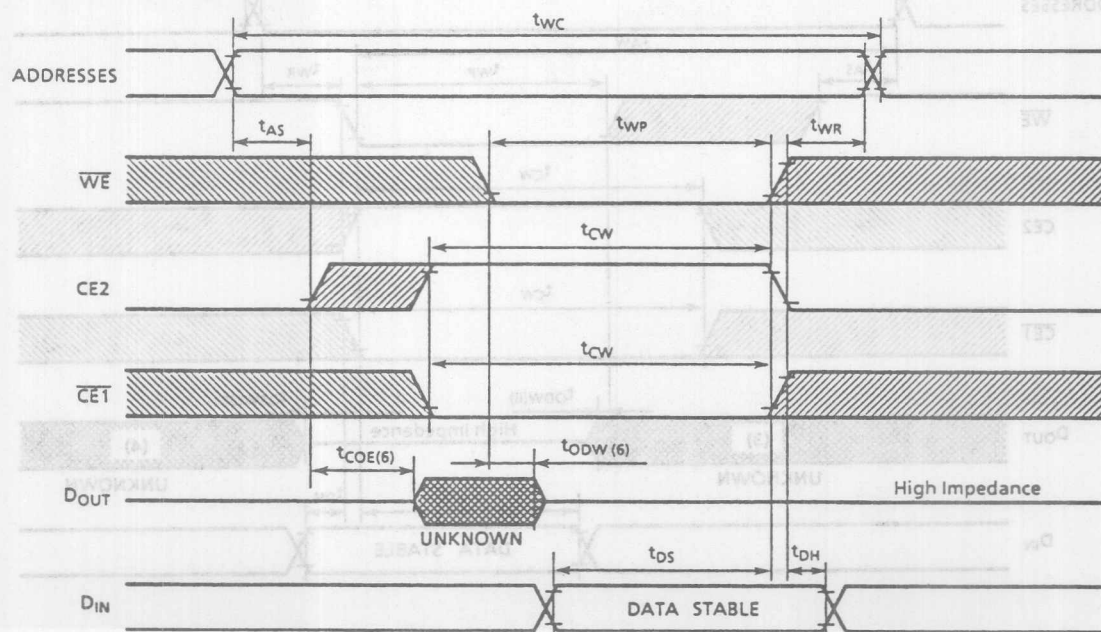


Figure 1.

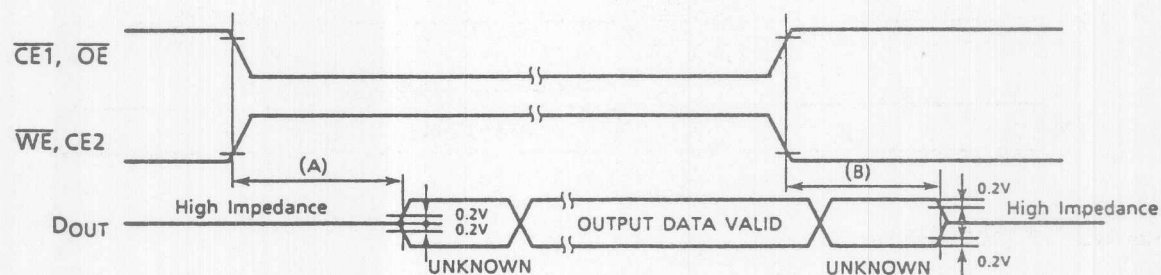
Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled Write)

Write Cycle 2 ⁽⁵⁾ ($\overline{\text{CE1}}$ Controlled Write)Write Cycle 3 ⁽⁵⁾ (CE2 Controlled Write)

Notes:

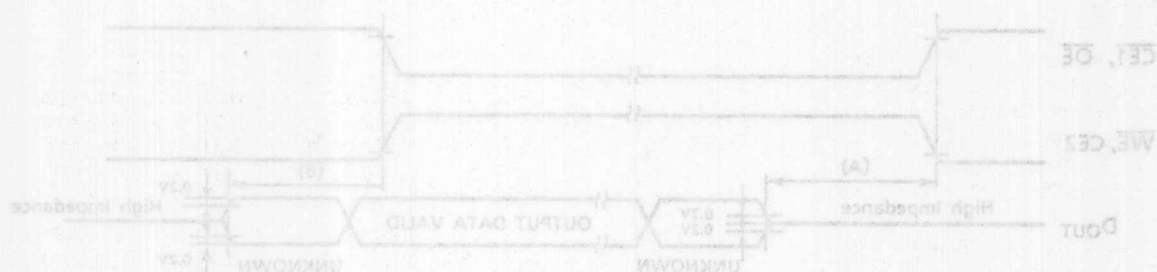
1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the $\overline{CE1}$ low transition or $CE2$ high transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the $\overline{CE1}$ high transition or $CE2$ low transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 (A) t_{COE} , t_{OEE} , $t_{OE\overline{W}}$ Output Enable Time
 (B) t_{COD} , t_{ODO} , $t_{OD\overline{W}}$ Output Disable Time



Notes

Notes:

1. The operating temperature (T_a) is guaranteed with tolerance at low exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the $\overline{CE1}$ low transition or $\overline{CE2}$ high transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the $\overline{CE1}$ high transition or $\overline{CE2}$ low transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 (A) t_{OE} low to low Output Enable Time
 (B) t_{OD} low to low Output Disable Time



SILICON GATE BiCMOS

32,768 WORD x 9 BIT BiCMOS STATIC RAM

Description

The TC55B329P/J is a 294,912 bit high speed BiCMOS static random access memory organized as 32,768 words by 9 bits and operated from a single 5V supply. Toshiba's BiCMOS technology and advanced circuit design enable high speed operation.

The TC55B329P/J features low power dissipation when the device is deselected using chip enable ($\overline{CE1}$, $\overline{CE2}$) and has an output enable input (\overline{OE}) for fast memory access.

The TC55B329P/J is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC55B329P/J is available in a 300mil width, 32-pin DIP and SOJ suitable for high density surface assembly.

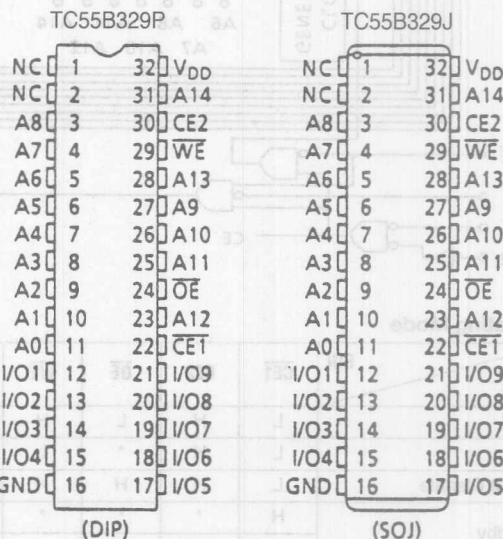
Features

- Fast access time
 - TC55B329P/J-10 10ns (max.)
 - TC55B329P/J-12 12ns (max.)
- Low power dissipation
 - Operation:
 - TC55B329P/J-10 170mA (max.)
 - TC55B329P/J-12 170mA (max.)
 - Standby: 15mA (max.)
- Single 5V power supply: $5V \pm 10\%$
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Package:
 - TC55B329P: DIP32-P-300
 - TC55B329J: SOJ32-P-300

Pin Names

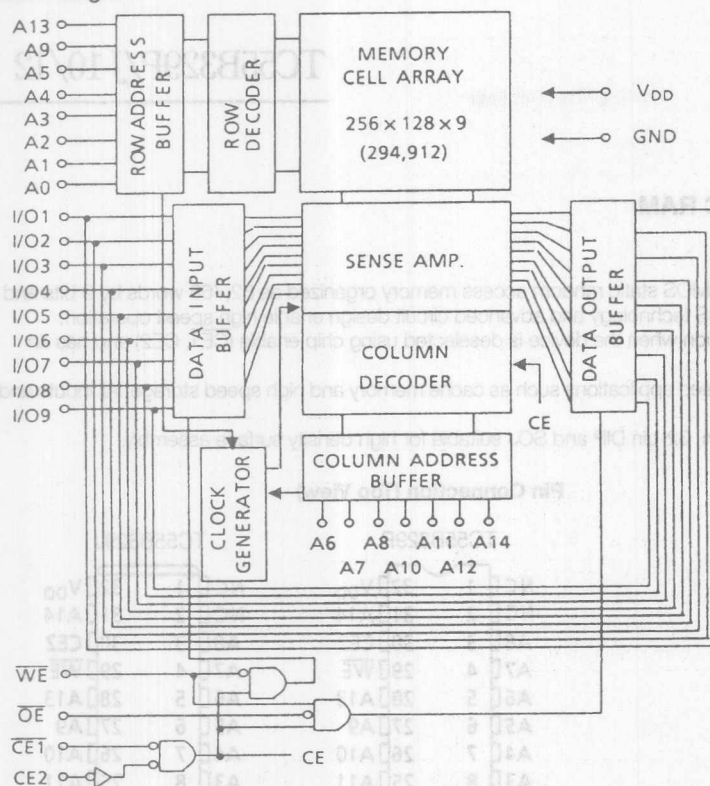
A0 ~ A14	Address Inputs
I/O1 ~ I/O9	Data Inputs/Outputs
$\overline{CE1}$, $\overline{CE2}$	Chip Enable Inputs
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
NC	No Connection

Pin Connection (Top View)



UNIT	RATING	ITEM
V	-0.5 - 7.0	Power Supply Voltage
V	2.0 - 7.0	Input Voltage
V	-0.5 - $V_{DD} + 0.5$	Output Voltage
W	1.0	Power Dissipation
$^{\circ}C \cdot sec$	250×10	Soldering Temperature - Time
$^{\circ}C$	-55 - 150	Storage Temperature
$^{\circ}C$	-10 - 85	Operating Temperature

Block Diagram



Operating Mode

MODE \ PIN	CE1	CE2	OE	WE	I/O1 ~ I/O9	POWER
Read	L	H	L	H	Output	I _{DD}
Write	L	H	*	L	Input	I _{DD}
Output Disable	L	H	H	H	High Impedance	I _{DD}
Standby	H	*	*	*	High Impedance	I _{DD}
	*	L	*	*	High Impedance	I _{DD}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V _{IN}	Input Voltage	-2.0 ~ 7.0	V
V _{IO}	Input/Output Voltage	-0.5* ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-65 ~ 150	°C
T _{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

* -3V with a pulse width of 10ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	8	—	—	mA
I_{DDO}	Operating Current	$t_{\text{cycle}} = \text{Min cycle}$, $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$ Other Inputs = V_{IH}/V_{IL} , $I_{OUT} = 0\text{mA}$	—	—	170	mA
I_{BDS1}	Standby Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ Other Inputs = V_{IH}/V_{IL}	—	—	30	mA
I_{BDS2}		$\overline{CE1} = V_{DD} - 0.2\text{V}$ or $CE2 = 0.2\text{V}$ Other Inputs = $V_{DD} - 0.2\text{V}$ or 0.2V	—	—	15	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
C_{IO}	Input/Output Capacitance	$V_{IO} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.



Figure 7.

Output Load	Output Timing Measurement Reference Levels	Input Timing Measurement Reference Levels	Input Pulse Rise and Fall Time	Input Pulse Levels	AC Test Conditions
Fig. 1	1.5V	1.5V	5ns	0.9V/0.5V	

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55B329P/J-10		TC55B329P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	—	12	—	ns
t_{ACC}	Address Access Time	—	10	—	12	
t_{CO1}	$\overline{CE1}$ Access Time	—	10	—	12	
t_{CO2}	CE2 Access Time	—	10	—	12	
t_{OE}	\overline{OE} Access Time	—	5	—	6	
t_{OH}	Output Data Hold Time from Address Change	3	—	3	—	
t_{COE}	Output Enable Time from $\overline{CE1}$ or CE2	3	—	3	—	
t_{COD}	Output Disable Time from $\overline{CE1}$ or CE2	—	5	—	6	
t_{OEE}	Output Enable Time from \overline{OE}	1	—	1	—	
t_{ODO}	Output Disable Time from \overline{OE}	—	5	—	6	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	10	—	12	

Write Cycle

SYMBOL	PARAMETER	TC55B329P/J-10		TC55B329P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	—	12	—	ns
t_{CW}	Chip Enable to End of Write	7	—	8	—	
t_{AS}	Address Setup Time	0	—	0	—	
t_{AW}	Address Valid to End of Write	7	—	8	—	
t_{WP}	Write Pulse Width	6	—	7	—	
t_{WR}	Write Recovery Time	1	—	1	—	
t_{DS}	Data Setup Time	6	—	7	—	
t_{DH}	Data Hold Time	0	—	0	—	
t_{OEw}	Output Enable Time from \overline{WE}	1	—	1	—	
t_{ODw}	Output Disable Time from \overline{WE}	—	5	—	6	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

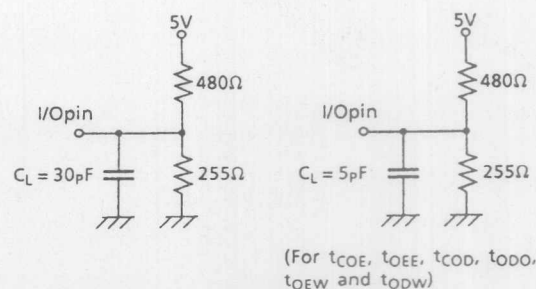
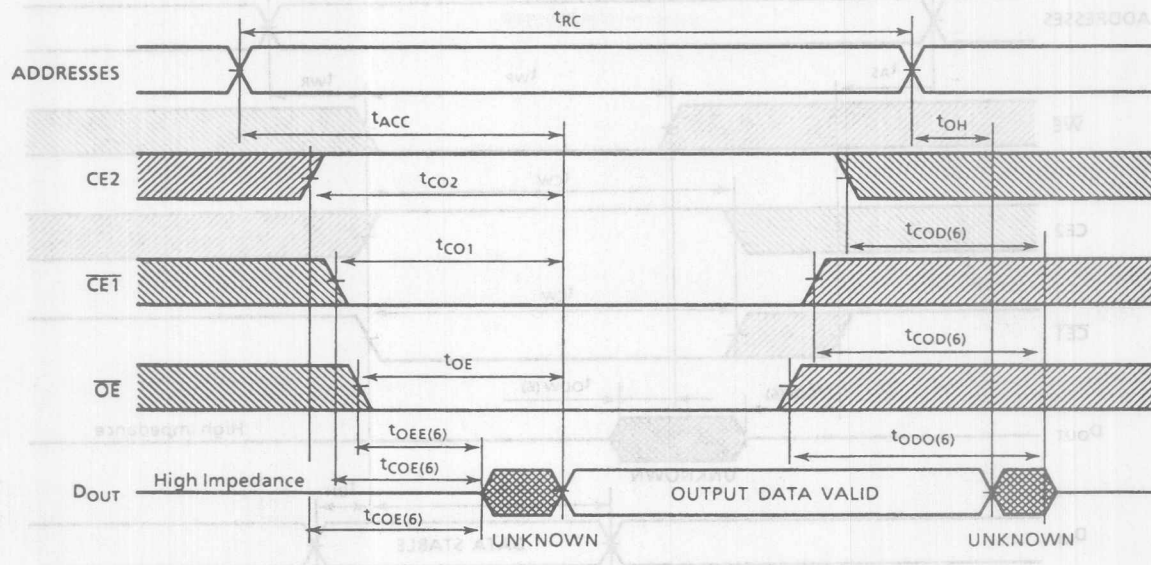
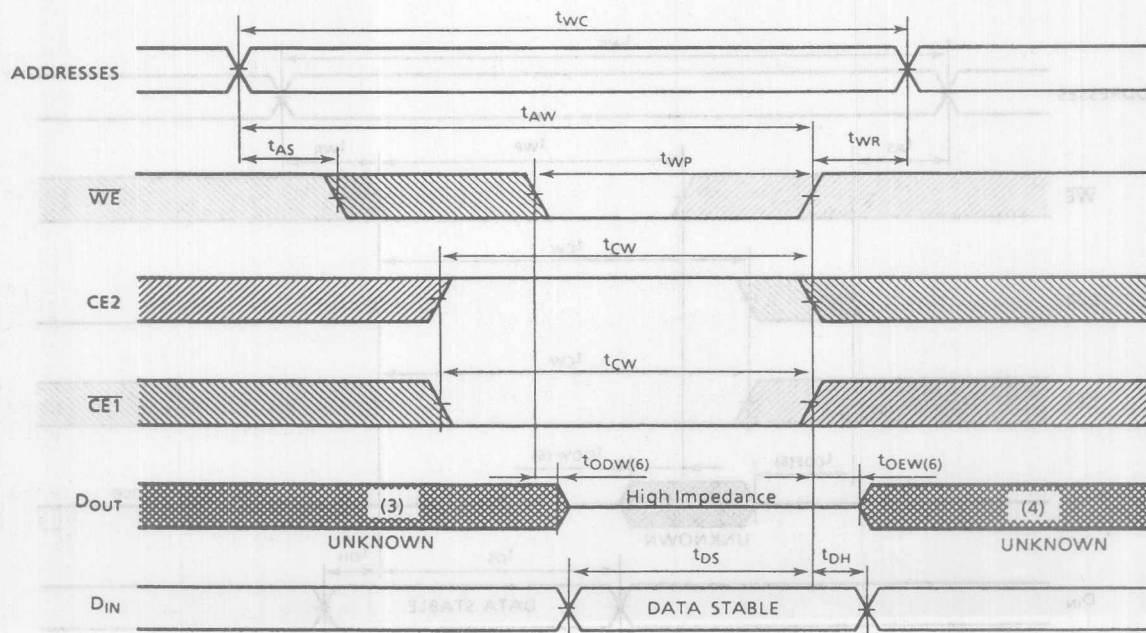
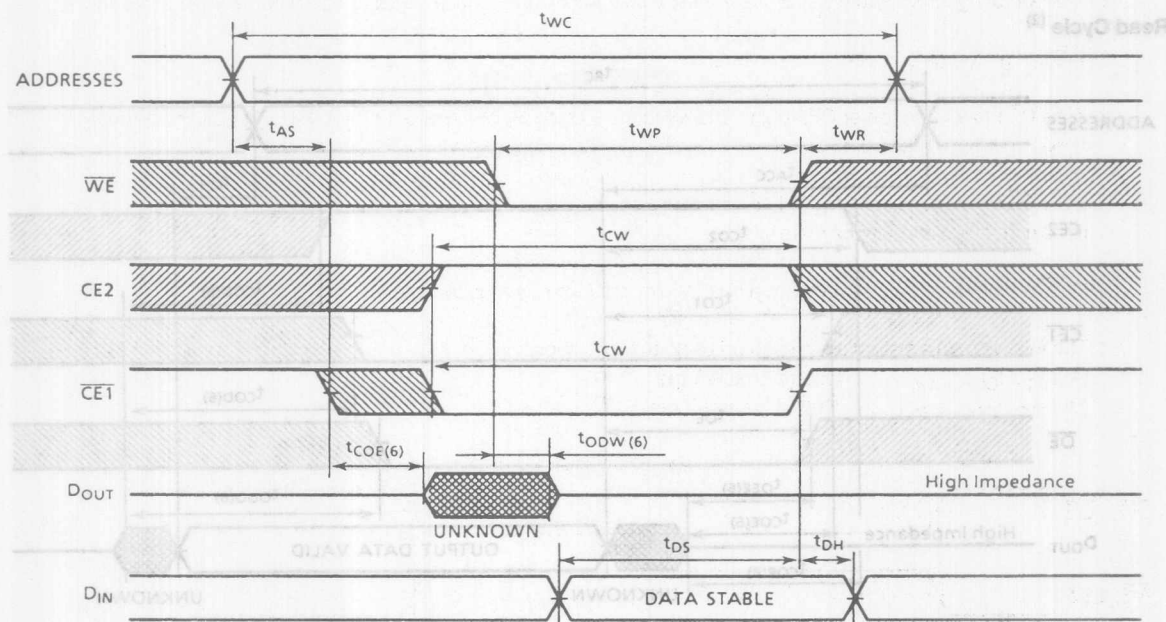
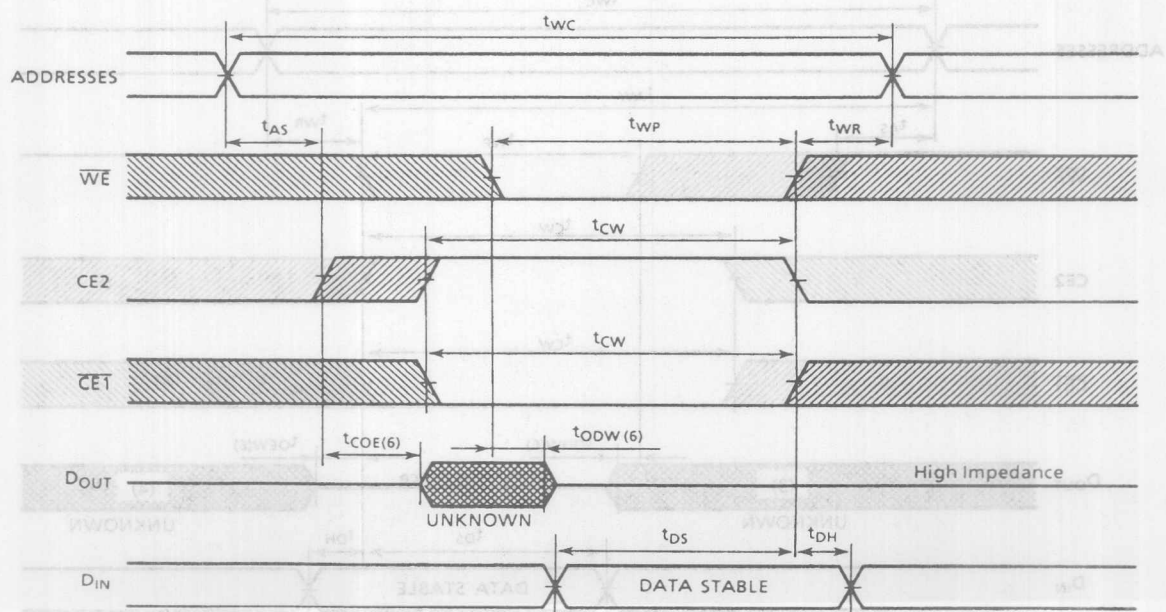


Figure 1.

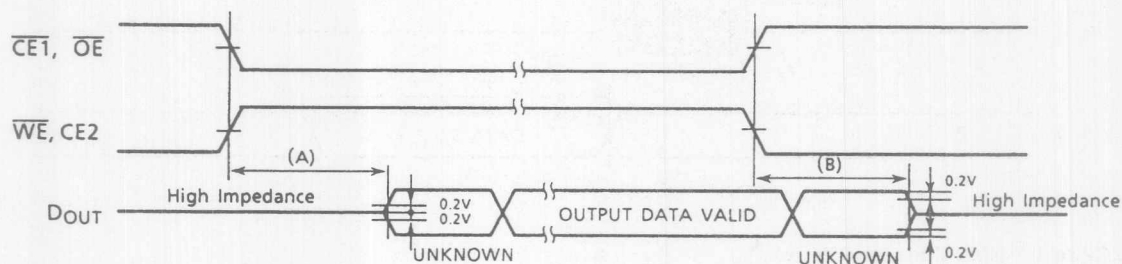
Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled Write)

Write Cycle 2 ⁽⁵⁾ ($\overline{\text{CE1}}$ Controlled Write)Write Cycle 3 ⁽⁵⁾ (CE2 Controlled Write)

Notes:

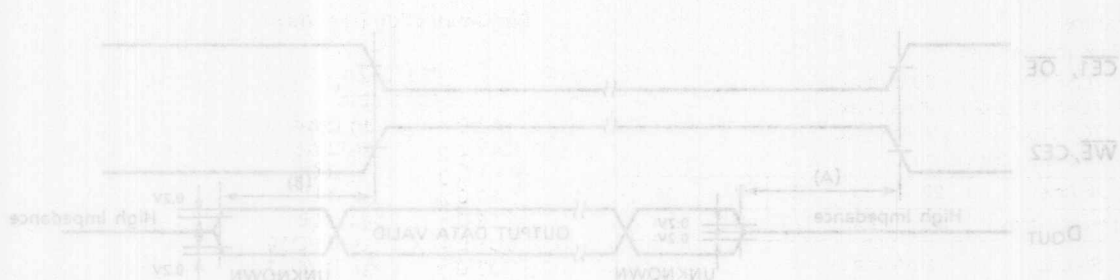
1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the $\overline{CE1}$ low transition or $CE2$ high transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the $\overline{CE1}$ high transition or $CE2$ low transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{COE} , t_{OEE} , $t_{OE\overline{W}}$ Output Enable Time
 - (B) t_{COD} , t_{ODO} , $t_{OD\overline{W}}$ Output Disable Time



Notes

Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the $\overline{CE1}$ low transition or $\overline{CE2}$ high transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the $\overline{CE1}$ high transition or $\overline{CE2}$ low transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 - (A) $t_{OE, low}$... Output Enable Time
 - (B) $t_{OD, low}$... Output Disable Time



SILICON GATE CMOS

32,768 WORD x 16 BIT CMOS STATIC RAM

Description

The TC551632J is a 524,288 bit high speed CMOS static random access memory organized as 32,768 words by 16 bits and operated from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC551632J features low power dissipation when the device is deselected using chip enable (CE), and has an output enable input (OE) for fast memory access. Byte access is supported by upper and lower byte controls.

The TC551632J is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC551632J is available in a 400mil width, 40-pin SOJ suitable for high density surface assembly.

Features

- Fast access time
 - TC551632J-20 20ns (max.)
 - TC551632J-25 25ns (max.)
 - TC551632J-35 35ns (max.)
- Low power dissipation

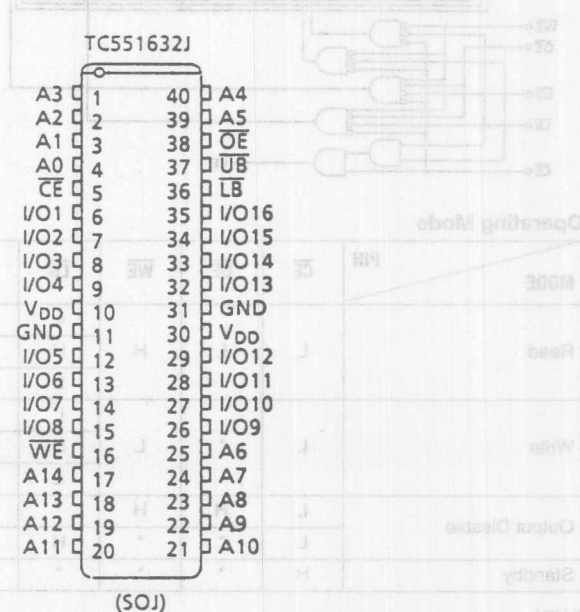
Cycle Time	20	25	35	100	ns
Operation (max.)	220	200	170	130	mA

- Standby: 1mA (max.)
- Single 5V power supply: $5V \pm 10\%$
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Data byte controls: \overline{LB} , \overline{UB}
- Package: SOJ40-P-400

Pin Names

A0 ~ A14	Address Inputs
I/O1 ~ I/O16	Data Inputs/Outputs
CE	Chip Enable Input
WE	Write Enable Input
OE	Output Enable Input
LB, UB	Data Byte Control Inputs
V _{DD}	Power (+5V)
GND	Ground

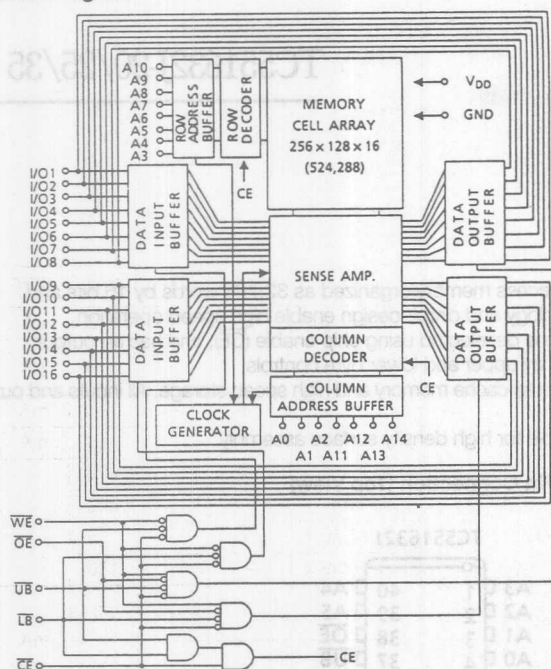
Pin Connection (Top View)



(SOJ)

UNIT	RATING	ITEM	SYMBOL
V	-0.5 ~ 7.0	Power Supply Voltage	V _{DD}
V	-0.5 ~ 7.0	Input Voltage	V _{IN}
V	-0.5 ~ V _{DD} + 0.5	Input/Output Voltage	V _{IO}
W	7.5	Power Dissipation	P _D
°C	280 ~ 10	Storage Temperature	T _{STG}
°C	-55 ~ 150	Operating Temperature	T _{OP}

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O1 ~ I/O8	I/O9 ~ I/O16	POWER
Read		L	L	H	L	L	Output	Output	I_{DDO}
					H	L	High Impedance	Output	I_{DDO}
					L	H	Output	High Impedance	I_{DDO}
Write		L	*	L	L	L	Input	Input	I_{DDO}
					H	L	High Impedance	Input	I_{DDO}
					L	H	Input	High Impedance	I_{DDO}
Output Disable		L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
		L	*	*	H	H	High Impedance	High Impedance	I_{DDO}
Standby		H	*	*	*	*	High Impedance	High Impedance	I_{DDO}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0* ~ 7.0	V
V_{IO}	Input/Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

* -3V with a pulse width of 10ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	8	—	—	mA
I_{DDO}	Operating Current	$\overline{CE} = V_{IL}$, $I_{OUT} = 0\text{mA}$, Other Inputs = V_{IH}/V_{IL}	$t_{\text{cycle}} = 20\text{ns}$	—	—	220
			$t_{\text{cycle}} = 25\text{ns}$	—	—	200
			$t_{\text{cycle}} = 35\text{ns}$	—	—	170
			$t_{\text{cycle}} = 100\text{ns}$	—	—	130
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, or $\overline{UB} = \overline{LB} = V_{IH}$ Other Inputs = V_{IH}/V_{IL}	—	—	30	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2V$, or $\overline{UB} = \overline{LB} = V_{DD} - 0.2V$ Other Inputs = $V_{DD} - 0.2V$ or $0.2V$	—	—	1	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.



Figure 4

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC551632J-20		TC551632J-25		TC551632J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t_{ACC}	Address Access Time	—	20	—	25	—	35	
t_{CO}	\overline{CE} Access Time	—	20	—	25	—	35	
t_{OE}	\overline{OE} Access Time	—	10	—	12	—	17	
t_{BA}	\overline{UB} , \overline{LB} Access Time	—	20	—	25	—	35	
t_{OH}	Output Data Hold Time from Address Change	5	—	5	—	5	—	
t_{COE}	Output Enable Time from \overline{CE}	5	—	5	—	5	—	
t_{OEE}	Output Enable Time from \overline{OE}	1	—	1	—	1	—	
t_{BE}	Output Enable Time from \overline{UB} , \overline{LB}	1	—	1	—	1	—	
t_{COD}	Output Disable Time from \overline{CE}	—	8	—	8	—	8	
t_{ODO}	Output Disable Time from \overline{OE}	—	8	—	8	—	8	
t_{BD}	Output Disable Time from \overline{UB} , \overline{LB}	—	8	—	8	—	8	

Write Cycle

SYMBOL	PARAMETER	TC551632J-20		TC551632J-25		TC551632J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	20	—	25	—	35	—	ns
t_{WP}	Write Pulse Width	10	—	12	—	16	—	
t_{CW}	Chip Enable to End of Write	13	—	15	—	17	—	
t_{BW}	\overline{UB} , \overline{LB} Enable to End of Write	13	—	15	—	17	—	
t_{AW}	Address Valid to End of Write	12	—	14	—	16	—	
t_{AS}	Address Setup Time	0	—	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{DS}	Data Setup Time	10	—	10	—	10	—	
t_{DH}	Data Hold Time (\overline{WE})	0	—	0	—	0	—	
t_{DH1}	Data Hold Time (\overline{CE} , \overline{UB} , \overline{LB})	1	—	1	—	1	—	
t_{OEw}	Output Enable Time from \overline{WE}	1	—	1	—	1	—	
t_{ODw}	Output Disable Time from \overline{WE}	—	8	—	8	—	8	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

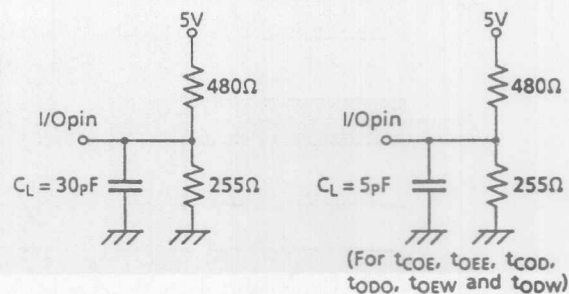
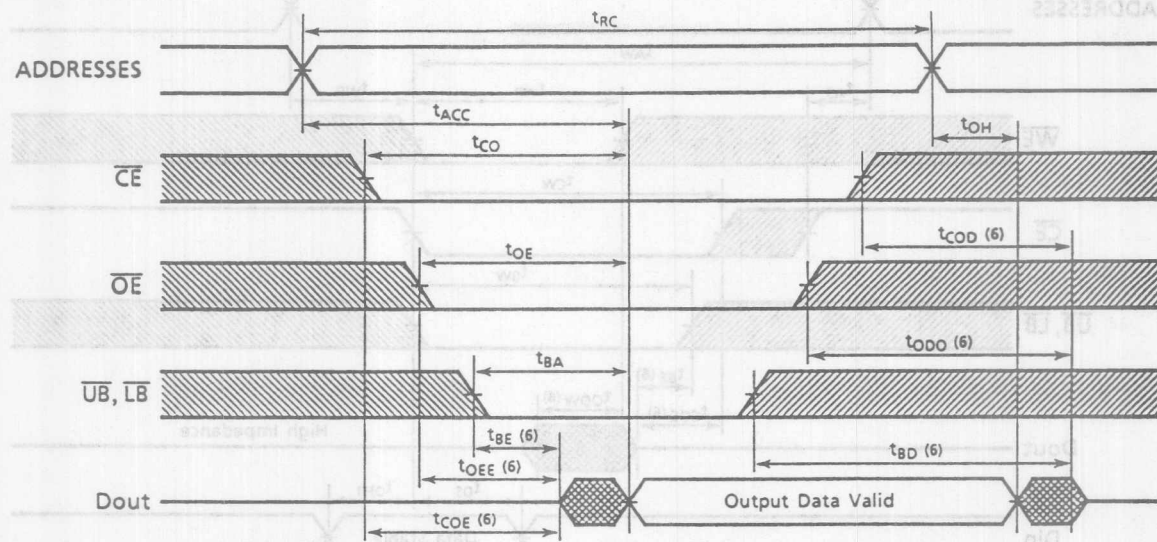
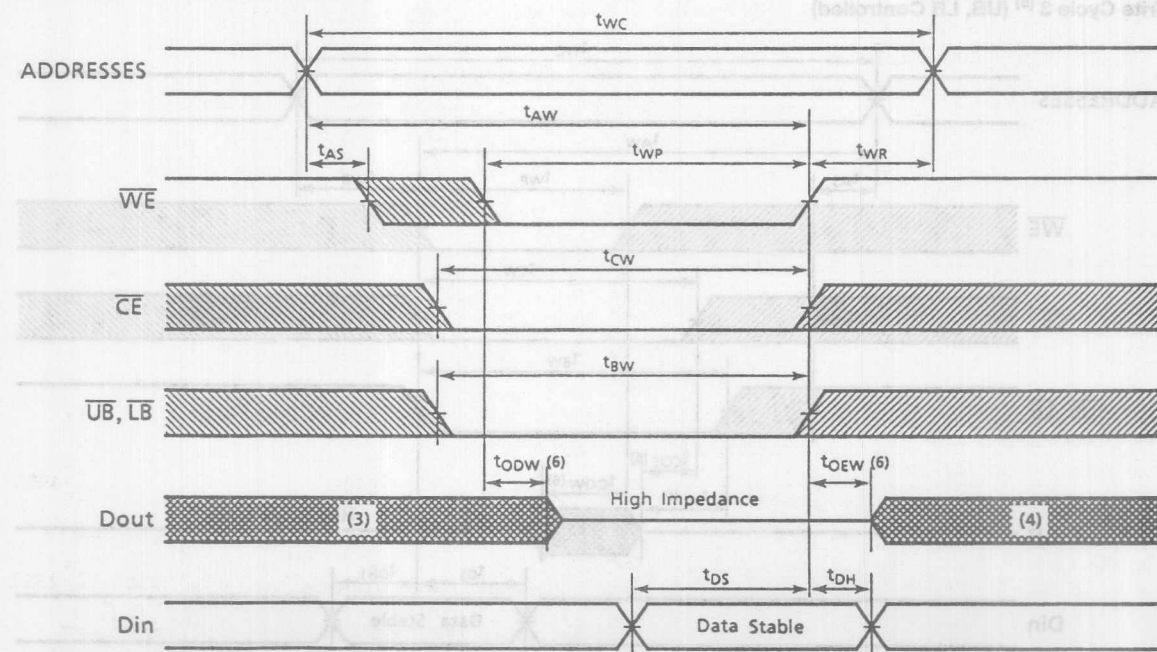
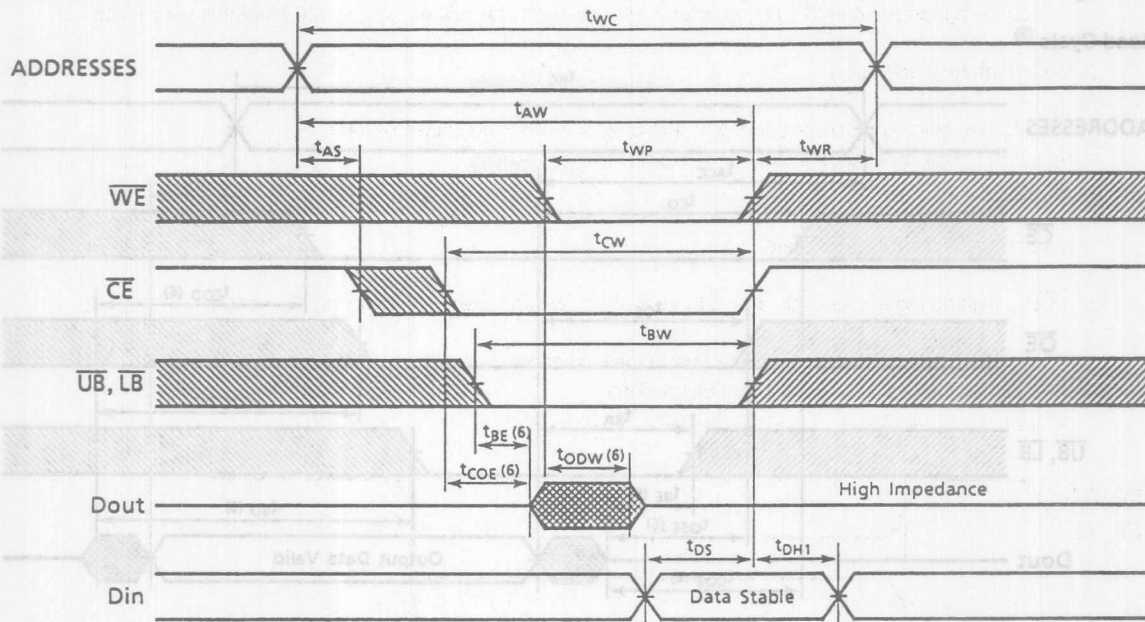
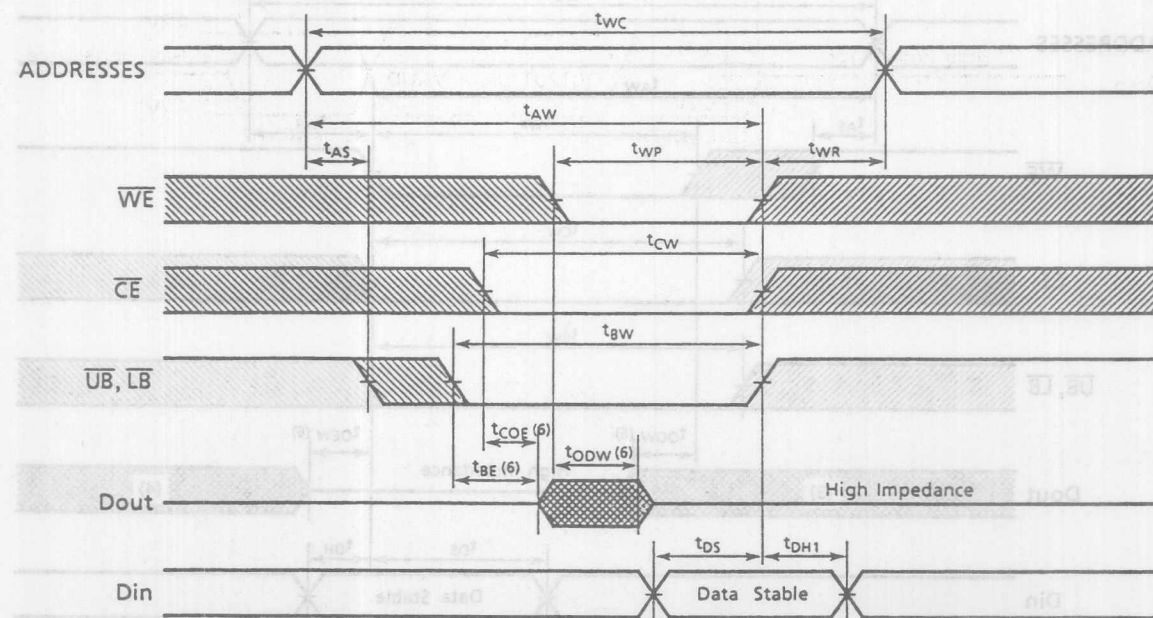


Figure 1.

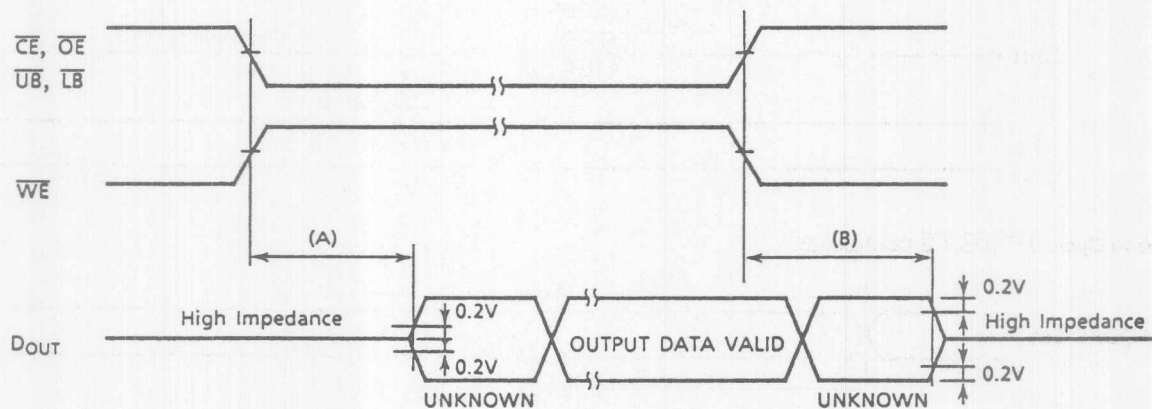
Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled)

Write Cycle 2 ⁽⁵⁾ ($\overline{\text{CE}}$ Controlled)Write Cycle 3 ⁽⁵⁾ ($\overline{\text{UB}}, \overline{\text{LB}}$ Controlled)

Notes:

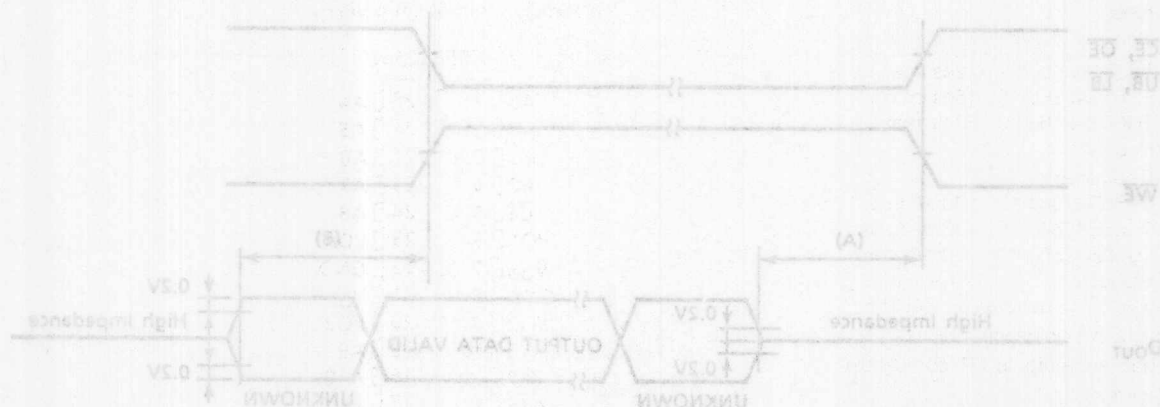
1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{OE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{OE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 (A) t_{COE} , t_{OEE} , t_{BE} , $t_{OE\overline{W}}$ Output Enable Time
 (B) t_{COD} , t_{ODO} , t_{BD} , t_{ODW} Output Disable Time



Notes

Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{OE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{OE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1:
 (A) $t_{OE, low \rightarrow low}$ Output Enable Time
 (B) $t_{OE, low \rightarrow low}$ Output Disable Time



TC55B4256J-12/15/20

SILICON GATE BiCMOS

262,144 WORD x 4 BIT BiCMOS STATIC RAM

Description

The TC55B4256J is a 1,048,576 bit high speed BiCMOS static random access memory organized as 262,144 words by 4 bits and operated from a single 5V supply. Toshiba's BiCMOS technology and advanced circuit design enable high speed operation.

The TC55B4256J features low power dissipation when the device is deselected using chip enable (CE).

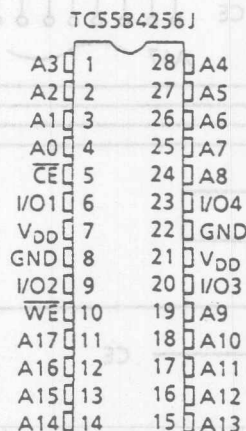
The TC55B4256J is suitable for use in applications where high speed is required such as cache memory, high speed storage, and main memory. All inputs and outputs are TTL compatible.

The TC55B4256J is available in a 400mil width, 28-pin SOJ suitable for high density surface assembly.

Features

- Fast access time
 - TC55B4256J-12 12ns (max.)
 - TC55B4256J-15 15ns (max.)
 - TC55B4256J-20 20ns (max.)
- Low power dissipation
 - Operation:
 - TC55B4256J-12 130mA (max.)
 - TC55B4256J-15 130mA (max.)
 - TC55B4256J-20 130mA (max.)
 - Standby: 12mA (max.)
- Single 5V power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Package:
 - TC55B4256J : SOJ28-P-400

Pin Connection (Top View)



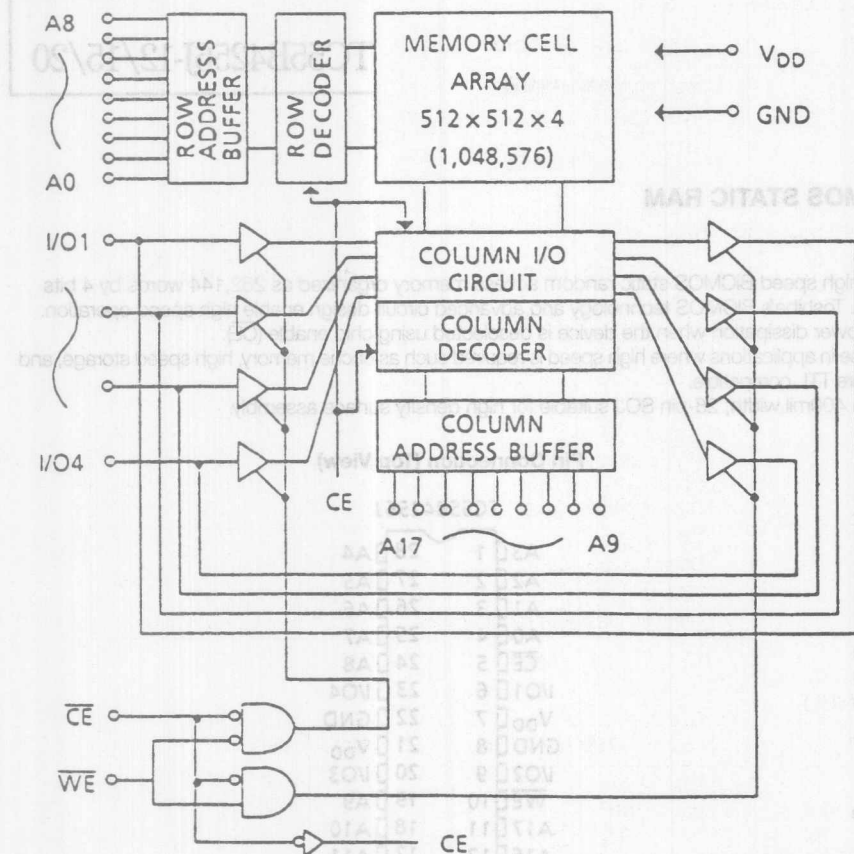
Pin Names

A0 ~ A17	Address Inputs
I/O1 ~ I/O4	Data Inputs/Outputs
CE	Chip Enable Input
WE	Write Enable Input
V _{DD}	Power (+5V)
GND	Ground

MODE	WE	CE	I/O	POWER
Read	H	L	Output	1000
Write	L	L	Input	1000
Standby	H	H	High-Z	1000

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V _{IN}	Input Voltage	-0.5 ~ 7.0	V
V _{IO}	Input/Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _C	Power Dissipation	800	mW
T _{STG}	Storage Temperature	-55 ~ 125	°C
T _{OP}	Operating Temperature	-10 ~ 85	°C

Block Diagram



Operating Mode

MODE \ PIN	$\overline{\text{CE}}$	$\overline{\text{WE}}$	I/O	POWER
Read	L	H	Output	I_{DDO}
Write	L	L	Input	I_{DDO}
Standby	H	*	High-Z	I_{DDs}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V _{IN}	Input Voltage	-2.0* ~ 7.0	V
V _{I/O}	Input/Output Voltage	-0.5* ~ V _{DD} + 0.5	V
P _D	Power Dissipation	900	mW
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-65 ~ 150	°C
T _{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

* -3V with a pulse width of 10ns

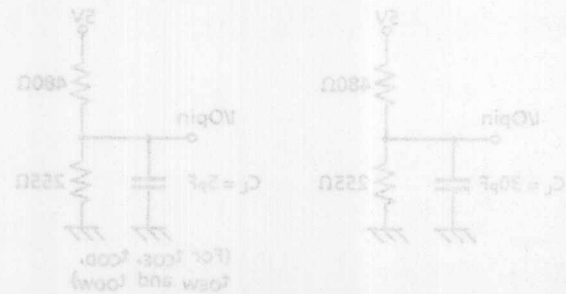
DC Characteristics ($T_a = 0 \sim 70^{\circ}\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	8	—	—	mA
I_{DDO}	Operating Current	$t_{\text{cycle}} = \text{Min cycle}$, $\overline{CE} = V_{IL}$, $I_{OUT} = 0\text{mA}$, Other Inputs = V_{IH}/V_{IL}	—	—	130	mA
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V_{IH}/V_{IL}	—	—	30	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2\text{V}$, Other Inputs = $V_{DD} - 0.2\text{V}$ or 0.2V	—	—	12	

Capacitance* ($T_a = 25^{\circ}\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.



AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55B4256J-12		TC55B4256J-15		TC55B4256J-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	12	—	15	—	20	—	ns
t_{ACC}	Address Access Time	—	12	—	15	—	20	
t_{CO}	Chip Enable Access Time	—	12	—	15	—	20	
t_{OH}	Output Data Hold Time from Address Change	4	—	4	—	4	—	
t_{COE}	Output Enable Time from \overline{CE}	4	—	4	—	4	—	
t_{COD}	Output Disable Time from \overline{CE}	—	6	—	7	—	8	

Write Cycle

SYMBOL	PARAMETER	TC55B4256J-12		TC55B4256J-15		TC55B4256J-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	12	—	15	—	20	—	ns
t_{WP}	Write Pulse Width	8	—	9	—	10	—	
t_{AW}	Address Valid to End of Write	9	—	10	—	11	—	
t_{CW}	Chip Enable to End of Write	8	—	9	—	10	—	
t_{AS}	Address Setup Time	0	—	0	—	0	—	
t_{WR}	Write Recovery Time	1	—	1	—	1	—	
t_{OEw}	Output Enable Time from \overline{WE}	1	—	1	—	1	—	
t_{ODW}	Output Disable Time from \overline{WE}	—	6	—	7	—	8	
t_{DS}	Data Setup Time	7	—	8	—	9	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

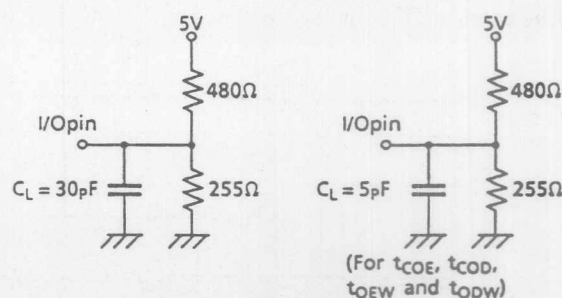
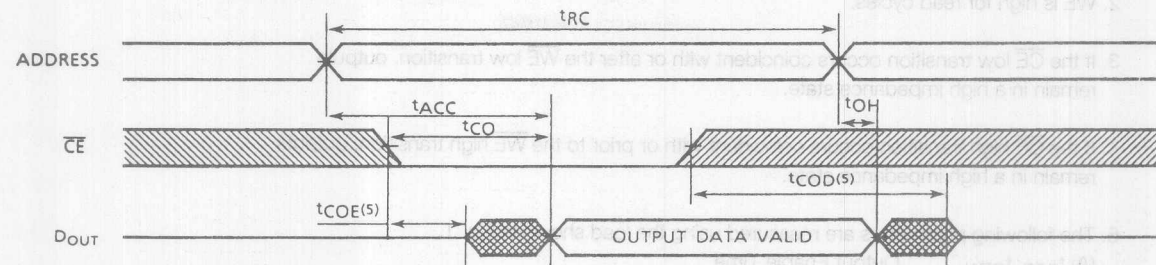
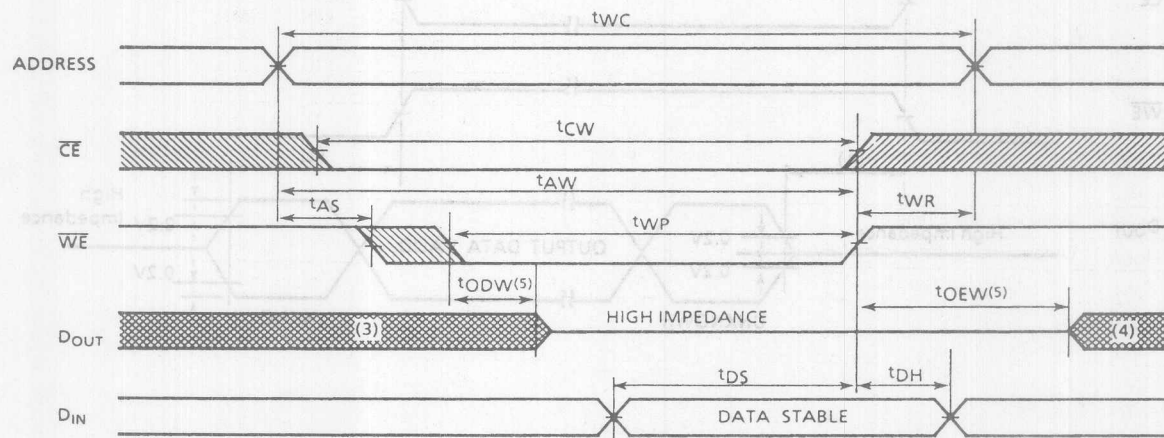
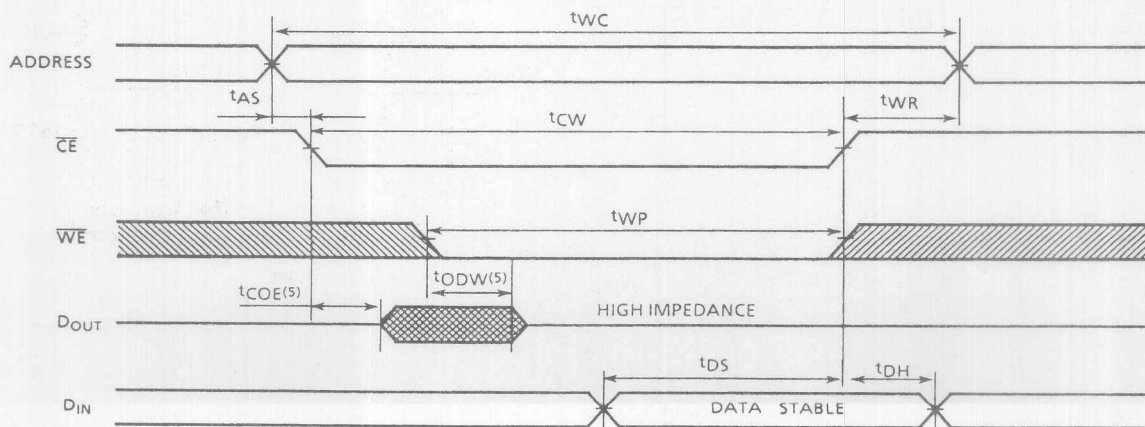


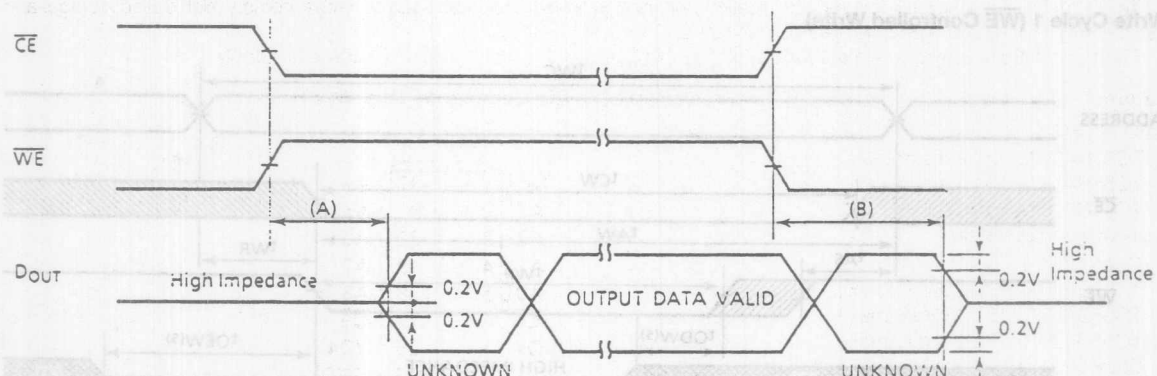
Figure 1.

Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 (\overline{WE} Controlled Write)Write Cycle 2 (\overline{CE} Controlled Write)

Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{COE} , $t_{OE\overline{W}}$ Output Enable Time
 - (B) t_{COD} , $t_{OD\overline{W}}$ Output Disable Time



SILICON GATE BiCMOS

262,144 WORD x 4 BIT BiCMOS STATIC RAM

Description

The TC55B4257J is a 1,048,576 bit high speed BiCMOS static random access memory organized as 262,144 words by 4 bits and operated from a single 5V supply. Toshiba's BiCMOS technology and advanced circuit design enable high speed operation.

The TC55B4257J features low power dissipation when the device is deselected using chip enable (\overline{CE}), and has an output enable input (\overline{OE}) for fast memory access.

The TC55B4257J is suitable for use in applications where high speed is required such as cache memory, high speed storage, and main memory. All inputs and outputs are TTL compatible.

The TC55B4257J is available in a 400mil width, 32-pin SOJ suitable for high density surface assembly.

Features

- Fast access time
 - TC55B4257J-12 12ns (max.)
 - TC55B4257J-15 15ns (max.)
 - TC55B4257J-20 20ns (max.)
- Low power dissipation
 - Operation:
 - TC55B4257J-12 130mA (max.)
 - TC55B4257J-15 130mA (max.)
 - TC55B4257J-20 130mA (max.)
 - Standby: 12mA (max.)
- Single 5V power supply: 5V \pm 10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Package:
 - TC55B4257J : SOJ32-P-400A

Pin Connection (Top View)

TC55B4257J

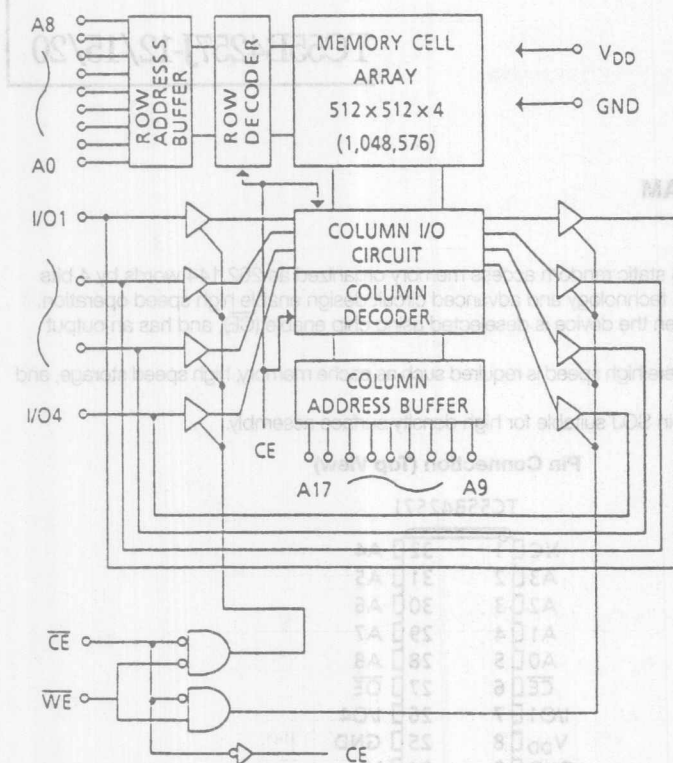
NC	1	32	A4
A3	2	31	A5
A2	3	30	A6
A1	4	29	A7
A0	5	28	A8
\overline{CE}	6	27	\overline{OE}
I/O1	7	26	I/O4
V _{DD}	8	25	GND
GND	9	24	V _{DD}
I/O2	10	23	I/O3
\overline{WE}	11	22	A9
A17	12	21	A10
A16	13	20	A11
A15	14	19	A12
A14	15	18	A13
NC	16	17	NC

(SOJ)

Pin Names

A0 ~ A17	Address Inputs
I/O1 ~ I/O4	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V _{DD}	Power (+5V)
GND	Ground
NC	No Connection

Block Diagram



Operating Mode

MODE \ PIN	CE	OE	WE	I/O	POWER
Read	L	L	H	Output	I_{ODD}
Write	L	*	L	Input	I_{ODD}
Output Disabled	L	H	H	High-Z	I_{ODD}
Standby	H	*	*	High-Z	I_{ODS}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0* ~ 7.0	V
V_{IO}	Input/Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	900	mW
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

* -3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

* -3V with a pulse width of 10ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	8	—	—	mA
I_{DDO}	Operating Current	$t_{\text{cycle}} = \text{Min cycle}$, $\overline{CE} = V_{IL}$, $I_{OUT} = 0\text{mA}$, Other Inputs = V_{IH}/V_{IL}	—	—	130	mA
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V_{IH}/V_{IL}	—	—	30	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2\text{V}$, Other Inputs = $V_{DD} - 0.2\text{V}$ or 0.2V	—	—	12	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
C_{IO}	Input/Output Capacitance	$V_{IO} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.



Figure 1

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55B4257J-12		TC55B4257J-15		TC55B4257J-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	12	—	15	—	20	—	ns
t_{ACC}	Address Access Time	—	12	—	15	—	20	
t_{CO}	Chip Enable Access Time	—	12	—	15	—	20	
t_{OE}	Output Enable Access Time	—	7	—	8	—	10	
t_{COE}	Output Enable Time from \overline{CE}	4	—	4	—	4	—	
t_{COD}	Output Disable Time from \overline{CE}	—	6	—	7	—	8	
t_{OEE}	Output Enable Time from \overline{OE}	0	—	0	—	0	—	
t_{ODO}	Output Disable Time from \overline{OE}	—	5	—	6	—	7	
t_{OH}	Output Data Hold Time from Address Change	4	—	4	—	4	—	

Write Cycle

SYMBOL	PARAMETER	TC55B4257J-12		TC55B4257J-15		TC55B4257J-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	12	—	15	—	20	—	ns
t_{WP}	Write Pulse Width	8	—	9	—	10	—	
t_{AW}	Address Valid to End of Write	9	—	10	—	11	—	
t_{CW}	Chip Enable to End of Write	8	—	9	—	10	—	
t_{AS}	Address Setup Time	0	—	0	—	0	—	
t_{WR}	Write Recovery Time	1	—	1	—	1	—	
t_{OEW}	Output Enable Time from \overline{WE}	1	—	1	—	1	—	
t_{ODW}	Output Disable Time from \overline{WE}	—	6	—	7	—	8	
t_{DS}	Data Setup Time	7	—	8	—	9	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

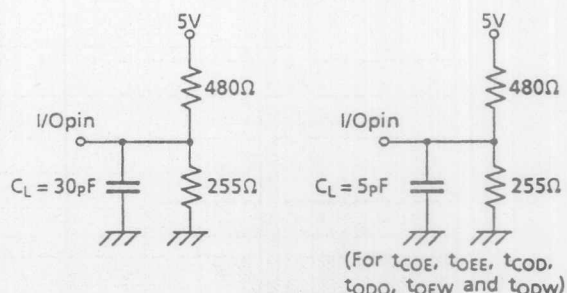
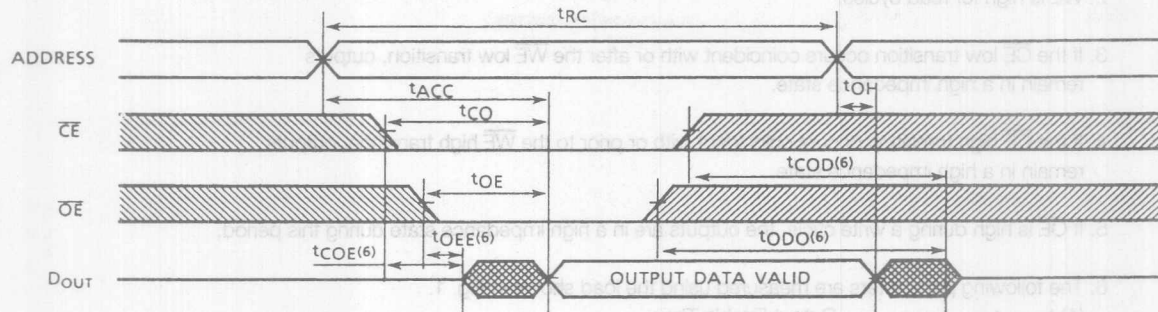
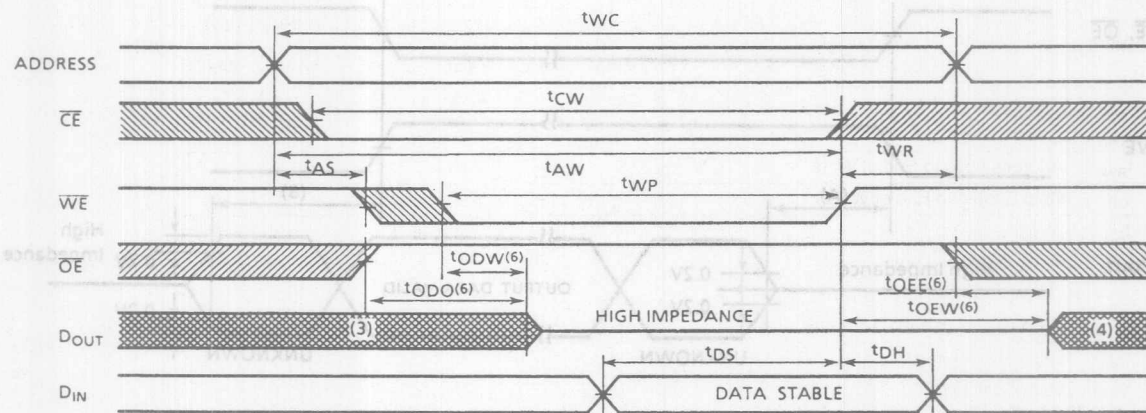
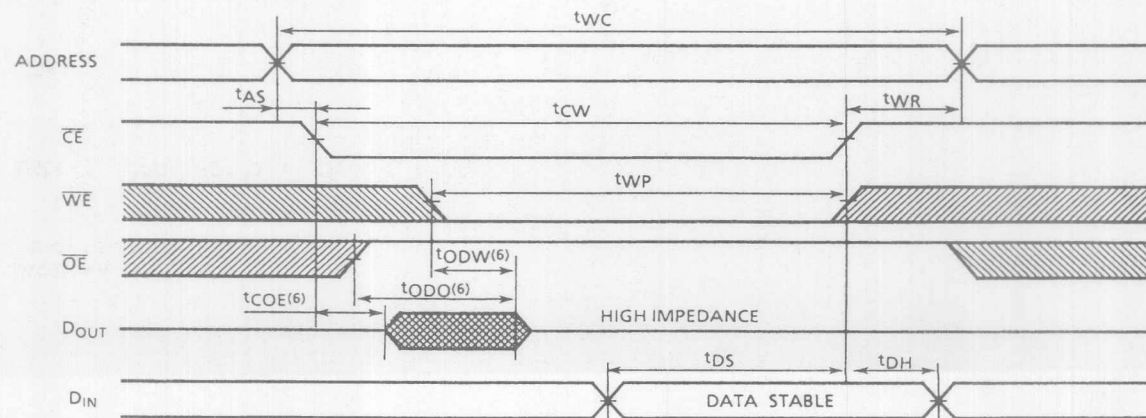


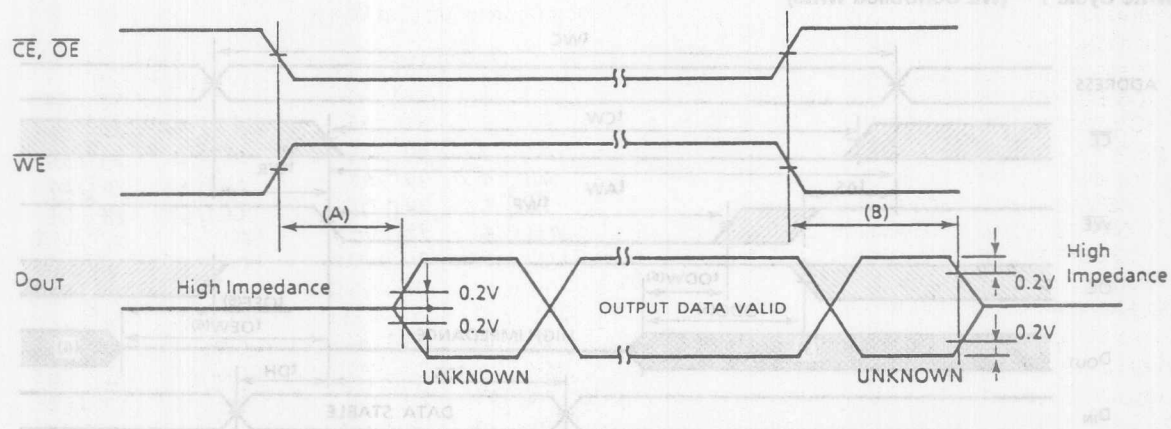
Figure 1.

Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled Write)Write Cycle 2 ⁽⁵⁾ (\overline{CE} Controlled Write)

Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{OE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{OE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{COE} , t_{OEE} , $t_{OE\overline{W}}$ Output Enable Time
 - (B) t_{COD} , t_{ODO} , $t_{OD\overline{W}}$ Output Disable Time



TC55B8128P/J-12/15/20

SILICON GATE BiCMOS

131,072 WORD x 8 BIT BiCMOS STATIC RAM

Description

The TC55B8128P/J is a 1,048,576 bit high speed BiCMOS static random access memory organized as 131,072 words by 8 bits and operated from a single 5V supply. Toshiba's BiCMOS technology and advanced circuit design enable high speed operation.

The TC55B8128P/J features low power dissipation when the device is deselected using chip enable (\overline{CE}), and has an output enable input (\overline{OE}) for fast memory access.

The TC55B8128P/J is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC55B8128P/J is available in a 400mil width, 32-pin DIP and SOJ suitable for high density surface assembly.

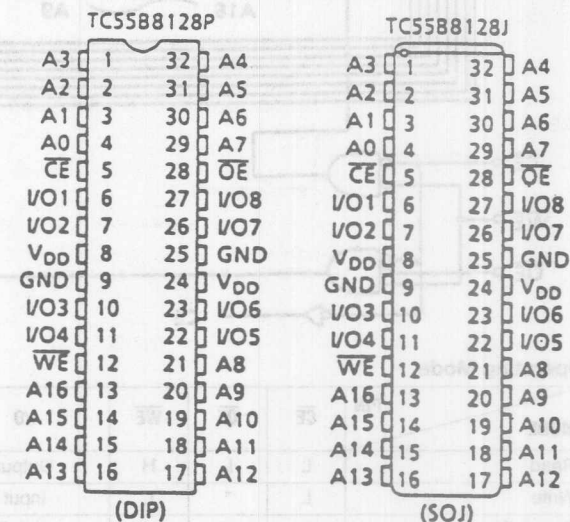
Features

- Fast access time
 - TC55B8128P/J-12 12ns (max.)
 - TC55B8128P/J-15 15ns (max.)
 - TC55B8128P/J-20 20ns (max.)
- Low power dissipation
 - Operation:
 - TC55B8128P/J-12 150mA (max.)
 - TC55B8128P/J-15 150mA (max.)
 - TC55B8128P/J-20 150mA (max.)
 - Standby: 15mA (max.)
- Single 5V power supply: $5V \pm 10\%$
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Package:
 - TC55B8128P: DIP32-P-400
 - TC55B8128J: SOJ32-P-400A

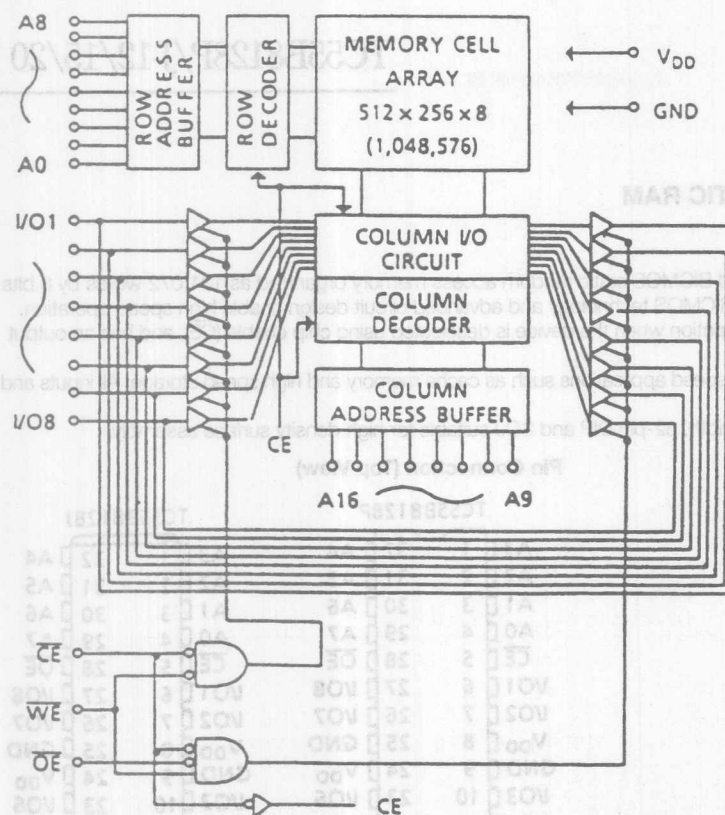
Pin Names

A0 ~ A16	Address Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	\overline{WE}	I/O	POWER
Read		L	L	H	Output	I_{DD0}
Write		L	*	L	Input	I_{DD0}
Output Disabled		L	H	H	High-Z	I_{DD0}
Standby		H	*	*	High-Z	I_{DD5}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0* ~ 7.0	V
V_{IO}	Input/Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	900	mW
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

* -3V with a pulse width of 10ns

- Fast access time
- TC55B8128P-12 12ns (max.)
- TC55B8128P-15 15ns (max.)
- TC55B8128P-20 20ns (max.)
- Low power dissipation
- Operation
- TC55B8128P-12 180mA (max.)
- TC55B8128P-15 180mA (max.)
- TC55B8128P-20 180mA (max.)
- Standby
- 18mA (max.)
- Single 5V power supply 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Package
- TC55B8128P: DIP28-P-400
- TC55B8128P: BOP28-P-400A

Pin Names

A0 - A16	Address inputs
I/O1 - I/O8	Data inputs/outputs
\overline{CE}	Chip Enable input
\overline{WE}	Write Enable input
\overline{OE}	Output Enable input
V_{DD}	Power (=5V)
GND	Ground

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

* -3V with a pulse width of 10ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	8	—	—	mA
I_{DDO}	Operating Current	$t_{\text{cycle}} = \text{Min cycle}$, $\overline{CE} = V_{IL}$, $I_{OUT} = 0\text{mA}$, Other Inputs = V_{IH}/V_{IL}	—	—	150	mA
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V_{IH}/V_{IL}	—	—	30	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2V$, Other Inputs = $V_{DD} - 0.2V$ or $0.2V$	—	—	15	mA

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
C_{IO}	Input/Output Capacitance	$V_{IO} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.



Figure 1

Output Load	Fig. 1
Output Timing Measurement Reference Levels	1.5V
Input Timing Measurement Reference Levels	1.5V
Input Pulse Rise and Fall Time	5ns
Input Pulse Levels	3.0V/0.0V

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55B8128P/J-12		TC55B8128P/J-15		TC55B8128P/J-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	12	—	15	—	20	—	
t_{ACC}	Address Access Time	—	12	—	15	—	20	
t_{CO}	Chip Enable Access Time	—	12	—	15	—	20	
t_{OE}	Output Enable Access Time	—	7	—	8	—	10	
t_{COE}	Output Enable Time from \overline{CE}	4	—	4	—	4	—	ns
t_{COD}	Output Disable Time from \overline{CE}	—	6	—	7	—	8	
t_{OEE}	Output Enable Time from \overline{OE}	0	—	0	—	0	—	
t_{ODO}	Output Disable Time from \overline{OE}	—	5	—	6	—	7	
t_{OH}	Output Data Hold Time from Address Change	4	—	4	—	4	—	

Write Cycle

SYMBOL	PARAMETER	TC55B8128P/J-12		TC55B8128P/J-15		TC55B8128P/J-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	12	—	15	—	20	—	
t_{WP}	Write Pulse Width	8	—	9	—	10	—	
t_{AW}	Address Valid to End of Write	9	—	10	—	11	—	
t_{CW}	Chip Enable to End of Write	8	—	9	—	10	—	
t_{AS}	Address Setup Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	1	—	1	—	1	—	
t_{OEW}	Output Enable Time from \overline{WE}	1	—	1	—	1	—	
t_{ODW}	Output Disable Time from \overline{WE}	—	6	—	7	—	8	
t_{DS}	Data Setup Time	7	—	8	—	9	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

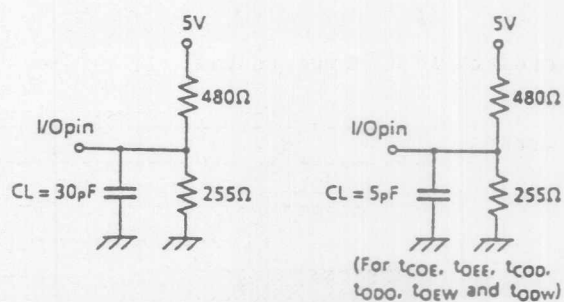
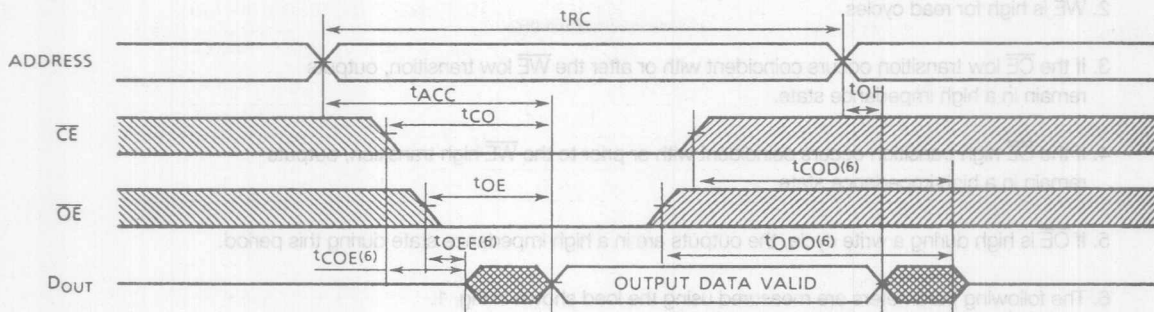
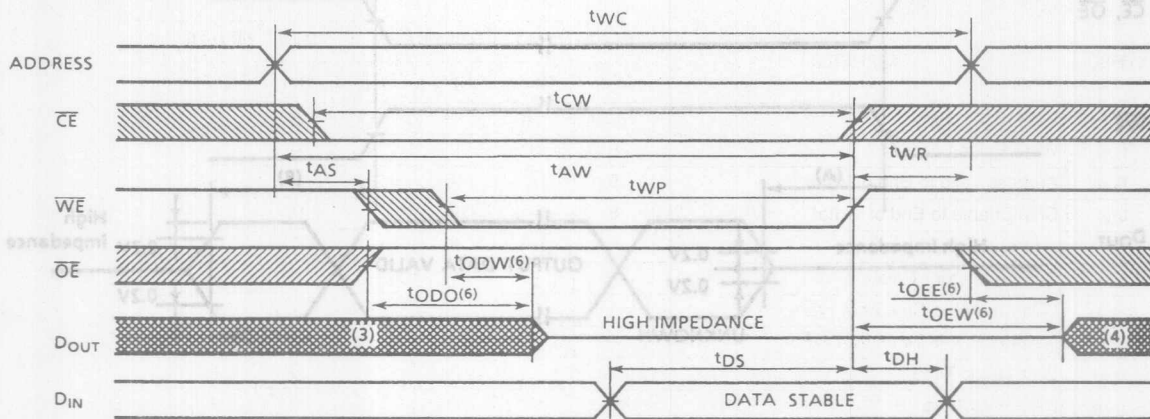
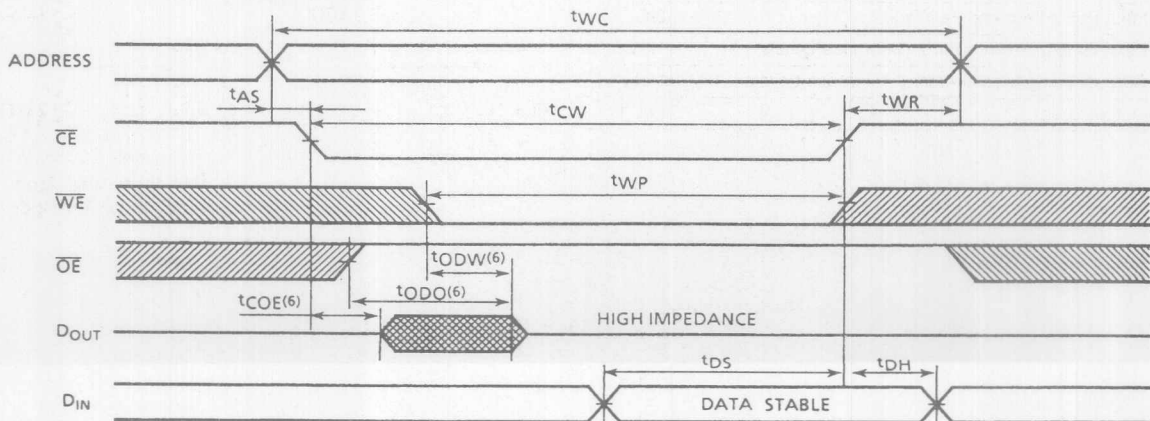


Figure 1.

Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled Write)Write Cycle 2 ⁽⁵⁾ (\overline{CE} Controlled Write)

2. \overline{WE} is high for read cycles.

3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.

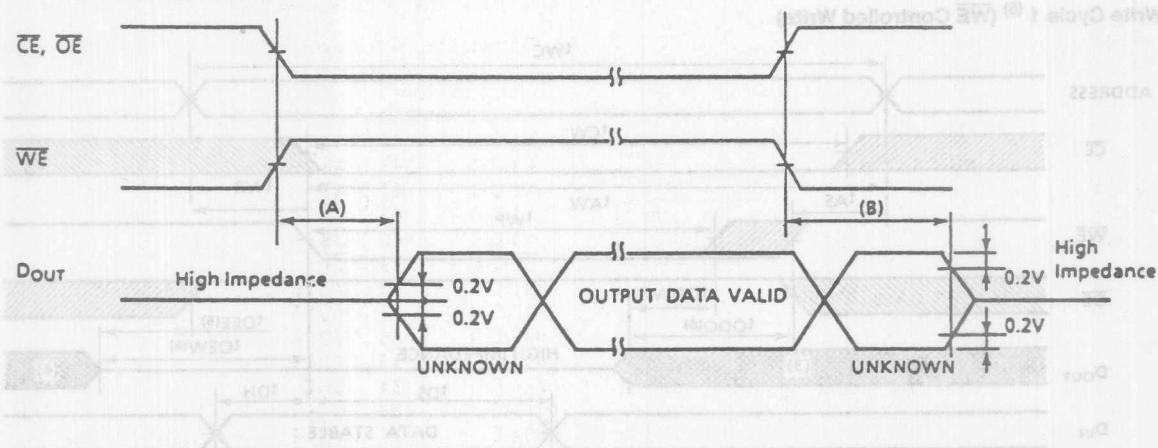
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.

5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.

6. The following parameters are measured using the load shown in Fig. 1.

(A) t_{COE} , t_{OEE} , $t_{OE\overline{W}}$ Output Enable Time

(B) t_{COD} , t_{ODO} , $t_{OD\overline{W}}$ Output Disable Time



SILICON GATE CMOS

65,536 WORD x 16 BIT CMOS STATIC RAM

Description

The TC551664J is a 1,048,576 bit high speed CMOS static random access memory organized as 65,536 words by 16 bits and operated from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC551664J features low power dissipation when the device is deselected using chip enable (\overline{CE}), and has an output enable input (\overline{OE}) for fast memory access. Byte access is supported by upper and lower byte controls.

The TC551664J is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC551664J is available in a 400mil width, 44-pin SOJ suitable for high density surface assembly.

Features

- Fast access time
 - TC551664J -15 15ns (max.)
 - TC551664J -20 20ns (max.)
 - TC551664J -25 25ns (max.)
- Low power dissipation

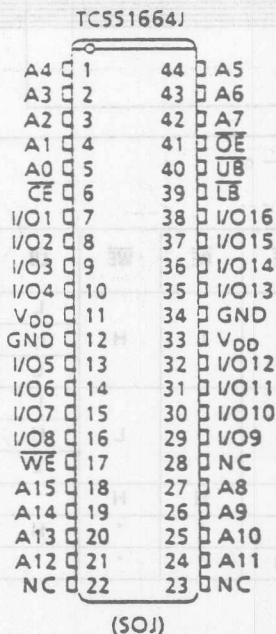
Cycle Time	15	20	25	30	50	ns
Operation (max.)	260	220	200	180	150	mA

- Standby: 1mA (max.)
- Single 5V power supply: $5V \pm 10\%$
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Data byte controls: \overline{LB} , \overline{UB}
- Package: SOJ44-P-400

Pin Names

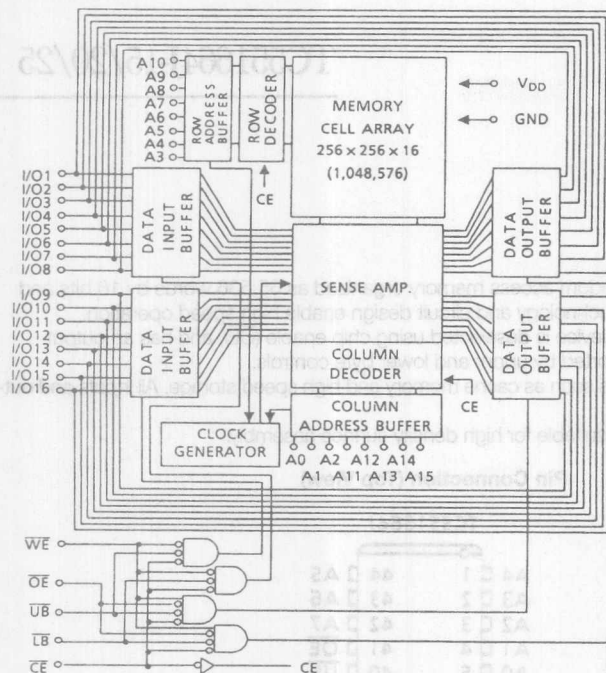
A0 ~ A15	Address Inputs
I/O1 ~ I/O16	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
\overline{LB} , \overline{UB}	Data Byte Control Inputs
V_{DD}	Power (+5V)
GND	Ground
NC	No Connection

Pin Connection (Top View)



UNIT	RATING	ITEM	SYMBOL
V	-0.5 ~ 7.0	Power Supply Voltage	V_{DD}
V	-2.0 ~ -1.0	Input Voltage	V_{in}
V	0.2 ~ $V_{DD} + 0.5$	Input/Output Voltage	V_{IO}
W	1.5	Power Dissipation	P_D
°C	250 ~ 10	Storage Temperature	T_{STG}
°C	-65 ~ 150	Operating Temperature	T_{OP}

Block Diagram



Operating Mode

MODE \ PIN	\overline{CE}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O1 ~ I/O8	I/O9 ~ I/O16	POWER
Read	L	L	H	L	L	Output	Output	I _{DDO}
				H	L	High Impedance	Output	I _{DDO}
				L	H	Output	High Impedance	I _{DDO}
Write	L	*	L	L	L	Input	Input	I _{DDO}
				H	L	High Impedance	Input	I _{DDO}
				L	H	Input	High Impedance	I _{DDO}
Output Disable	L	H	H	*	*	High Impedance	High Impedance	I _{DDO}
	L	*	*	H	H	High Impedance	High Impedance	I _{DDO}
Standby	H	*	*	*	*	High Impedance	High Impedance	I _{DDO}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V _{IN}	Input Voltage	-2.0* ~ 7.0	V
V _{I/O}	Input/Output Voltage	-0.5* ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.5	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-65 ~ 150	°C
T _{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

* -3V with a pulse width of 10ns

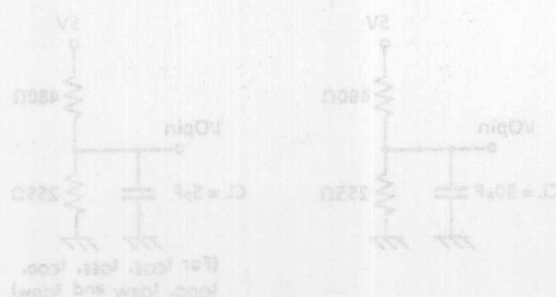
DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	8	—	—	mA
I_{DDO}	Operating Current	$\overline{CE} = V_{IL}$, $I_{OUT} = 0\text{mA}$, Other Inputs = V_{IH}/V_{IL}	$t_{\text{cycle}} = 15\text{ns}$	—	—	260
			$t_{\text{cycle}} = 20\text{ns}$	—	—	220
			$t_{\text{cycle}} = 25\text{ns}$	—	—	200
			$t_{\text{cycle}} = 30\text{ns}$	—	—	180
			$t_{\text{cycle}} = 50\text{ns}$	—	—	150
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V_{IH}/V_{IL}	—	—	30	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2\text{V}$ Other Inputs = $V_{DD} - 0.2\text{V}$ or 0.2V	—	—	1	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.



Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	50Ω

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC551664J -15		TC551664J -20		TC551664J -25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	—	20	—	25	—	ns
t_{ACC}	Address Access Time	—	15	—	20	—	25	
t_{CO}	\overline{CE} Access Time	—	15	—	20	—	25	
t_{OE}	\overline{OE} Access Time	—	8	—	10	—	12	
t_{BA}	\overline{UB} , \overline{LB} Access Time	—	8	—	10	—	12	
t_{OH}	Output Data Hold Time from Address Change	5	—	5	—	5	—	
t_{COE}	Output Enable Time from \overline{CE}	5	—	5	—	5	—	
t_{OEE}	Output Enable Time from \overline{OE}	1	—	1	—	1	—	
t_{BE}	Output Enable Time from \overline{UB} , \overline{LB}	1	—	1	—	1	—	
t_{COD}	Output Disable Time from \overline{CE}	—	8	—	8	—	8	
t_{ODO}	Output Disable Time from \overline{OE}	—	8	—	8	—	8	
t_{BD}	Output Disable Time from \overline{UB} , \overline{LB}	—	8	—	8	—	8	

Write Cycle

SYMBOL	PARAMETER	TC551664J -15		TC551664J -20		TC551664J -25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	—	20	—	25	—	ns
t_{WP}	Write Pulse Width	9	—	10	—	12	—	
t_{CW}	Chip Enable to End of Write	12	—	13	—	15	—	
t_{BW}	\overline{UB} , \overline{LB} Enable to End of Write	9	—	12	—	14	—	
t_{AW}	Address Valid to End of Write	9	—	12	—	14	—	
t_{AS}	Address Setup Time	0	—	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{DS}	Data Setup Time	8	—	10	—	10	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	
t_{OEW}	Output Enable Time from \overline{WE}	1	—	1	—	1	—	
t_{ODW}	Output Disable Time from \overline{WE}	—	8	—	8	—	8	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

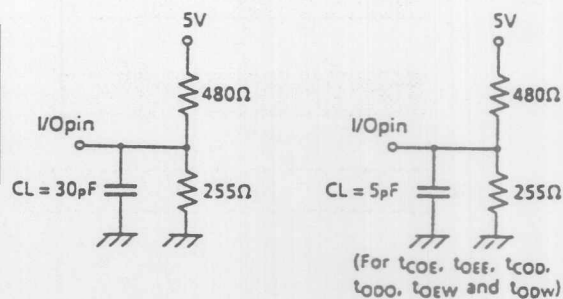
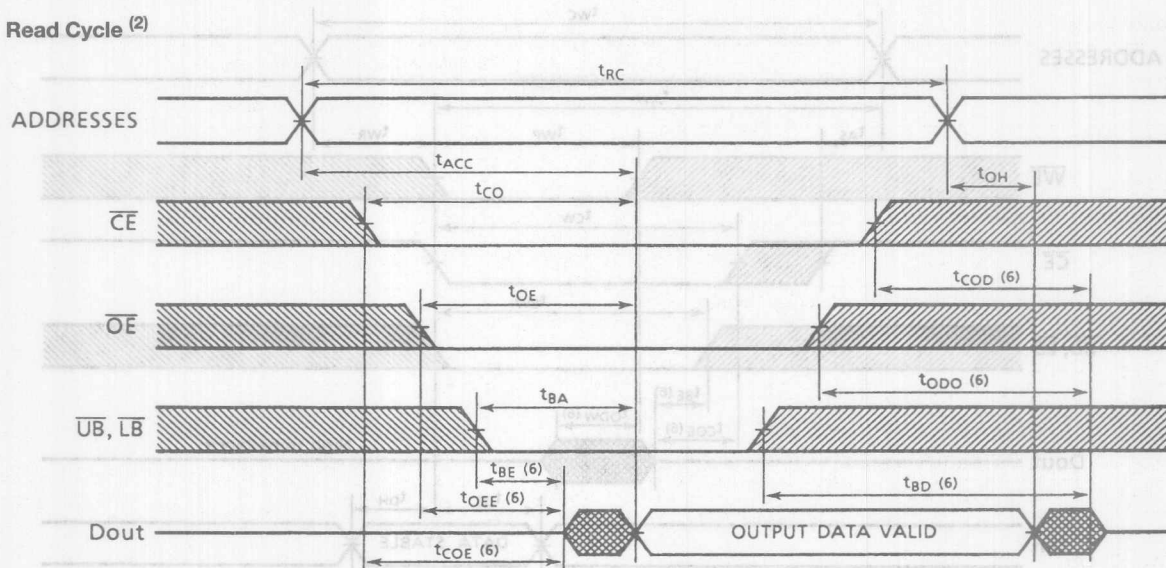
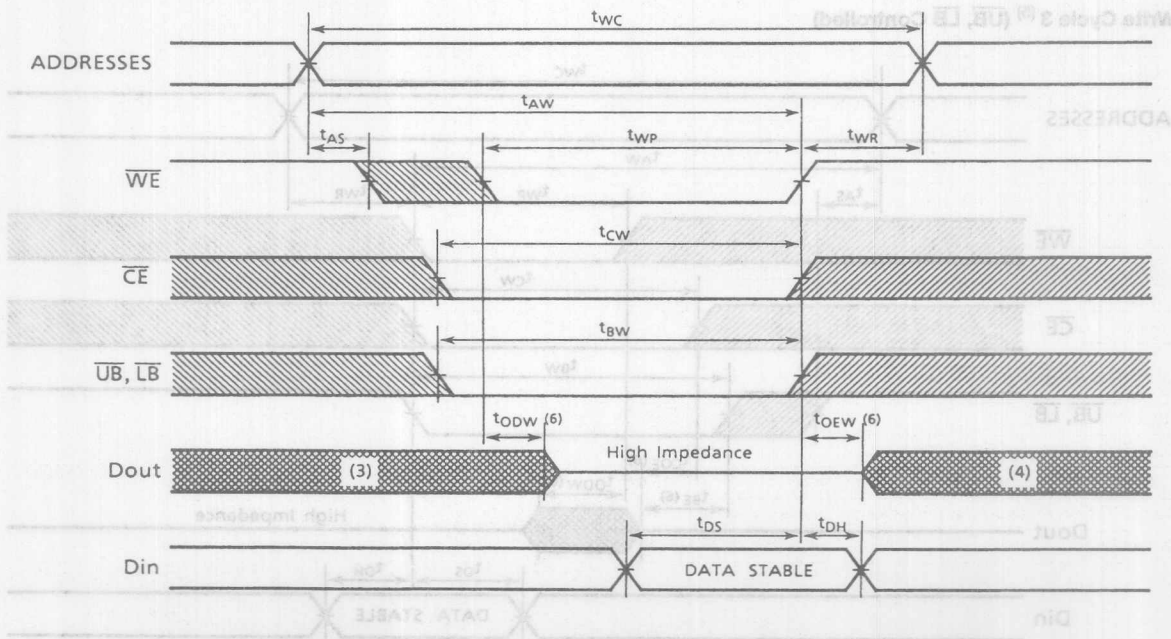
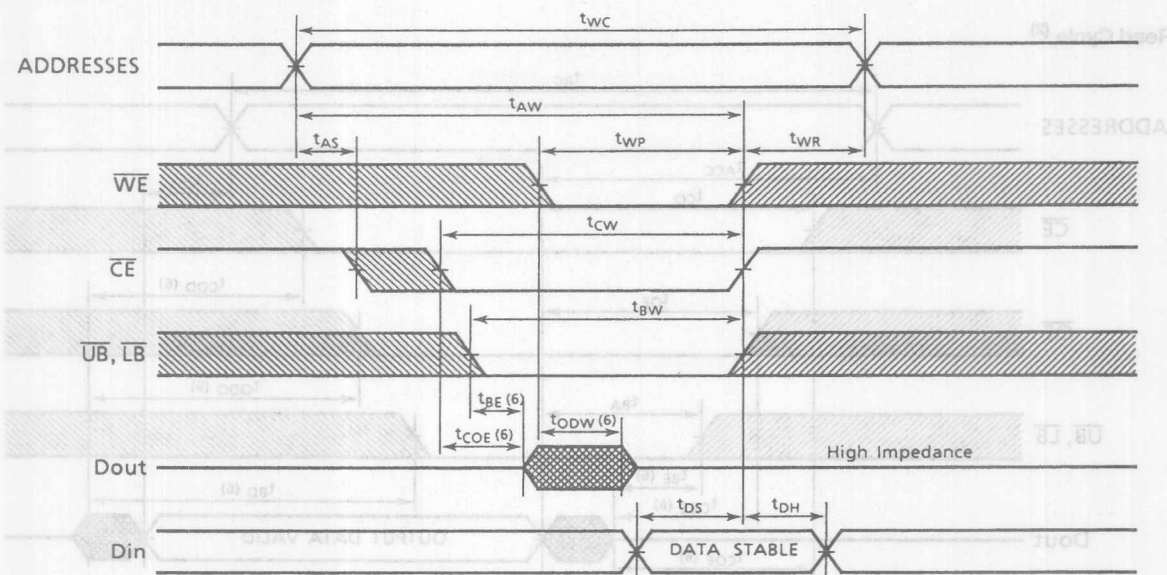
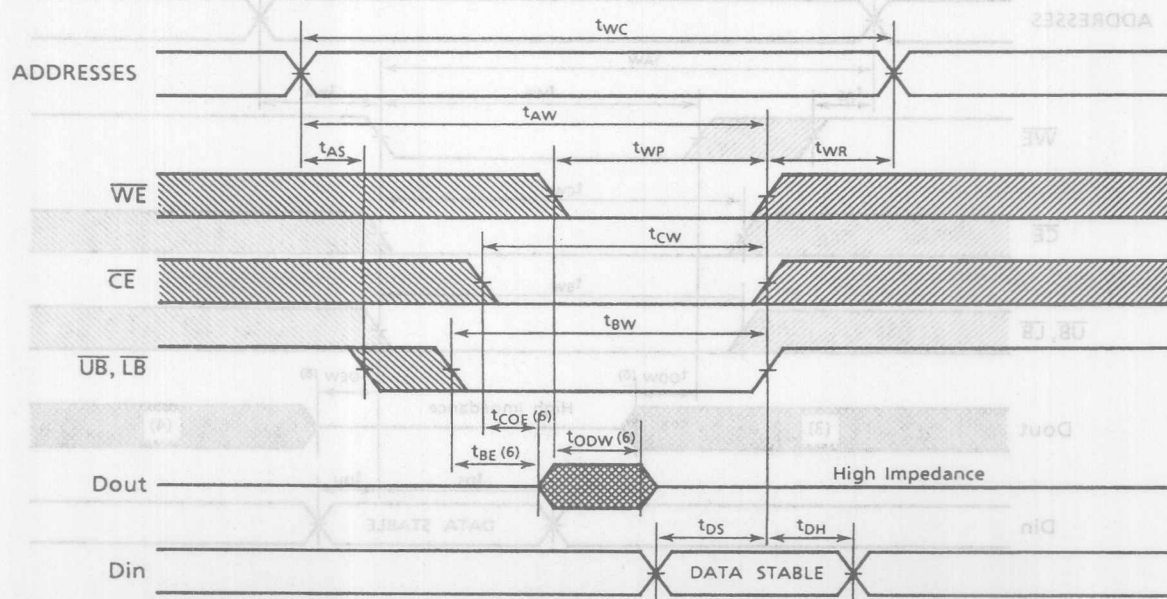


Figure 1.

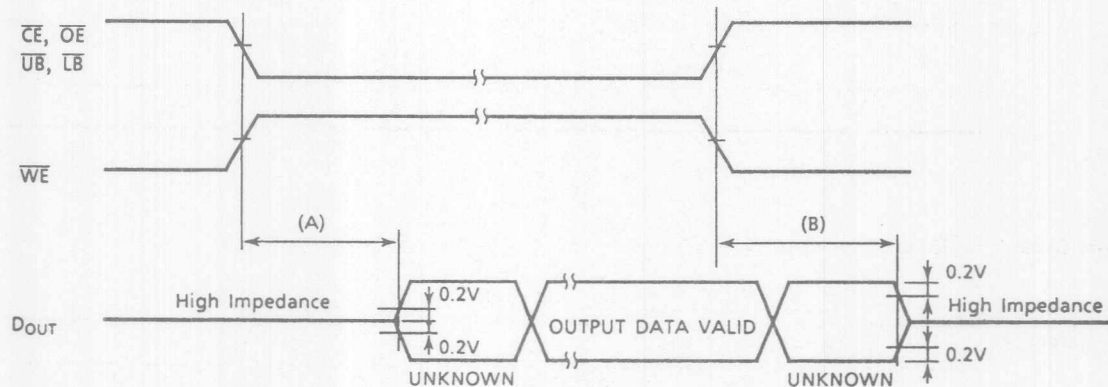
Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled)

Write Cycle 2 ⁽⁵⁾ ($\overline{\text{CE}}$ Controlled)Write Cycle 3 ⁽⁵⁾ ($\overline{\text{UB}}, \overline{\text{LB}}$ Controlled)

Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{COE} , t_{OEE} , t_{BE} , $t_{OE\overline{W}}$ Output Enable Time
 - (B) t_{COD} , t_{ODO} , t_{BD} , $t_{OD\overline{W}}$ Output Disable Time

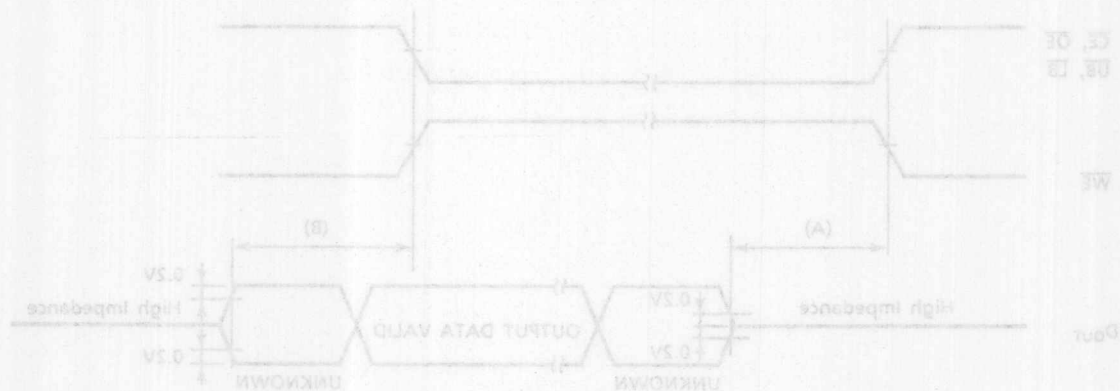


Notes

Notes:

1. The operating temperature (T_A) is guaranteed with transistor air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.

- (A) $t_{OE} \text{ low} \rightarrow \text{low}$ Output Enable Time
 (B) $t_{OD} \text{ low} \rightarrow \text{low}$ Output Disable Time



TC55V1664J/FT-10/12/15

PRELIMINARY

SILICON GATE CMOS

65,536 WORD x 16 BIT CMOS STATIC RAM

Description

The TC55V1664J/FT is a 1,048,576 bit high speed CMOS static random access memory organized as 65,536 words by 16 bits and operated from a single 3.3V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC55V1664J/FT features low power dissipation when the device is deselected using chip enable (\overline{CE}), and has an output enable input (\overline{OE}) for fast memory access. Byte access is supported by upper and lower byte controls.

The TC55V1664J/FT is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are LVTTTL compatible.

The TC55V1664J/FT is available in a 400mil width, 44-pin plastic SOJ and thin small outline package (forward type) suitable for high density surface assembly.

Features

- Fast access time
 - TC55V1664J/FT -10 10ns (max.)
 - TC55V1664J/FT -12 12ns (max.)
 - TC55V1664J/FT -15 15ns (max.)
- Low power dissipation

Cycle Time	10	12	15	20	30	ns
Operation (max.)	260	220	200	180	150	mA

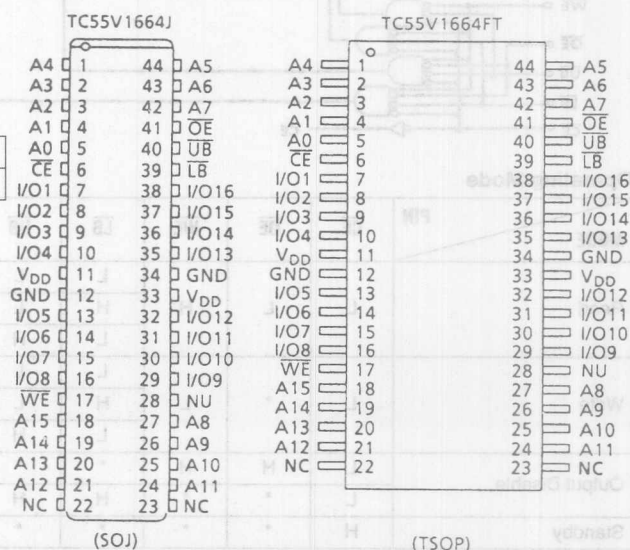
- Standby: 1mA (max.)
- Single 3.3V power supply: 3.3V±0.3V
- Fully static operation
- Inputs and outputs LVTTTL compatible
- Output buffer control: \overline{OE}
- Data byte controls: \overline{LB} , \overline{UB}
- Package
 - TC55V1664J: SOJ44-P-400
 - TC55V1664FT: TSOP44-P-400

Pin Names

Pin	Name
A0 ~ A15	Address Inputs
I/O1 ~ I/O16	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
\overline{LB} , \overline{UB}	Data Byte Control Inputs
V_{DD}	Power (+3.3V)
GND	Ground
NC	No Connection
NU*	Not Usable (Input)

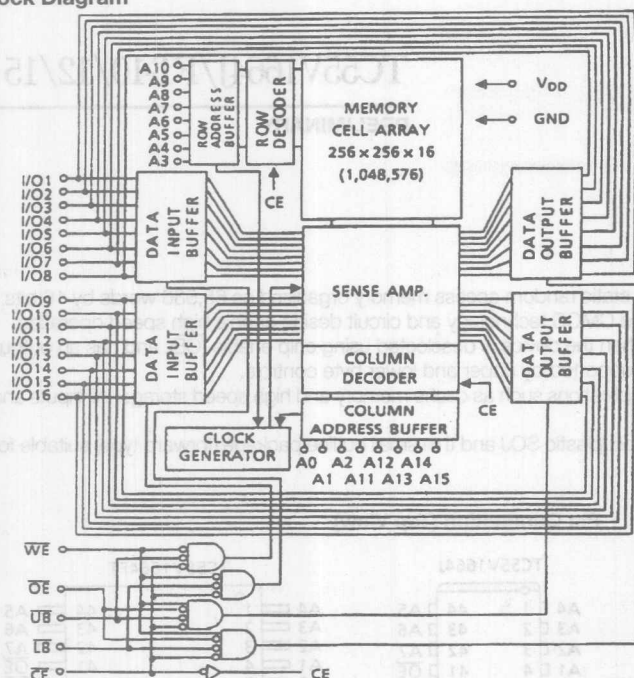
* The NU pin must be kept electronically open, pulled down to GND, or less than 0.8V. Applying a voltage greater than 0.8V to the NU pin is prohibited.

Pin Connection (Top View)



UNIT	RATING	TEST	SYMBOL
V	-0.5 ~ -1.5	Power Supply Voltage	V_{DD}
V	-0.5 ~ -1.5	Input Voltage	V_{in}
V	0.5 ~ $V_{DD} + 0.5$	Output Voltage	V_{out}
W	1.2	Power Dissipation	P_D
°C	25 ~ 125	Storage Temperature	T_{STG}
°C	-10 ~ 55	Operating Temperature	T_{OP}

Block Diagram



Operating Mode

MODE	PIN	CE	OE	WE	LB	UB	I/O1 ~ I/O8	I/O9 ~ I/O16	POWER
Read		L	L	H	L	L	Output	Output	I _{DDO}
					H	L	High Impedance	Output	I _{DDO}
					L	H	Output	High Impedance	I _{DDO}
Write		L	*	L	L	L	Input	Input	I _{DDO}
					H	L	High Impedance	Input	I _{DDO}
					L	H	Input	High Impedance	I _{DDO}
Output Disable		L	H	H	*	*	High Impedance	High Impedance	I _{DDO}
		L	*	*	H	H	High Impedance	High Impedance	I _{DDO}
Standby		H	*	*	*	*	High Impedance	High Impedance	I _{DDS}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 4.6	V
V _{IN}	Input Voltage	-0.5* ~ 4.6	V
V _{IO}	Input/Output Voltage	-0.5* ~ V _{DD} + 0.5**	V
P _D	Power Dissipation	1.2	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-65 ~ 150	°C
T _{OPR}	Operating Temperature	-10 ~ 85	°C

** Not yet specified

AC Characteristics ($T_a = 0 - 70^\circ\text{C}$), $V_{DD} = 3.3\text{V} \pm 0.2\text{V}$

	MIN.	TYP.	MAX.	UNIT
	—	—	±1	μA
	—	—	±1	μA
	-1	—	20	μA
	—	—	±1	
	2.4	—	—	V
	$V_{DD} - 0.2$	—	—	
	—	—	0.4	
	—	—	0.2	
ns	—	—	260	
ns	—	—	220	mA
ns	—	—	200	
ns	—	—	180	
ns	—	—	150	
	—	—	20	mA
	—	—	1	

	MAX.	UNIT
	6	pF
	8	pF

AC Test Conditions

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

Read Cycle

SYMBOL	PARAMETER	TC55V1664J/FT -10		TC55V1664J/FT -12		TC55V1664J/FT -15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	—	12	—	15	—	
t_{ACC}	Address Access Time	—	10	—	12	—	15	
t_{CO}	\overline{CE} Access Time	—	10	—	12	—	15	
t_{OE}	\overline{OE} Access Time	—	5	—	6	—	8	
t_{BA}	\overline{UB} , \overline{LB} Access Time	—	5	—	6	—	8	
t_{OH}	Output Data Hold Time from Address Change	3	—	3	—	3	—	ns
t_{COE}	Output Enable Time from \overline{CE}	3	—	3	—	3	—	
t_{OEE}	Output Enable Time from \overline{OE}	1	—	1	—	1	—	
t_{BE}	Output Enable Time from \overline{UB} , \overline{LB}	1	—	1	—	1	—	
t_{COD}	Output Disable Time from \overline{CE}	—	6	—	7	—	8	
t_{ODO}	Output Disable Time from \overline{OE}	—	6	—	7	—	8	
t_{BD}	Output Disable Time from \overline{UB} , \overline{LB}	—	6	—	7	—	8	

Write Cycle

SYMBOL	PARAMETER	TC55V1664J/FT -10		TC55V1664J/FT -12		TC55V1664J/FT -15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	—	12	—	15	—	
t_{WP}	Write Pulse Width	7	—	8	—	9	—	
t_{CW}	Chip Enable to End of Write	9	—	10	—	11	—	
t_{BW}	\overline{UB} , \overline{LB} Enable to End of Write	9	—	10	—	11	—	
t_{AW}	Address Valid to End of Write	9	—	10	—	11	—	
t_{AS}	Address Setup Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{DS}	Data Setup Time	6	—	7	—	8	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	
t_{OEW}	Output Enable Time from \overline{WE}	1	—	1	—	1	—	
t_{ODW}	Output Disable Time from \overline{WE}	—	6	—	7	—	8	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

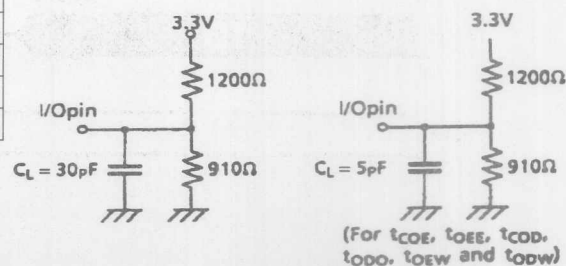
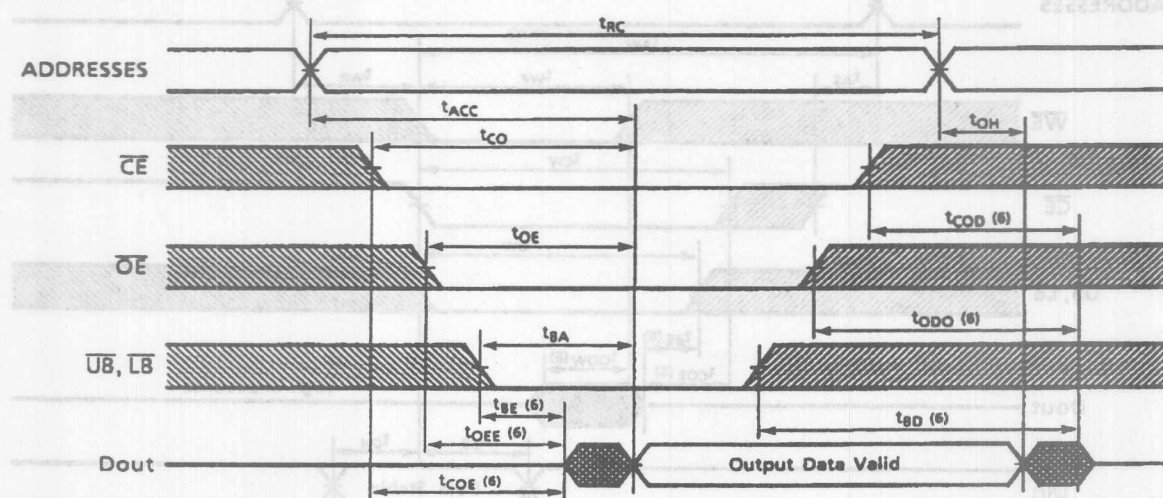
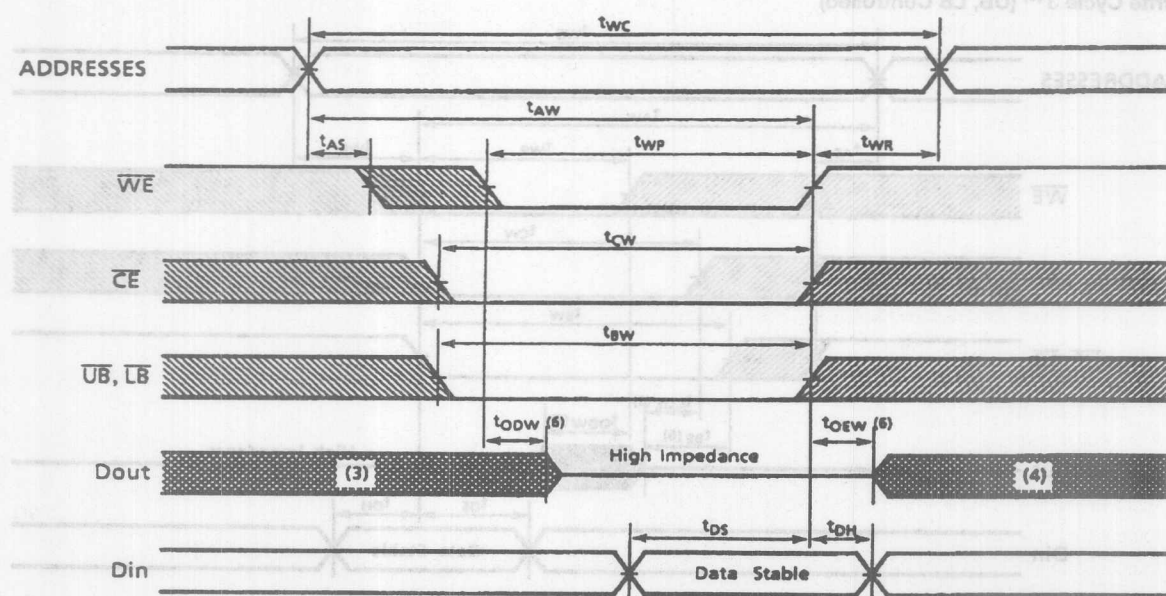
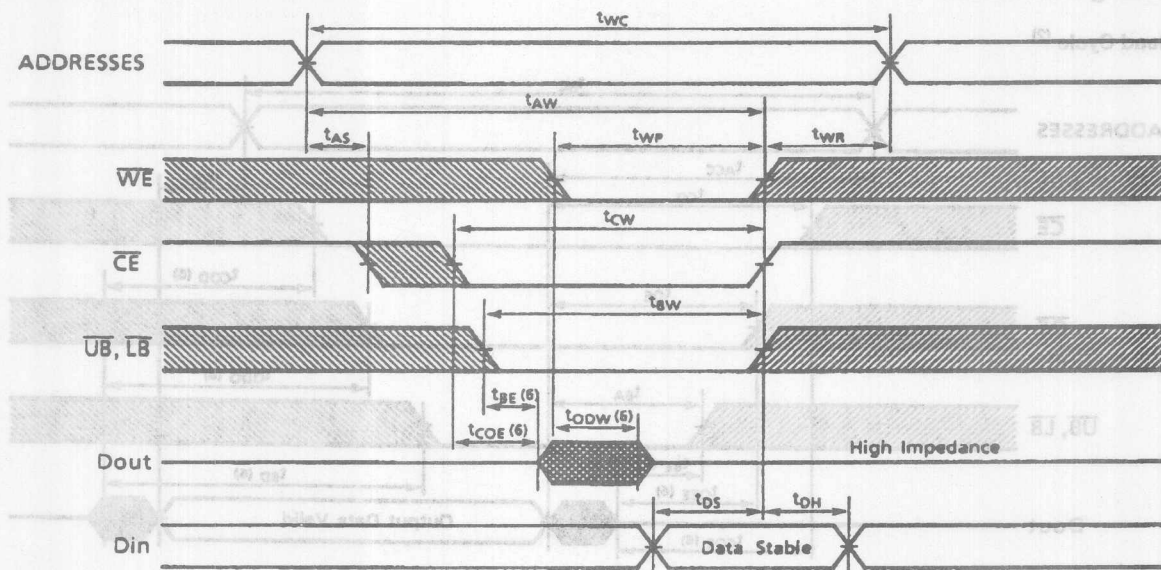
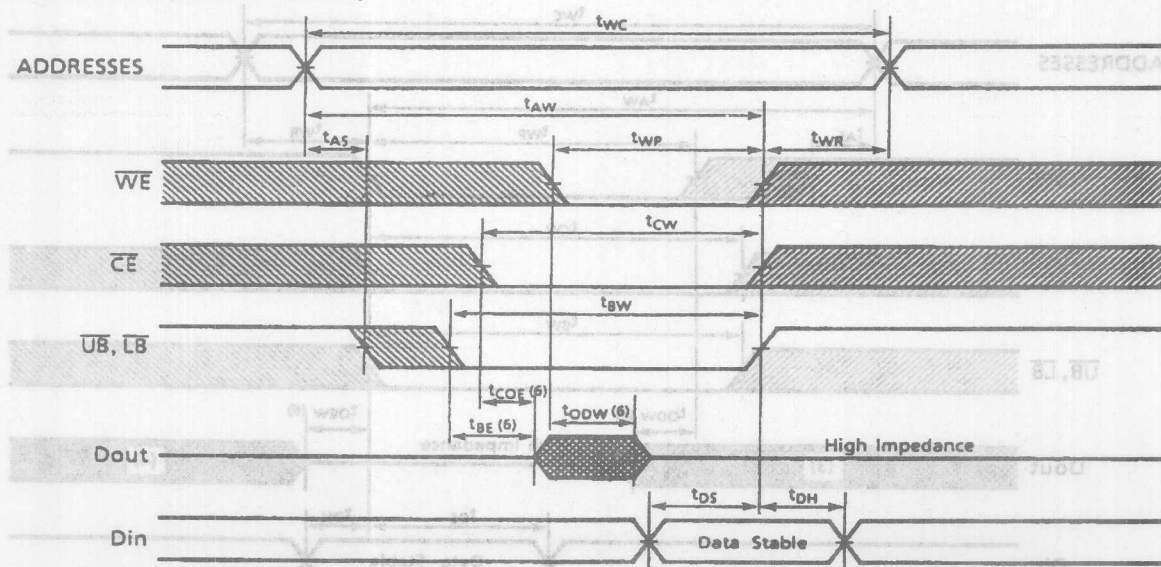


Figure 1.

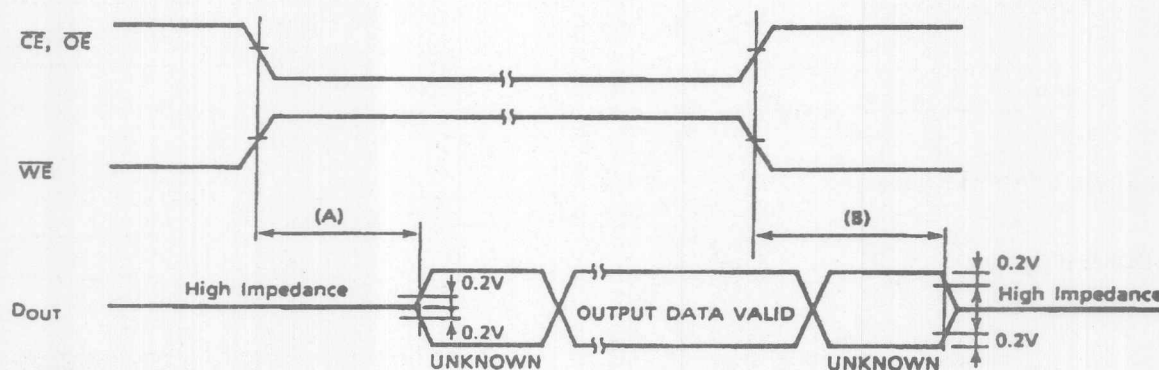
Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled)

Write Cycle 2 ⁽⁵⁾ (\overline{CE} Controlled)Write Cycle 3 ⁽⁵⁾ ($\overline{UB}, \overline{LB}$ Controlled)

Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 (A) t_{COE} , t_{OEE} , t_{BE} , $t_{OE\overline{W}}$ Output Enable Time
 (B) t_{COD} , t_{ODO} , t_{BD} , $t_{OD\overline{W}}$ Output Disable Time



Notes

TC55V1864J/FT-10/12/15

PRELIMINARY

SILICON GATE CMOS

65,536 WORD x 18 BIT CMOS STATIC RAM

Description

The TC55V1864J/FT is a 1,179,648 bit high speed CMOS static random access memory organized as 65,536 words by 18 bits and operated from a single 3.3V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC55V1864J/FT features low power dissipation when the device is deselected using chip enable (\overline{CE}), and has an output enable input (\overline{OE}) for fast memory access. Byte access is supported by upper and lower byte controls.

The TC55V1864J/FT is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are LVTTTL compatible.

The TC55V1864J/FT is available in a 400mil width, 44-pin plastic SOJ and thin small outline package (forward type) suitable for high density surface assembly.

Features

- Fast access time
 - TC55V1864J/FT -10 10ns (max.)
 - TC55V1864J/FT -12 12ns (max.)
 - TC55V1864J/FT -15 15ns (max.)
- Low power dissipation

Cycle Time	10	12	15	20	30	ns
Operation (max.)	260	220	200	180	150	mA

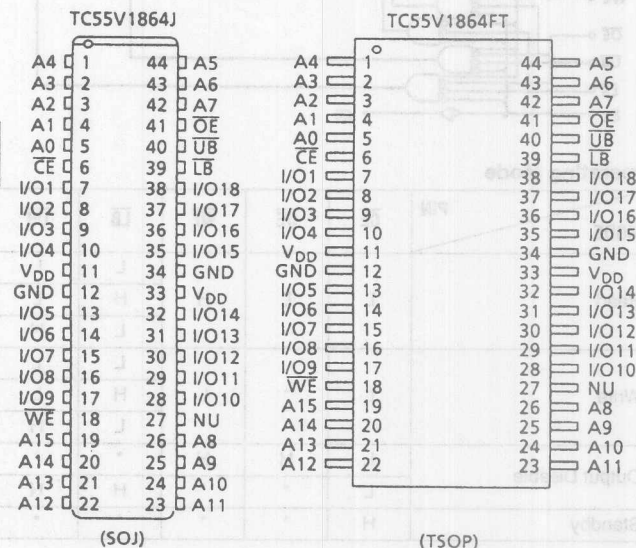
- Standby: 1mA (max.)
- Single 3.3V power supply: 3.3V \pm 0.3V
- Fully static operation
- Inputs and outputs LVTTTL compatible
- Output buffer control: \overline{OE}
- Data byte controls: \overline{LB} , \overline{UB}
- Package
 - TC55V1864J: SOJ44-P-400
 - TC55V1864FT: TSOP44-P-400

Pin Names

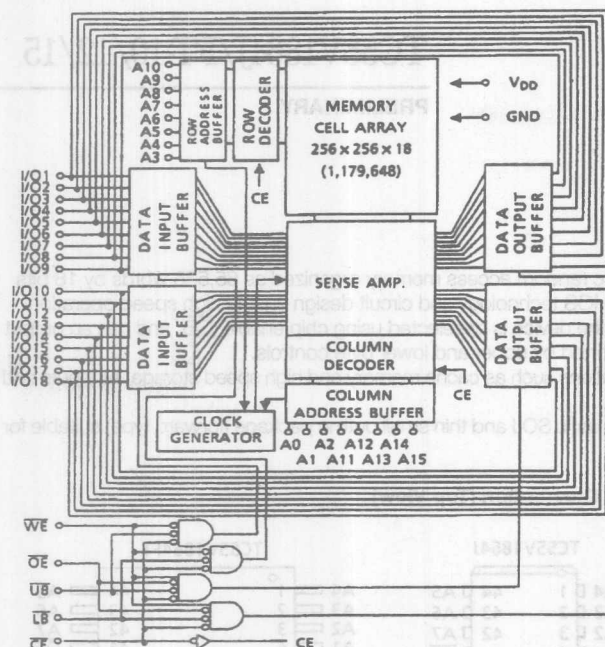
A0 ~ A15	Address Inputs
I/O1 ~ I/O18	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
\overline{LB} , \overline{UB}	Data Byte Control Inputs
V _{DD}	Power (+3.3V)
GND	Ground
NU*	Not Usable (Input)

* The NU pin must be kept electronically open, pulled down to GND, or less than 0.8V. Applying a voltage greater than 0.8V to the NU pin is prohibited.

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE \ PIN	\overline{CE}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O1 ~ I/O9	I/O10 ~ I/O18	POWER
Read	L	L	H	L	L	Output	Output	I _{DDO}
				H	L	High Impedance	Output	I _{DDO}
				L	H	Output	High Impedance	I _{DDO}
Write	L	*	L	L	L	Input	Input	I _{DDO}
				H	L	High Impedance	Input	I _{DDO}
				L	H	Input	High Impedance	I _{DDO}
Output Disable	L	H	H	*	*	High Impedance	High Impedance	I _{DDO}
	L	*	*	H	H	High Impedance	High Impedance	I _{DDO}
Standby	H	*	*	*	*	High Impedance	High Impedance	I _{DDS}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 4.6	V
V _{IN}	Input Voltage	-0.5* ~ 4.6	V
V _{I/O}	Input/Output Voltage	-0.5* ~ V _{DD} + 0.5**	V
P _D	Power Dissipation	1.2	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-65 ~ 150	°C
T _{OPR}	Operating Temperature	-10 ~ 85	°C

*/** Not yet specified

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	—	$V_{DD} + 0.3^{**}$	V
V_{IL}	Input Low Voltage	-0.3*	—	0.8	V

*/** Not yet specified

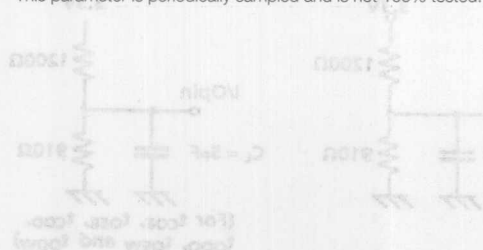
DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current (except NU Pin)	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1	μA
$I_{I(NU)}$	Input Current (NU Pin)	$V_{IN} = 0 \sim 0.8\text{V}$ $V_{IN} = 0 \sim 0.2\text{V}$	-1	—	20	μA
V_{OH}	Output High Voltage	$I_{OH} = -2\text{mA}$ $I_{OH} = -20\mu\text{A}$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2\text{mA}$ $I_{OL} = 20\mu\text{A}$	—	—	0.4	V
I_{DDO}	Operating Current	$\overline{CE} = V_{IL}$, $I_{OUT} = 0\text{mA}$, Other Inputs = V_{IH}/V_{IL}	—	—	260	mA
		$t_{\text{cycle}} = 10\text{ns}$	—	—	220	
		$t_{\text{cycle}} = 12\text{ns}$	—	—	200	
		$t_{\text{cycle}} = 15\text{ns}$	—	—	180	
		$t_{\text{cycle}} = 20\text{ns}$	—	—	150	
		$t_{\text{cycle}} = 30\text{ns}$	—	—	—	
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V_{IH}/V_{IL}	—	—	20	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2\text{V}$ Other Inputs = $V_{DD} - 0.2\text{V}$ or 0.2V	—	—	1	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.



AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

Read Cycle

SYMBOL	PARAMETER	TC55V1864J/FT -10		TC55V1864J/FT -12		TC55V1864J/FT -15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{ACC}	Address Access Time	—	10	—	12	—	15	
t_{CO}	\overline{CE} Access Time	—	10	—	12	—	15	
t_{OE}	\overline{OE} Access Time	—	5	—	6	—	8	
t_{BA}	\overline{UB} , \overline{LB} Access Time	—	5	—	6	—	8	
t_{OH}	Output Data Hold Time from Address Change	3	—	3	—	3	—	
t_{COE}	Output Enable Time from \overline{CE}	3	—	3	—	3	—	
t_{OEE}	Output Enable Time from \overline{OE}	1	—	1	—	1	—	
t_{BE}	Output Enable Time from \overline{UB} , \overline{LB}	1	—	1	—	1	—	
t_{COD}	Output Disable Time from \overline{CE}	—	6	—	7	—	8	
t_{ODO}	Output Disable Time from \overline{OE}	—	6	—	7	—	8	
t_{BD}	Output Disable Time from \overline{UB} , \overline{LB}	—	6	—	7	—	8	

Write Cycle

SYMBOL	PARAMETER	TC55V1864J/FT -10		TC55V1864J/FT -12		TC55V1864J/FT -15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{WP}	Write Pulse Width	7	—	8	—	9	—	
t_{CW}	Chip Enable to End of Write	9	—	10	—	11	—	
t_{BW}	\overline{UB} , \overline{LB} Enable to End of Write	9	—	10	—	11	—	
t_{AW}	Address Valid to End of Write	9	—	10	—	11	—	
t_{AS}	Address Setup Time	0	—	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{DS}	Data Setup Time	6	—	7	—	8	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	
t_{OEW}	Output Enable Time from \overline{WE}	1	—	1	—	1	—	
t_{ODW}	Output Disable Time from \overline{WE}	—	6	—	7	—	8	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

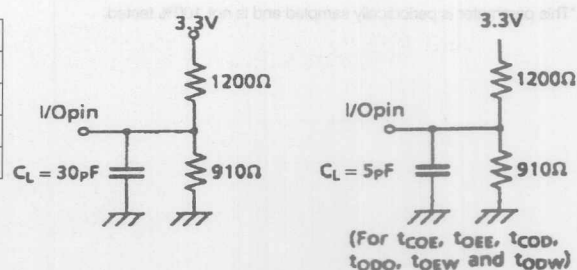
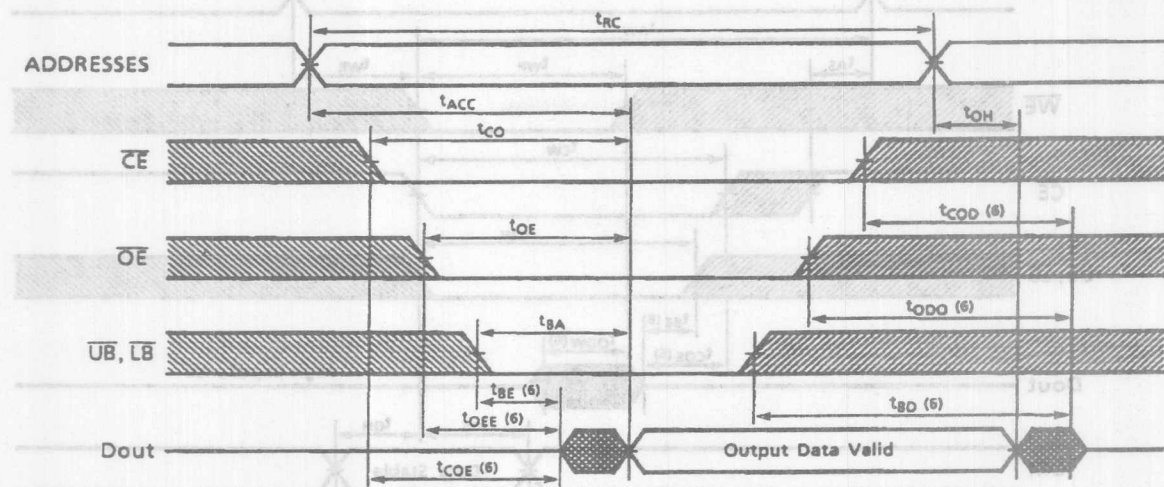
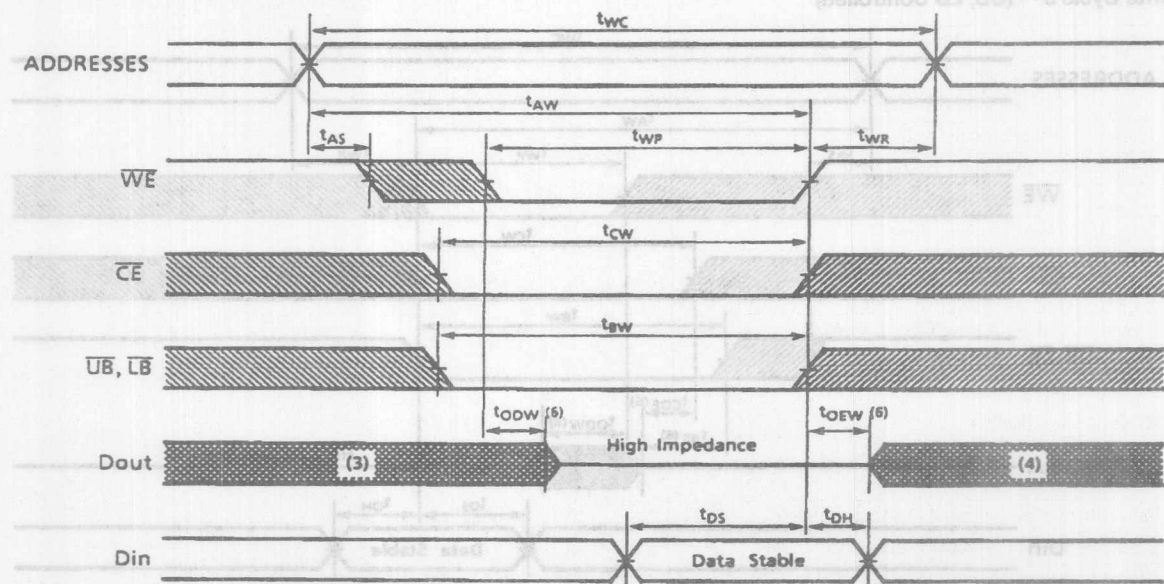
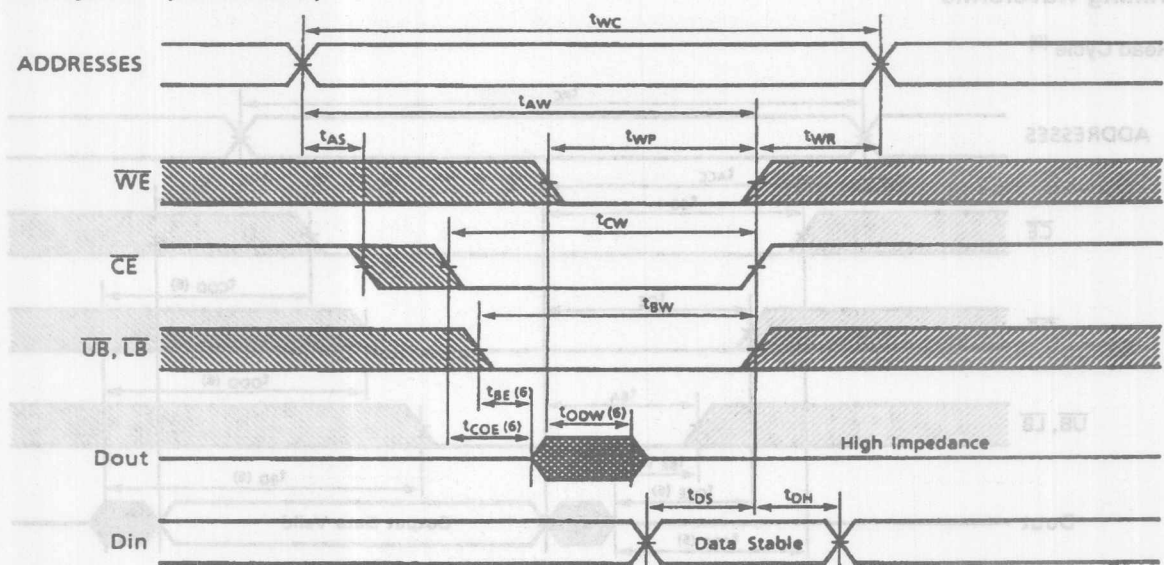
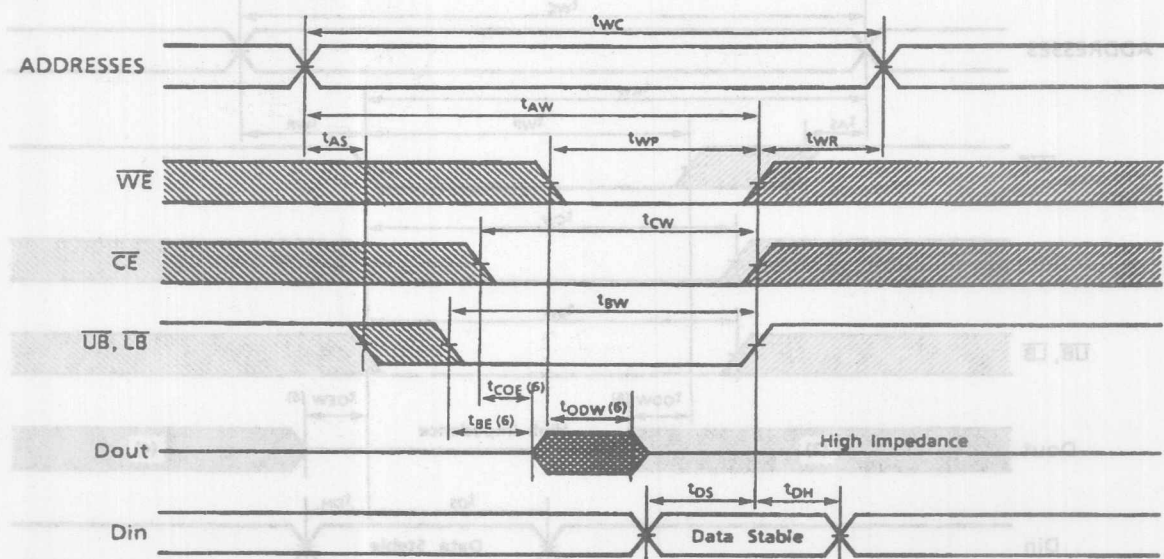


Figure 1.

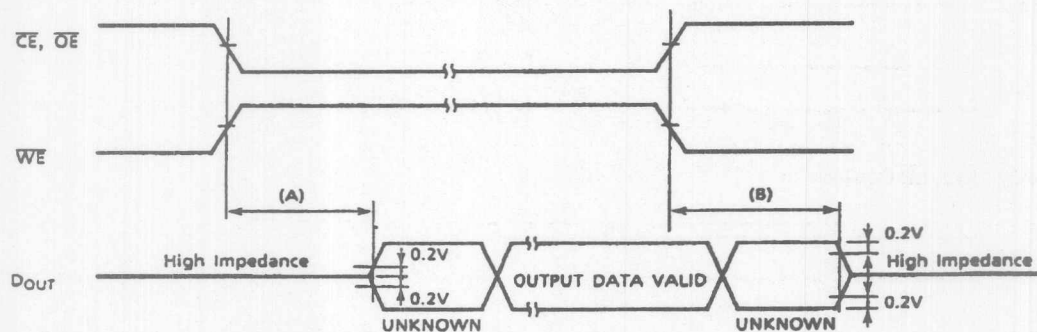
Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled)

Write Cycle 2 ⁽⁵⁾ (\overline{CE} Controlled)Write Cycle 3 ⁽⁵⁾ ($\overline{UB}, \overline{LB}$ Controlled)

Notes:

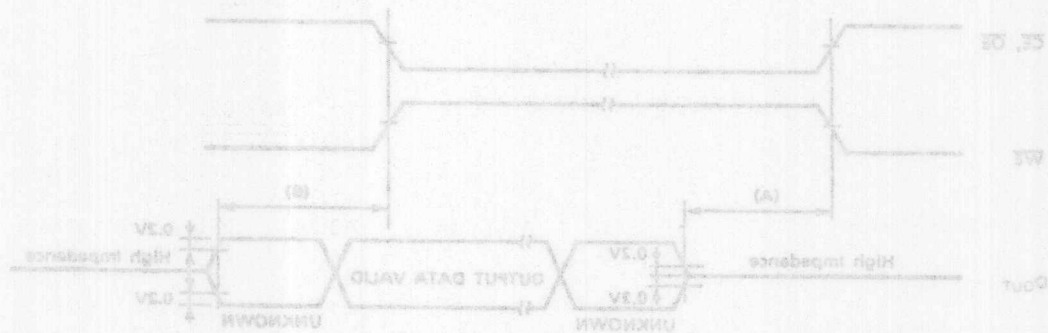
1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{COE} , t_{OEE} , t_{BE} , t_{OEw} Output Enable Time
 - (B) t_{COD} , t_{ODO} , t_{BD} , t_{ODW} Output Disable Time



Notes

Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 - (A) $t_{OE, low \rightarrow low}$ Output Enable Time
 - (B) $t_{OD, low \rightarrow low}$ Output Disable Time



TC551402J-20/25/30

4,194,304 WORD x 1 BIT/1,048,576 WORD x 4 BIT CMOS STATIC RAM

Description

The TC551402J is a 4,194,304 bit high speed CMOS static random access memory that is configurable to an organization of either 4,194,304 words by 1 bit or 1,048,576 words by 4 bits when power is initially applied to the device. The mode (x1/x4) is selected by the input level of pin 17 (B1/B4). The TC551402J operates from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC551402J features low power dissipation when the SRAM is deselected using chip enable (\overline{CE}), and has an output enable input (\overline{OE}) for fast memory access. It is suitable for use in high speed applications such as cache memory, high speed storage, and main memory. All inputs and outputs are TTL compatible.

The TC551402J is available in a 32-pin, 400mil SOJ package suitable for high density assembly.

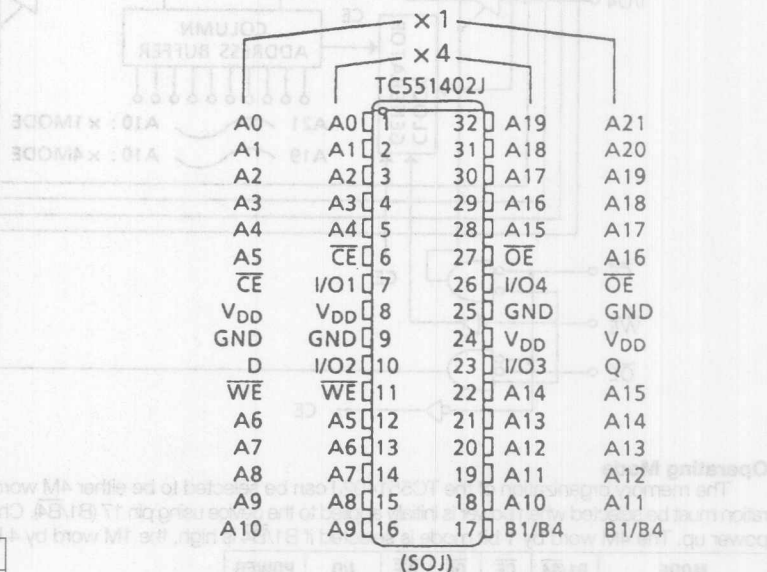
Features

- Fast access time
 - TC551402J-20 20ns (max.)
 - TC551402J-25 25ns (max.)
 - TC551402J-30 30ns (max.)
- Low power dissipation
 - Operation:
 - TC551402J-20 160mA (max.)
 - TC551402J-25 160mA (max.)
 - TC551402J-30 150mA (max.)
 - Standby: 10mA (max.)
- Fully static operation
- Single power supply: 5V \pm 10%
- Output buffer control: \overline{OE}
- Inputs and outputs TTL compatible
- Separate data I/O (x1 mode)
- Common data I/O (x4 mode)
- Package
 - TC551402J: SOJ32-P-400A

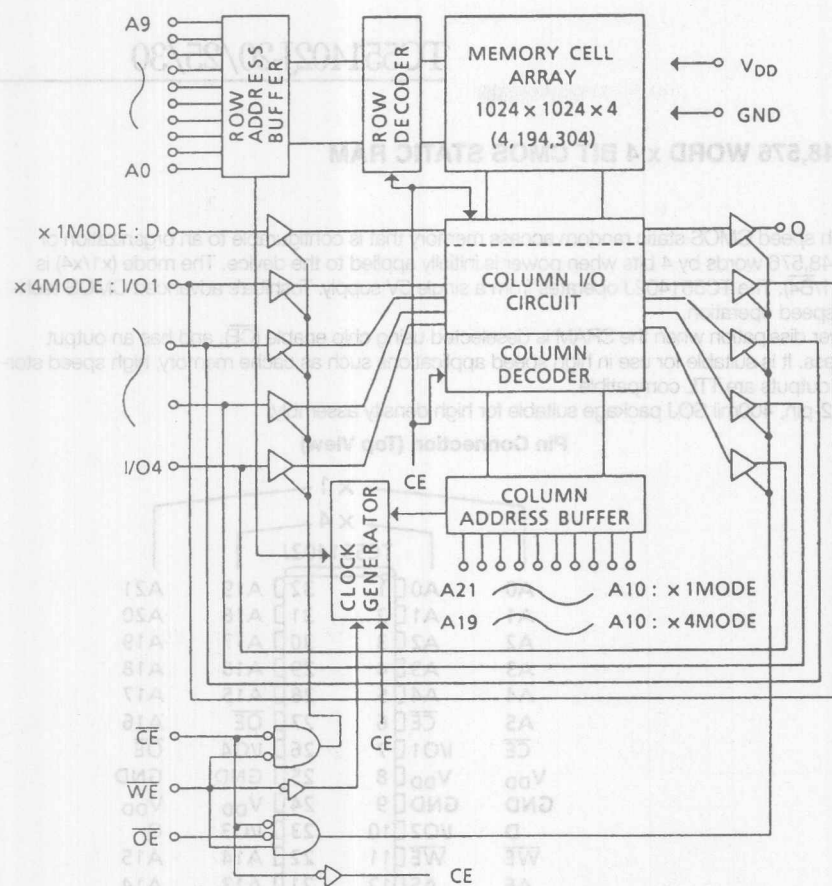
Pin Names

A0 ~ A21	Address Inputs
I/O1 ~ I/O4	Data Inputs/Outputs
D	Data Input
Q	Data Output
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V _{DD}	Power (+5V)
GND	Ground
B1/B4	Bit Select (x1/x4)

Pin Connection (Top View)



Block Diagram



Operating Mode

The memory organization of the TC551402J can be selected to be either 4M words by 1 bit or 1M word by 4 bits. The configuration must be selected when power is initially applied to the device using pin 17 (B1/B4). Changing the state of this pin is prohibited after power up. The 4M word by 1 bit mode is selected if B1/B4 is high, the 1M word by 4 bit mode is selected if B1/B4 is low.

MODE		B1/B4	CE	OE	WE	I/O	POWER
x1 MODE	Read	H	L	L	H	D _{OUT}	I _{DDO}
	Write	H	L	*	L	D _{IN}	I _{DDO}
	Output Disabled	H	L	H	H	High-Z	I _{DDO}
	Standby	H	H	*	*	High-Z	I _{DDS}
x4 MODE	Read	L	L	L	H	D _{OUT}	I _{DDO}
	Write	L	L	*	L	D _{IN}	I _{DDO}
	Output Disabled	L	L	H	H	High-Z	I _{DDO}
	Standby	L	H	*	*	High-Z	I _{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0* ~ 7.0	V
V_{IO}	Input/Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
V_{OUT}	Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

* -3V with pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

* -3V with pulse width of 10ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	8	—	—	mA
I_{DDO}	Operating Current	$t_{cycle} = \text{Min cycle}$, $\overline{CE} = V_{IL}$ $I_{OUT} = 0 \text{ mA}$ Other Inputs = V_{IH}/V_{IL}	-20	—	160	mA
			-25	—	160	
			-30	—	150	
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V_{IH}/V_{IL}	—	—	30	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2V$ Other Inputs = $V_{DD} - 0.2V$ or $0.2V$	—	—	10	mA

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	8	pF
C_{IO}, C_{OUT}	I/O, Output Capacitance	$V_{OUT} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C ⁽¹⁾, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551402J-20		TC551402J-25		TC551402J-30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	20	—	25	—	30	—	ns
t _{ACC}	Address Access Time	—	20	—	25	—	30	
t _{CO}	Chip Enable Access Time	—	20	—	25	—	30	
t _{OE}	Output Enable Access Time	—	10	—	12	—	14	
t _{COE}	Output Enable Time from \overline{CE}	5	—	5	—	5	—	
t _{COD}	Output Disable Time from \overline{CE}	—	10	—	10	—	10	
t _{OEE}	Output Enable Time from \overline{OE}	1	—	1	—	1	—	
t _{ODO}	Output Disable Time From \overline{OE}	—	8	—	10	—	12	
t _{OH}	Output Data Hold Time from Address Change	5	—	5	—	5	—	
t _{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	
t _{PD}	Chip Deselection to Power Down Time	—	20	—	25	—	30	

Write Cycle

SYMBOL	PARAMETER	TC551402J-20		TC551402J-25		TC551402J-30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	20	—	25	—	30	—	ns
t _{WP}	Write Pulse Width	11	—	13	—	15	—	
t _{AW}	Address Valid to End of Write	17	—	20	—	23	—	
t _{CW}	Chip Enable to End of Write	17	—	20	—	23	—	
t _{AS}	Address Setup Time	0	—	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	
t _{DS}	Data Setup Time	10	—	12	—	14	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	
t _{OE_W}	Output Enable Time from \overline{WE}	1	—	1	—	1	—	
t _{OD_W}	Output Disable Time from \overline{WE}	—	8	—	10	—	12	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

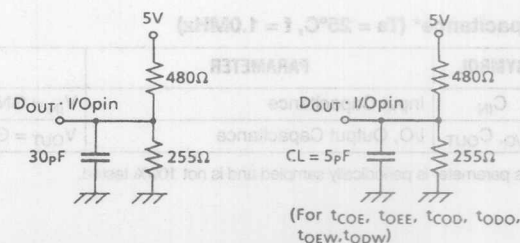
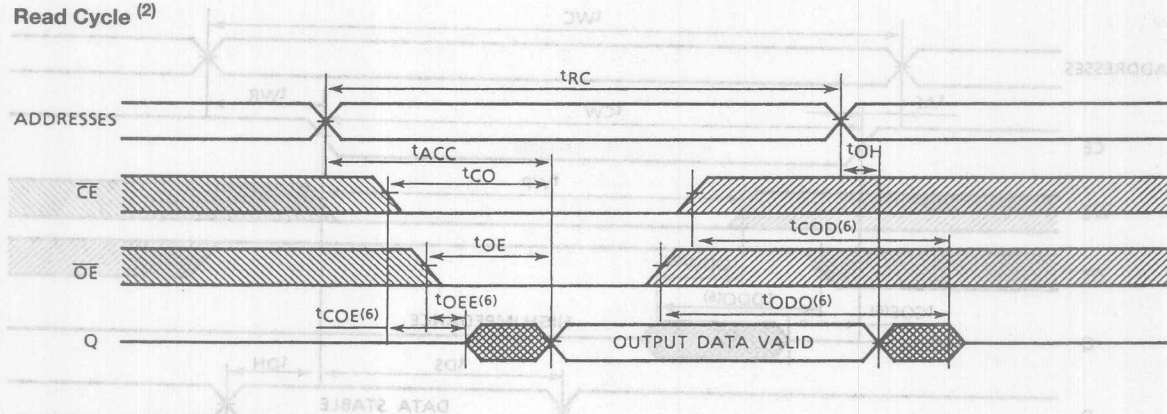
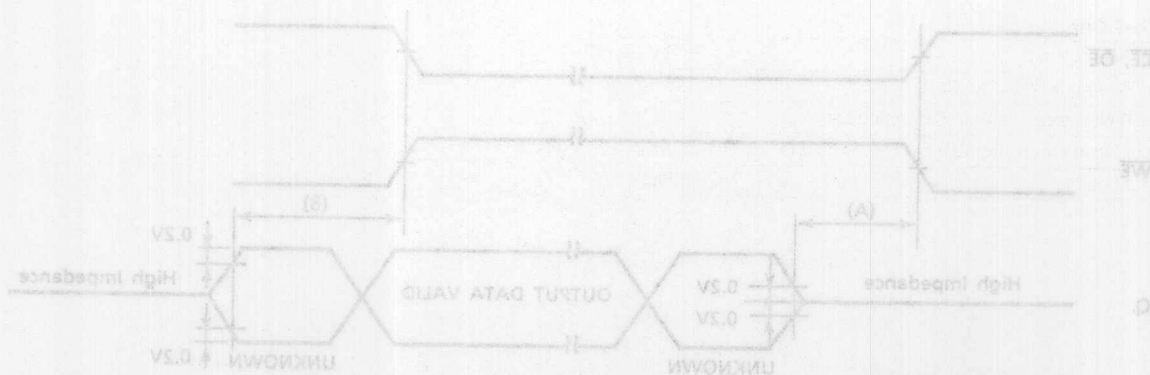
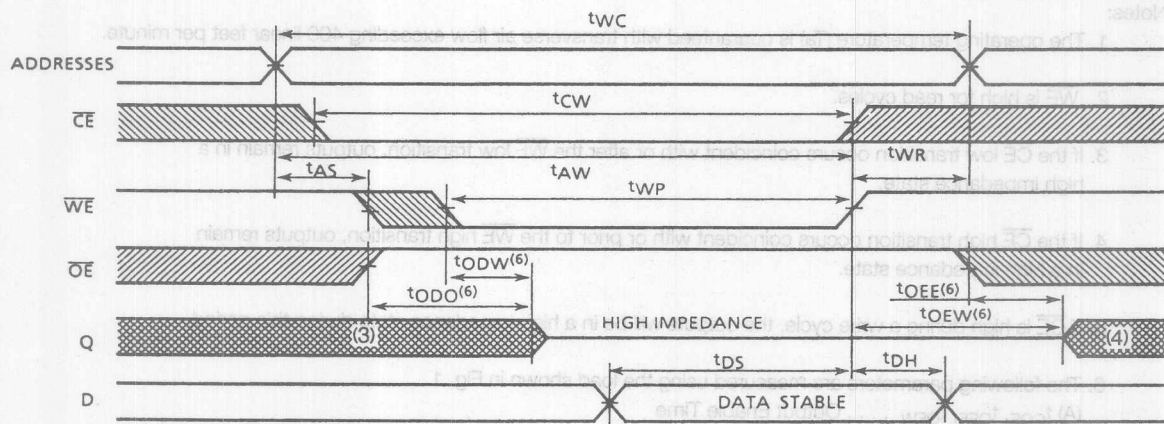
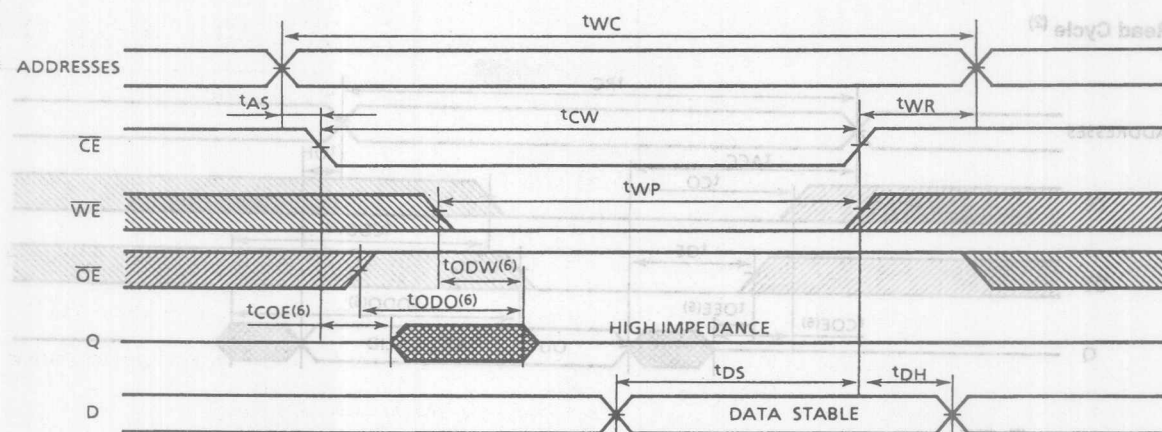


Figure 1.

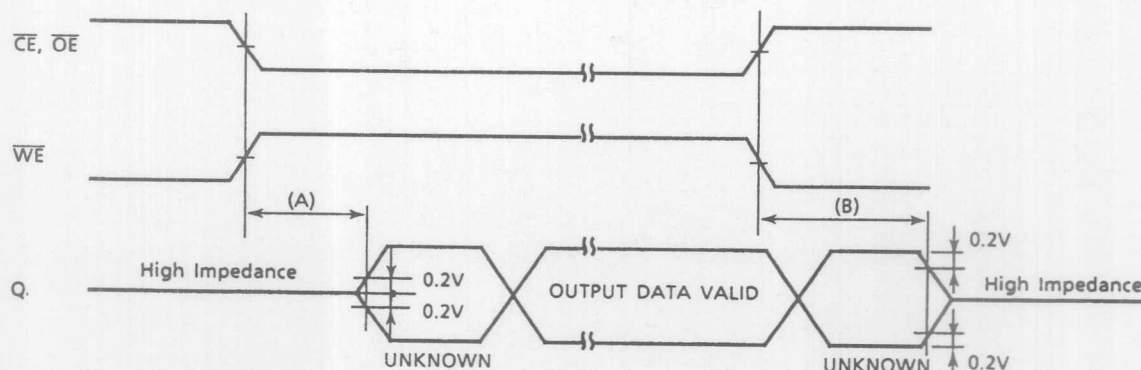
Timing Waveforms

Read Cycle ⁽²⁾Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled Write)

Write Cycle 2⁽⁵⁾ ($\overline{\text{CE}}$ Controlled Write)

Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. $\overline{\text{WE}}$ is high for read cycles.
3. If the $\overline{\text{CE}}$ low transition occurs coincident with or after the $\overline{\text{WE}}$ low transition, outputs remain in a high impedance state.
4. If the $\overline{\text{CE}}$ high transition occurs coincident with or prior to the $\overline{\text{WE}}$ high transition, outputs remain in a high impedance state.
5. If $\overline{\text{OE}}$ is high during a write cycle, the outputs will be in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 (A) t_{COE} , t_{OEE} , t_{OEw} . . . Output Enable Time
 (B) t_{COD} , t_{ODO} , t_{ODW} . . . Output Disable Time



TC554101J-20/25/30

SILICON GATE CMOS

1,048,576 WORD x 4 BIT SEPARATE I/O CMOS STATIC RAM

Description

The TC554101J is a 4,194,304 bit high speed CMOS static random access memory organized as 1,048,576 words by 4 bits and operated from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC554101J features low power dissipation when the device is deselected using chip enable (\overline{CE}), and has an output enable input (\overline{OE}) for fast memory access.

The TC554101J is suitable for use in applications where high speed is required such as cache memory, high speed storage, and main memory. All inputs and outputs are TTL compatible.

The TC554101J is available in a 400mil width, 36-pin SOJ suitable for high density surface assembly.

Features

- Fast access time
 - TC554101J -20 20ns (max.)
 - TC554101J -25 25ns (max.)
 - TC554101J -30 30ns (max.)
- Low power dissipation
 - TC554101J -20 160mA (max.)
 - TC554101J -25 160mA (max.)
 - TC554101J -30 150mA (max.)
 - Standby: 10mA (max.)
- Single 5V power supply: $5V \pm 10\%$
- Fully static operation
- Inputs and outputs TTL compatible
- Separate inputs and outputs
- Output buffer control: \overline{OE}
- Package:
 - TC554101J: SOJ36-P-400

Pin Names

A0 ~ A19	Address Inputs
D1 ~ D4	Data Inputs
Q1 ~ Q4	Data Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
TF*	Test Function

* The TF pin is low for normal operation.

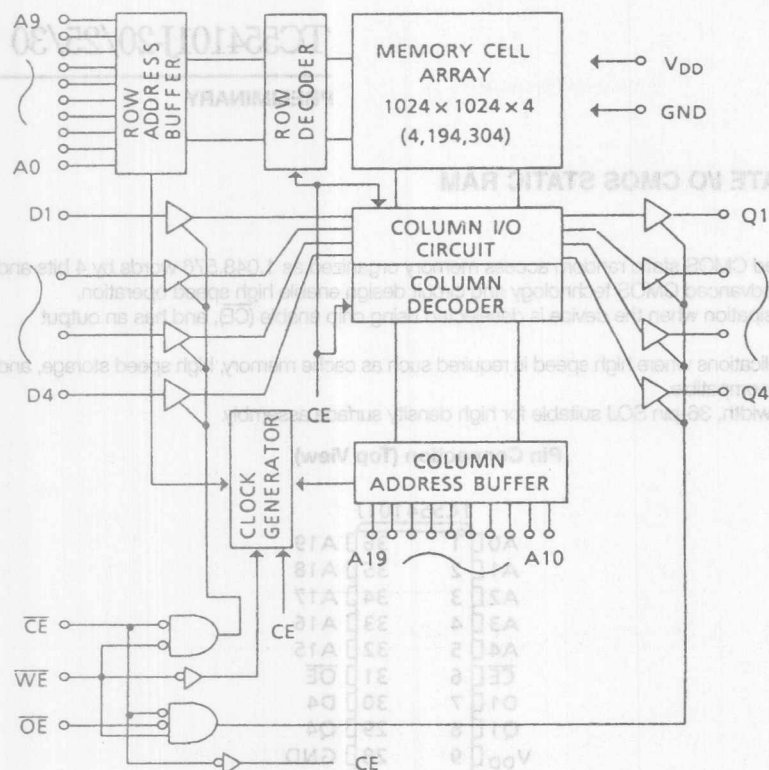
Pin Connection (Top View)

TC554101J			
A0	1	36	A19
A1	2	35	A18
A2	3	34	A17
A3	4	33	A16
A4	5	32	A15
\overline{CE}	6	31	\overline{OE}
D1	7	30	D4
Q1	8	29	Q4
V_{DD}	9	28	GND
GND	10	27	V_{DD}
Q2	11	26	Q3
D2	12	25	D3
\overline{WE}	13	24	TF
A5	14	23	A14
A6	15	22	A13
A7	16	21	A12
A8	17	20	A11
A9	18	19	A10

(SOJ)

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	0.5 - 7.0	V
V_{in}	Input Voltage	0.5 - 7.0	V
V_{out}	Output Voltage	0.5 - $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{oper}	Operating Temperature	-55 - 125	°C
T_{stor}	Storage Temperature	-65 - 150	°C
T_{shut}	Shutdown Temperature	-10 - 55	°C

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	\overline{WE}	I/O	POWER
Read		L	L	H	D_{OUT}	I_{DDO}
Write		L	*	L	D_{IN}	I_{DDO}
Output Disable		L	H	H	High-Z	I_{DDO}
Standby		H	*	*	High-Z	I_{DDs}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0* ~ 7.0	V
V_{OUT}	Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

*-3V with a pulse width of 10ns

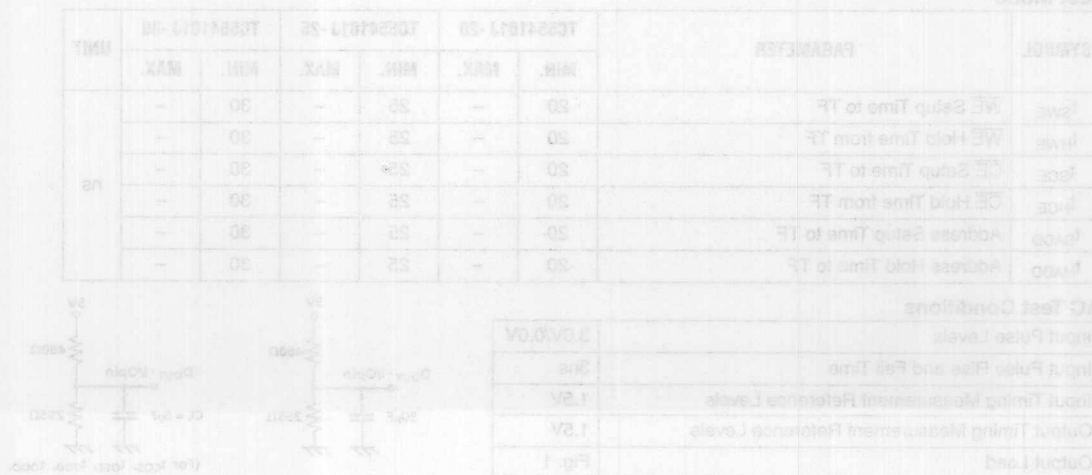
DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	8	—	—	mA
I_{DDO}	Operating Current	$t_{\text{cycle}} = \text{Min cycle,}$ $\overline{CE} = V_{IL}$, $I_{OUT} = 0\text{mA}$, Other Inputs = V_{IH}/V_{IL}	-20	—	160	μA
			-25	—	160	mA
			-30	—	150	
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V_{IH}/V_{IL}	—	—	30	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2V$ Other Inputs = $V_{DD} - 0.2V$ or $0.2V$	—	—	10	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.



AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC554101J-20		TC554101J-25		TC554101J-30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	20	—	25	—	30	—	ns
t_{ACC}	Address Access Time	—	20	—	25	—	30	
t_{CO}	Chip Enable Access Time	—	20	—	25	—	30	
t_{OE}	Output Enable Access Time	—	10	—	12	—	14	
t_{COE}	Output Enable Time from \overline{CE}	5	—	5	—	5	—	
t_{COD}	Output Disable Time from \overline{CE}	—	10	—	10	—	10	
t_{OEE}	Output Enable Time from \overline{OE}	1	—	1	—	1	—	
t_{ODO}	Output Disable Time from \overline{OE}	—	8	—	10	—	10	
t_{OH}	Output Data Hold Time from Address Change	5	—	5	—	5	—	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	20	—	25	—	30	

Write Cycle

SYMBOL	PARAMETER	TC554101J-20		TC554101J-25		TC554101J-30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	20	—	25	—	30	—	ns
t_{WP}	Write Pulse Width	11	—	13	—	15	—	
t_{AW}	Address Valid to End of Write	17	—	20	—	23	—	
t_{CW}	Chip Enable to End of Write	17	—	20	—	23	—	
t_{AS}	Address Setup Time	0	—	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{OEw}	Output Enable Time from \overline{WE}	1	—	1	—	1	—	
t_{ODw}	Output Disable Time from \overline{WE}	—	8	—	10	—	12	
t_{DS}	Data Setup Time	10	—	12	—	14	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	

Test Mode

SYMBOL	PARAMETER	TC554101J-20		TC554101J-25		TC554101J-30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{SWE}	\overline{WE} Setup Time to TF	20	—	25	—	30	—	ns
t_{HWE}	\overline{WE} Hold Time from TF	20	—	25	—	30	—	
t_{SCE}	\overline{CE} Setup Time to TF	20	—	25	—	30	—	
t_{HCE}	\overline{CE} Hold Time from TF	20	—	25	—	30	—	
t_{SADD}	Address Setup Time to TF	20	—	25	—	30	—	
t_{HADD}	Address Hold Time to TF	20	—	25	—	30	—	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

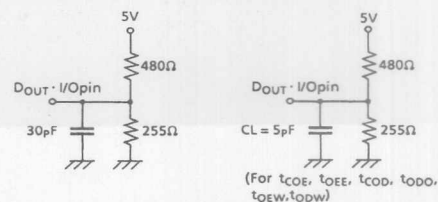
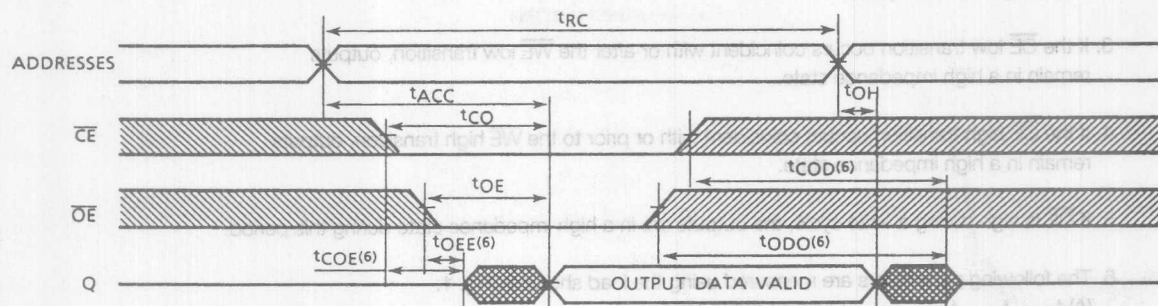
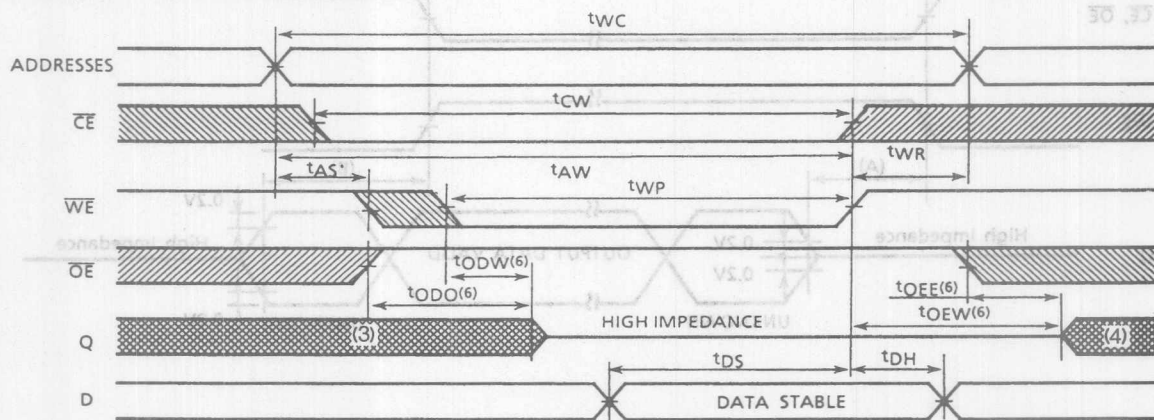
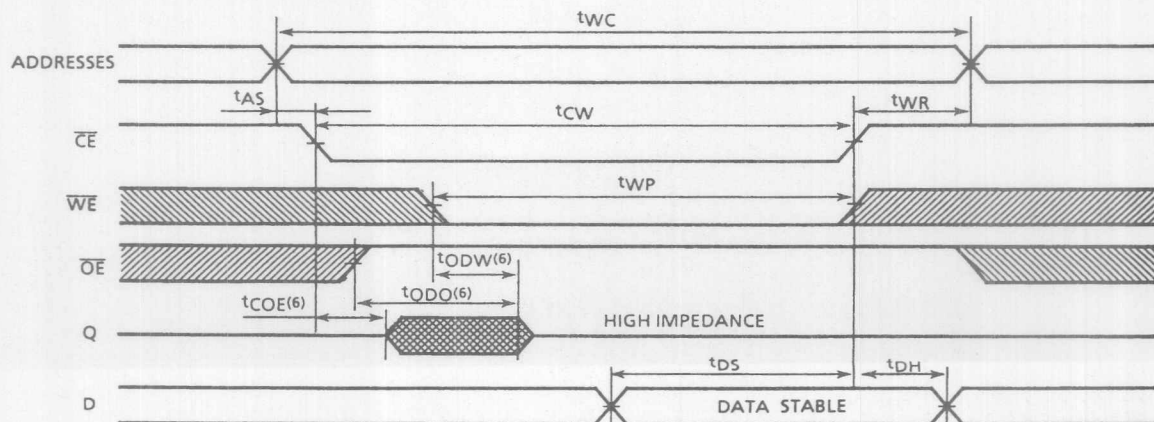


Figure 1.

Timing Waveforms

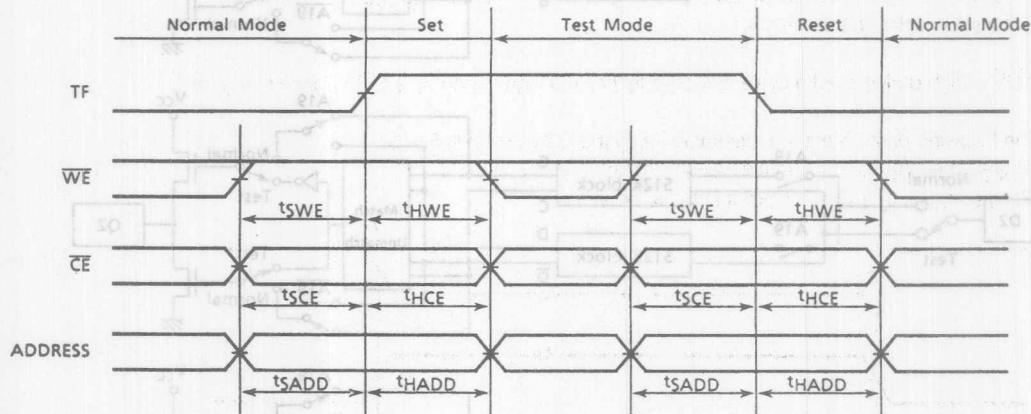
Read Cycle ⁽²⁾Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled Write)Write Cycle 2 ⁽⁵⁾ (\overline{CE} Controlled Write)

-

Test Mode

Although the TC554101J appears to be organized as 1,048,576 words by 4 bits, it is internally organized as 524,288 words by 8 bits.

In the "Test Mode", data is written into the 8-512K blocks in parallel and then retrieved. Address line A19 is not used. Upon reading, if the two bits associated with the I/O pin are equal (all "1"s or "0"s), the output pin indicates a "1". If they are not equal, the output pin would indicate a "0". Fig. 3 show the block diagram of the TC554101J. The "Test Mode" enables the 1M word memory to be tested as if it were only a 512K word memory. The "Test Mode" function can be performed in any timing cycle when the "TF" pin is held at V_{IH} (see Figure 2). Normal functioning requires that the "TF" pin be connected to V_{IL} .



$\overline{OE} = V_{IH} \text{ or } V_{IL}$

Figure 2. Test Mode Cycle

Block Diagram in Test Mode

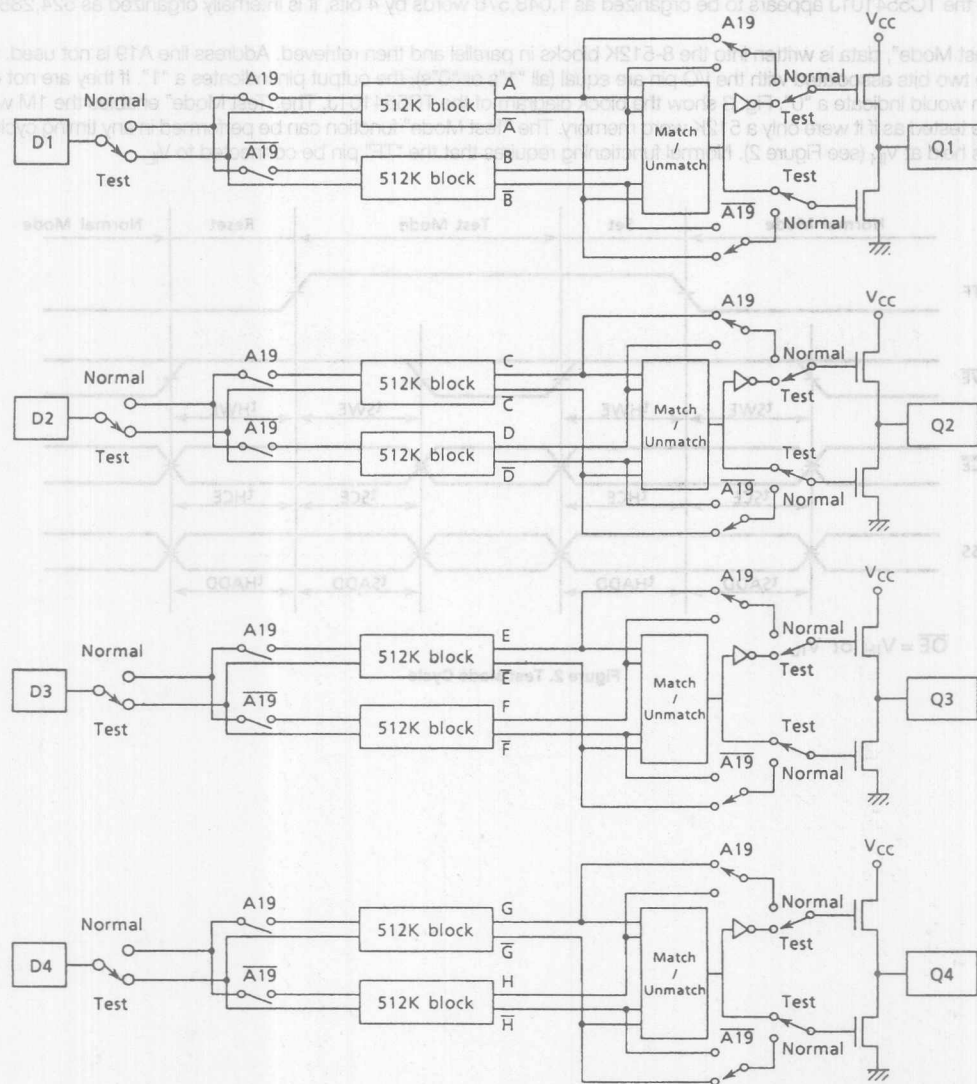


Figure 3. Block Diagram in Test Mode

Density	Organization	Package	Speed (ns)	Features	Page
TC58B8128	1M	128K x 8	10, 12	Synchronous 100MHz...C-13	
TC58B8125	1M	128K x 8	10, 12	Synchronous 100MHz...C-7	
TC58B8455B	1M	256K x 4	10, 12	Synchronous 100MHz...C-1	

Package J = SOJ

High Speed Synchronous SRAM

High Speed Synchronous Static RAM

	Density	Organization	Package	Speed (ns)	Features	Page
TC55BS4258.....	1M	256K x 4	J	10, 12	Synchronous 100MHz...	C-1
TC55BS8125.....	1M	128K x 8	J	10, 12	Synchronous 100MHz...	C-7
TC55BS8128.....	1M	128K x 8	J	10, 12	Synchronous 100MHz...	C-13

Package: J = SOJ

TC55BS4258J-10/12

PRELIMINARY

262,144 WORD x 4 BIT SYNCHRONOUS STATIC RAM

with Input Registers, Output Registers and Pass-Through Feature

Description

The TC55BS4258J is a 1,048,576 bit synchronous static random access memory fabricated using BiCMOS technology and organized as 262,144 words by 4 bits. The TC55BS4258J has separate data inputs and outputs and a write-cycle pass-through feature.

Designed for pipelined architectures, this device has internal input and output registers which latch on the positive edge of an external clock (CLK). All address, data, and control signals are latched. The setup and hold times for the inputs are 2ns and 1ns respectively. Synchronous SRAMs can lead to faster, more robust system operation by virtually eliminating the timing skew problems associated with conventional asynchronous SRAMs. For example, write operations are internally self-timed when initiated - eliminating the need for accurate write pulse generation and timing by the memory controller or microprocessor. A pass-through feature during write cycles allows the outputs to follow the inputs with a one clock cycle delay. For read cycles, data is available one clock cycle after the address is latched. All inputs and outputs are TTL compatible.

The TC55BS4258J is available in a 36-pin, 400mil SOJ package suitable for high density assembly.

Features

- Fast cycle time
 - TC55BS4258J-10 10ns (max.)
 - TC55BS4258J-12 12ns (max.)
- Fast clock access time
 - TC55BS4258J-10 5ns (max.)
 - TC55BS4258J-12 6ns (max.)
- Input and output registers for synchronous operation
- Data pass-through for write cycles
- Single power supply: 5V \pm 10%
- Separate data inputs and outputs
- Package: JEDEC standard pinout
 - 36-pin, 400mil SOJ: SOJ36-P-400

Pin Names

A0 ~ A17	Address Inputs
D0 ~ D3	Data Inputs
Q0 ~ Q3	Data Outputs
CLK	Clock Input
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V _{DD}	Power (+5V)
GND	Ground
NC	No Connection

Pin Connection (Top View)

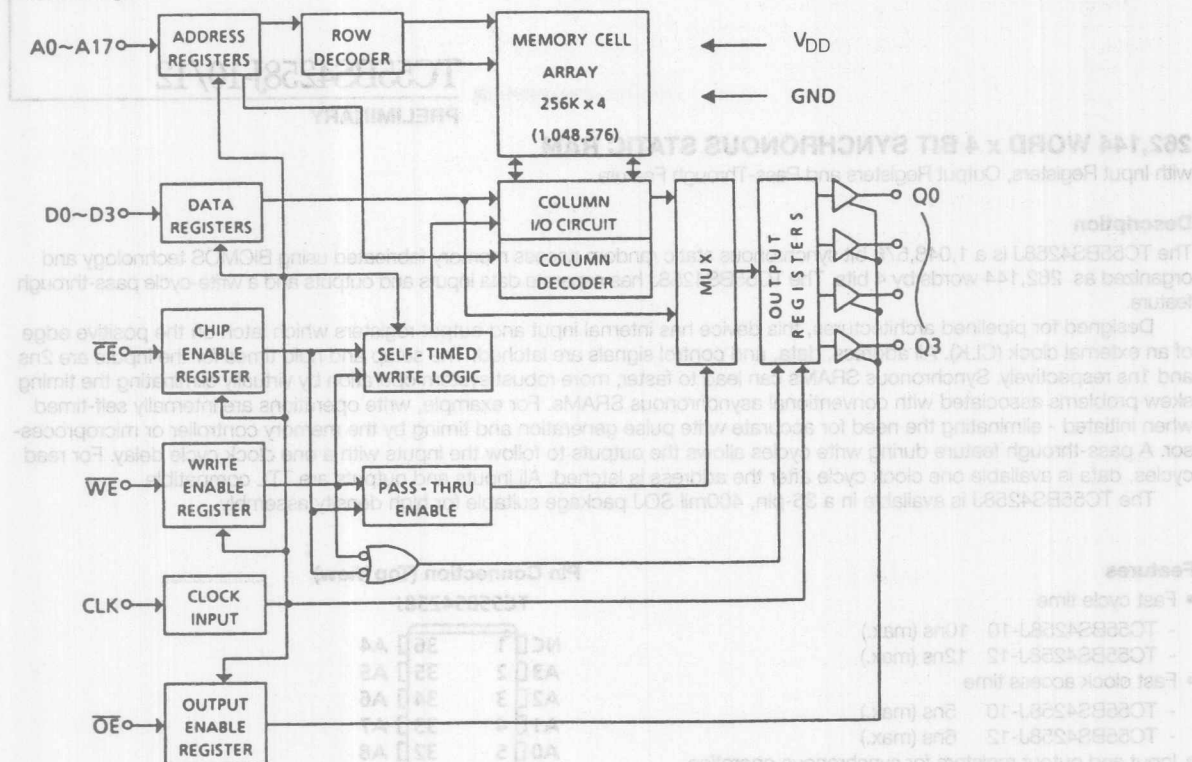
TC55BS4258J

NC	1	36	A4
A3	2	35	A5
A2	3	34	A6
A1	4	33	A7
A0	5	32	A8
\overline{CE}	6	31	\overline{OE}
D0	7	30	D3
Q0	8	29	Q3
V _{DD}	9	28	GND
GND	10	27	V _{DD}
Q1	11	26	Q2
D1	12	25	D2
\overline{WE}	13	24	CLK
A17	14	23	A9
A16	15	22	A10
A15	16	21	A11
A14	17	20	A12
NC	18	19	A13

(SOJ)

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V _{IN}	Input Voltage	-0.5 ~ 7.0	V
V _{OUT}	Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1300	mW
T _{STG}	Storage Temperature	-55 ~ 125	°C
T _{OP}	Operating Temperature	-40 ~ 85	°C

Block Diagram



Operating Mode

MODE	WE	CE	OE (next Cycle)	D	Q (next Cycle)
Write, Pass-Through	L	L	L	Valid	D _{OUT}
Write	L	L	H	Valid	High - Z
Pass-Through	L	H	L	Valid	D _{OUT}
Standby	L	H	H	*	High - Z
Read	H	L	L	*	D _{OUT}
Output Disable	H	L	H	*	High - Z
Standby	H	H	*	*	High - Z

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V _{IN}	Input Voltage	-2.0 ~ 7.0	V
V _{OUT}	Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1300	mW
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-65~150	°C
T _{OPR}	Operating Temperature	-10~85	°C

Pin Number	Pin Name
10	Address Inputs
11	Data Inputs
12	Data Outputs
13	Output Enable
14	Write Enable Input
15	Chip Enable Input
16	Output Enable Input
17	Power (VDD)
18	Ground
19	No Connection

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5	—	0.8	V

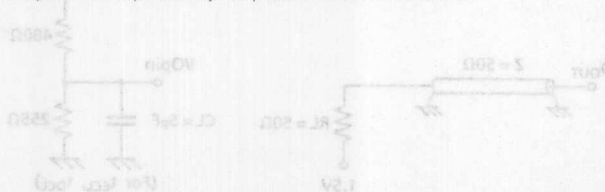
DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	8	—	—	mA
I_{DDO}	Operating Current	$t_{\text{cycle}} = \text{Min cycle}$, $\overline{CE} = V_{IL}$ $I_{OUT} = 0 \text{ mA}$	-10	—	200	mA
		Other Inputs = V_{IH}/V_{IL}	-12	—	190	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
C_{CLK}	Clock Input Capacitance	$V_{CLK} = \text{GND}$	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	8	pF

* This parameter is periodically sampled and is not 100% tested.



AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$ ⁽¹⁾, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TC55BS4258J-10		TC55BS4258J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{CY}	Cycle Time	10	—	12	—	
t_{CHH}	Clock Pulse High Width	3	—	3	—	
t_{CLL}	Clock Pulse Low Width	3	—	3	—	
t_{AS}	Address Setup Time	2	—	2	—	
t_{DS}	Data Input Setup Time	2	—	2	—	
t_{ES}	Chip Enable Input Setup Time	2	—	2	—	
t_{WS}	Write Enable Input Setup Time	2	—	2	—	
t_{GS}	Output Enable Input Setup Time	2	—	2	—	
t_{AH}	Address Hold Time	1	—	1	—	
t_{DH}	Data Input Hold Time	1	—	1	—	
t_{EH}	Chip Enable Input Hold Time	1	—	1	—	
t_{WH}	Write Enable Input Hold Time	1	—	1	—	
t_{GH}	Output Enable Input Hold Time	1	—	1	—	
t_{ACK}	Clock Access Time	1	5	1	6	
$t_{ECL(2)}$	Output Enable Time from Clock	1	5	1	6	
$t_{DCL(2)}$	Output Disable Time from Clock	1	5	1	6	

(1) : The operating temperature (T_a) is guaranteed with transverse air flow exceeding 500 linear feet per minute.(2) : Transition is measured $\pm 200\text{mV}$ from steady voltage with the loading in Fig. 1.

AC Test Conditions

Input Pulse Levels	3.0/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

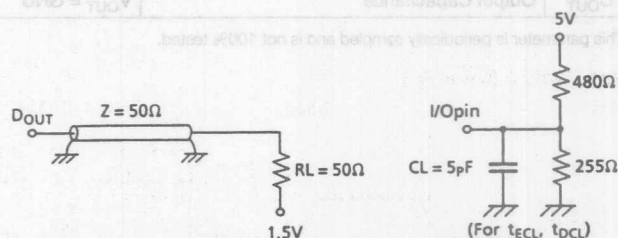
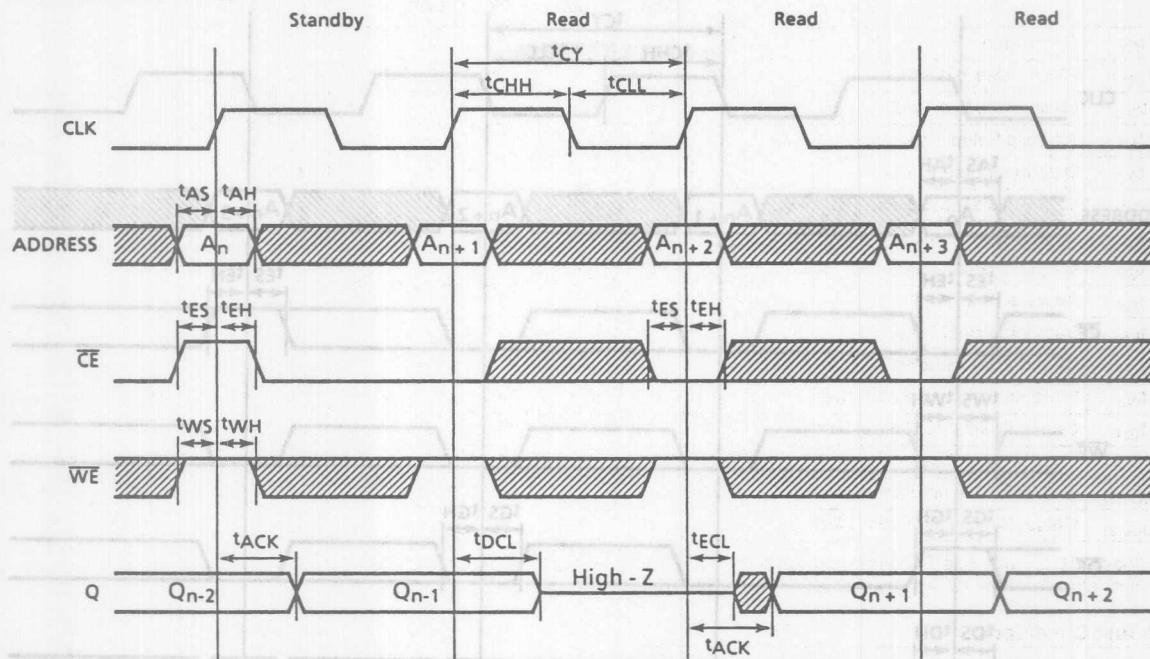
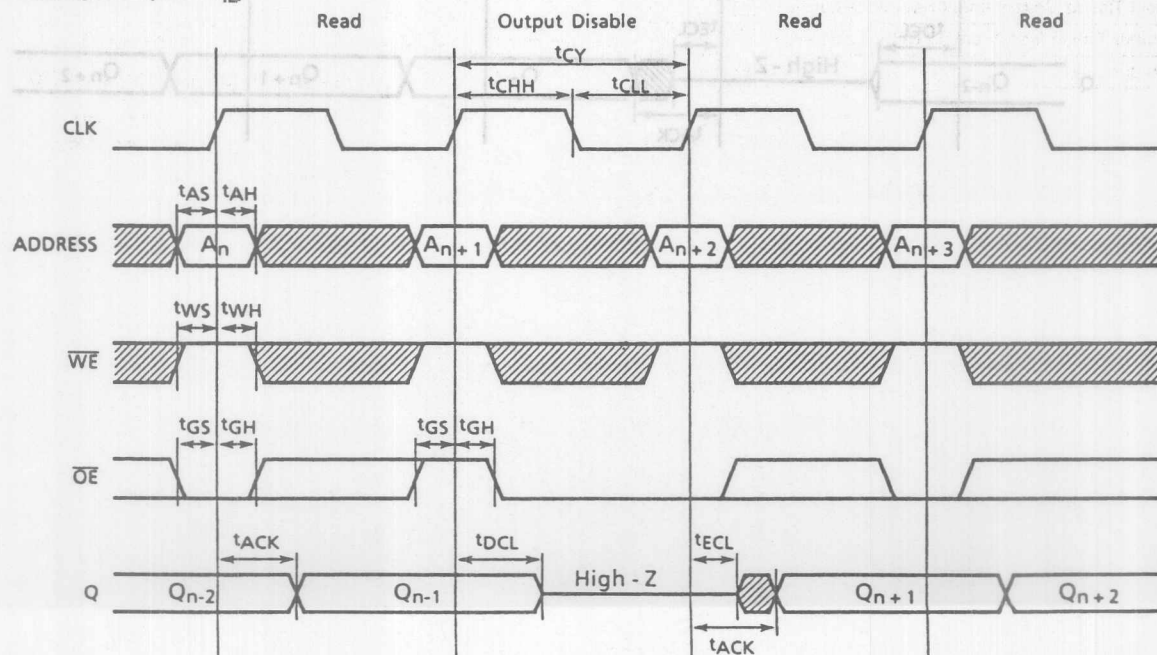
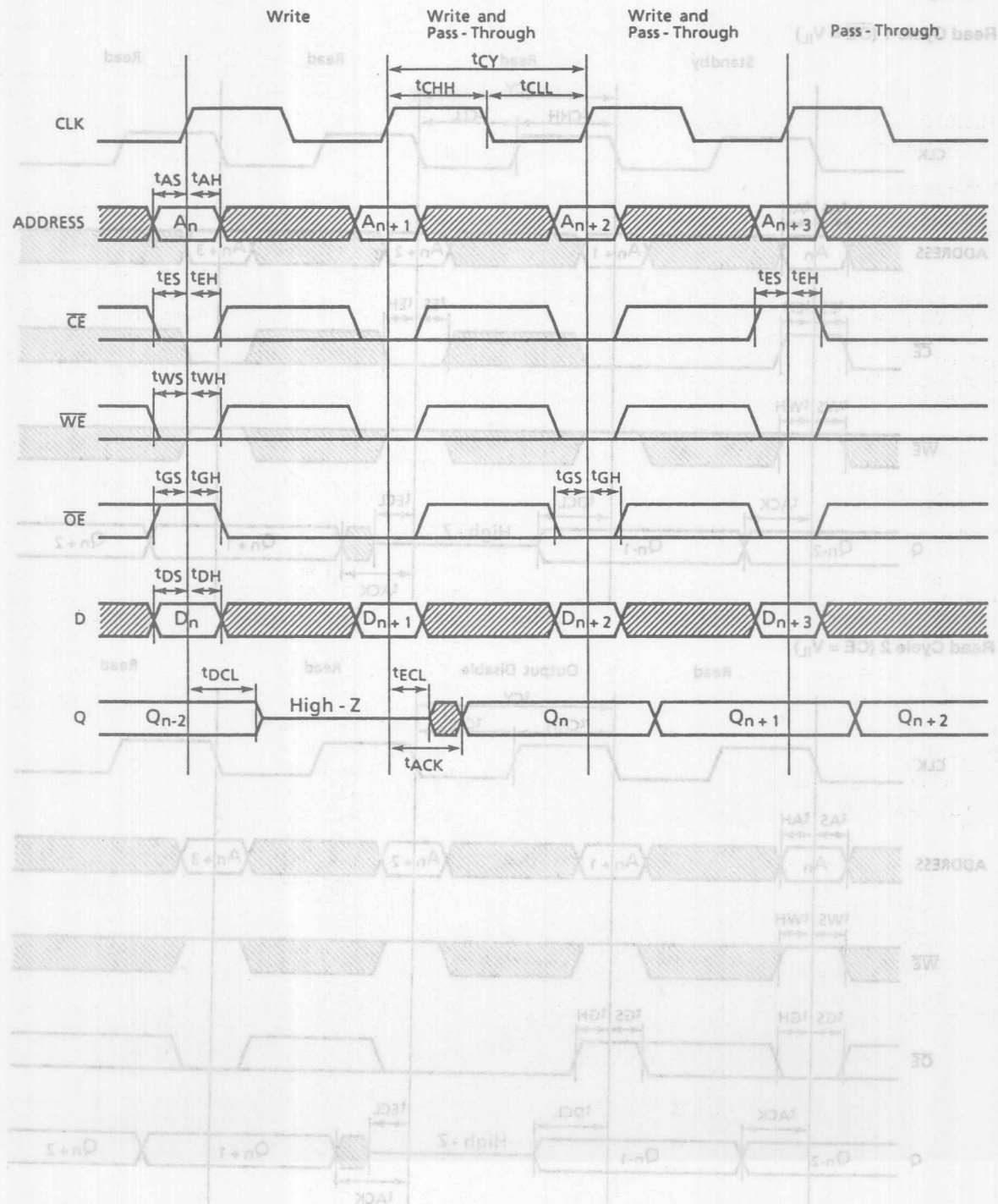


Figure 1.

Timing Waveforms

Read Cycle 1 ($\overline{OE} = V_{IL}$)Read Cycle 2 ($\overline{CE} = V_{IL}$)

Write and Pass-Through Mode



TC55BS8125J-10/12

PRELIMINARY

131,072 WORD x 8 BIT SYNCHRONOUS STATIC RAM

with Input Registers and Output Registers

Description

The TC55BS8125J is a 1,048,576 bit synchronous static random access memory fabricated using BiCMOS technology and organized as 131,072 words by 8 bits. The TC55BS8125J is similar to the TC55BS8128J but has common data I/O lines and does not have the write-cycle pass-through feature.

Designed for pipelined architectures, this device has internal input and output registers which latch on the positive edge of an external clock (CLK). All address, data, and control signals are latched. The setup and hold times for the inputs are 2ns and 1ns respectively. Synchronous SRAMs can lead to faster, more robust system operation by virtually eliminating the timing skew problems associated with conventional asynchronous SRAMs. For example, write operations are internally self-timed when initiated - eliminating the need for accurate write pulse generation and timing by the memory controller or microprocessor. For read cycles, data is available one clock cycle after the address is latched. All inputs and outputs are TTL compatible.

The TC55BS8125J is available in a 36-pin, 400mil SOJ package suitable for high density assembly.

Features

- Fast cycle time
 - TC55BS8125J-10 10ns (max.)
 - TC55BS8125J-12 12ns (max.)
- Fast clock access time
 - TC55BS8125J-10 5ns (max.)
 - TC55BS8125J-12 6ns (max.)
- Input and output registers for synchronous operation
- Single power supply: 5V±10%
- Common data I/O
- Package: JEDEC standard pinout
 - 36-pin, 400mil SOJ: SOJ36-P-400

Pin Names

A0 ~ A16	Address Inputs
I/O1 ~ I/O8	Data Input and Output
CLK	Clock Input
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V _{DD}	Power (+5V)
GND	Ground
NC	No Connection

Pin Connection (Top View)

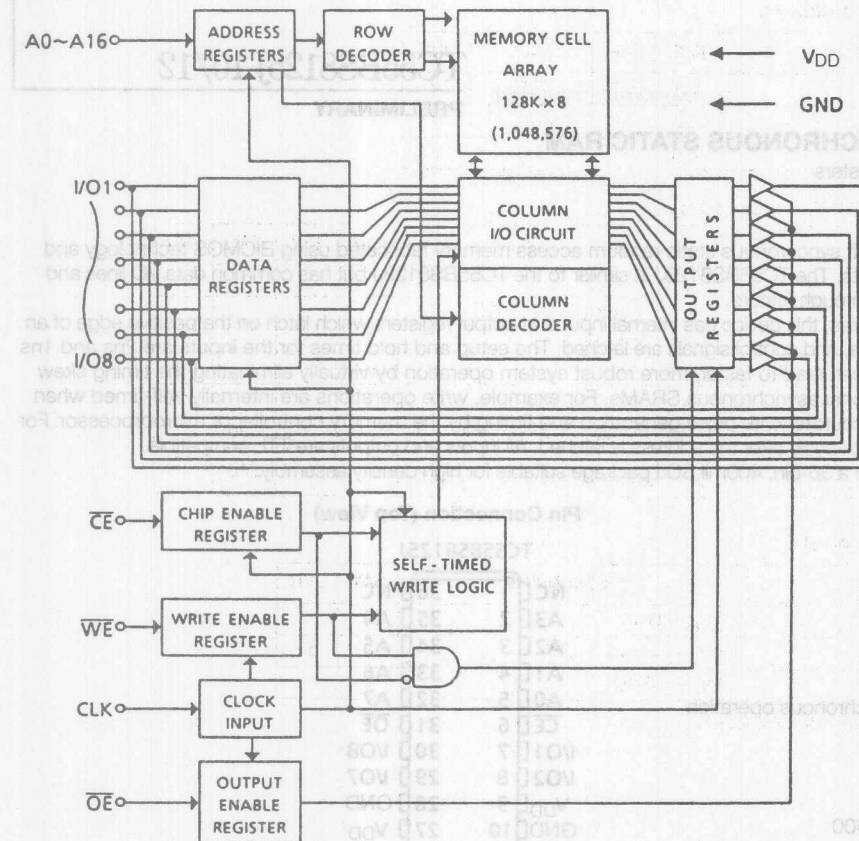
TC55BS8125J

NC	1	36	NC
A3	2	35	A4
A2	3	34	A5
A1	4	33	A6
A0	5	32	A7
\overline{CE}	6	31	\overline{OE}
I/O1	7	30	I/O8
I/O2	8	29	I/O7
V _{DD}	9	28	GND
GND	10	27	V _{DD}
I/O3	11	26	I/O6
I/O4	12	25	I/O5
\overline{WE}	13	24	CLK
A16	14	23	A8
A15	15	22	A9
A14	16	21	A10
A13	17	20	A11
NC	18	19	A12

(SOJ)

SYMBOL	ITEM	UNIT
V _{DD}	Power Supply Voltage	V
V _{IN}	Input Voltage	V
V _{IO}	Input/Output Voltage	V
P _D	Power Dissipation	mW
T _{OP}	Operating Temperature	°C
T _{STG}	Storage Temperature	°C
T _{SEC}	Sealing Temperature	°C

Block Diagram



Operating Mode

MODE	CE	WE	OE (next Cycle)	D	Q (next Cycle)
Write	L	L	*	D _{IN}	High - Z
Read	L	H	L	—	D _{OUT}
Output Disable	L	H	H	—	High - Z
Standby	H	*	*	—	High - Z

* H or L, —Not applicable

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V _{IN}	Input Voltage	-2.0 ~ 7.0	V
V _{I/O}	Input/Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1500	mW
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-65 ~ 150	°C
T _{OPR}	Operating Temperature	-10 ~ 85	°C

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	–	V _{DD} + 0.5	V
V _{IL}	Input Low Voltage	-0.5	–	0.8	V

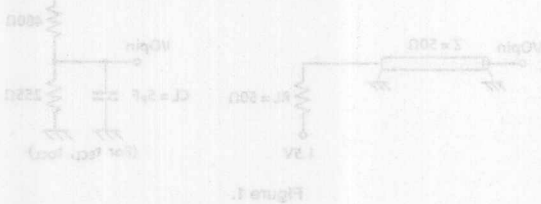
DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}	–	–	±10	μA
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, V _{OUT} = 0 ~ V _{DD}	–	–	±10	μA
I _{OH}	Output High Current	V _{OH} = 2.4V	-4	–	–	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V	8	–	–	mA
I _{DDO}	Operating Current	t _{cycle} = Min cycle, $\overline{CE} = V_{IL}$ I _{OUT} = 0 mA	-10	–	–	mA
		Other Inputs = V _{IH} /V _{IL}	-12	–	–	

Capacitance* (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	6	pF
C _{CLK}	Clock Input Capacitance	V _{CLK} = GND	8	pF
C _{I/O}	I/O Capacitance	V _{I/O} = GND	8	pF

* This parameter is periodically sampled and is not 100% tested.



AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$ ⁽¹⁾, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TC55BS8125J-10		TC55BS8125J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{CY}	Cycle Time	10	—	12	—	
t_{CHH}	Clock Pulse High Width	3	—	3	—	
t_{CLL}	Clock Pulse Low Width	3	—	3	—	
t_{AS}	Address Setup Time	2	—	2	—	
t_{DS}	Data Input Setup Time	2	—	2	—	
t_{ES}	Chip Enable Input Setup Time	2	—	2	—	
t_{WS}	Write Enable Input Setup Time	2	—	2	—	
t_{GS}	Output Enable Input Setup Time	2	—	2	—	
t_{AH}	Address Hold Time	1	—	1	—	ns
t_{DH}	Data Input Hold Time	1	—	1	—	
t_{EH}	Chip Enable Input Hold Time	1	—	1	—	
t_{WH}	Write Enable Input Hold Time	1	—	1	—	
t_{GH}	Output Enable Input Hold Time	1	—	1	—	
t_{ACK}	Clock Access Time	1	5	1	6	
$t_{ECL(2)}$	Output EnableTime from Clock	1	5	1	6	
$t_{DCL(2)}$	Output DisableTime from Clock	1	5	1	6	

(1) : The operating temperature (T_a) is guaranteed with transverse air flow exceeding 500 linear feet per minute.

(2) : Transition is measured $\pm 200\text{mV}$ from steady voltage with the loading in Fig. 1.

AC Test Conditions

Input Pulse Levels	3.0/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig.1

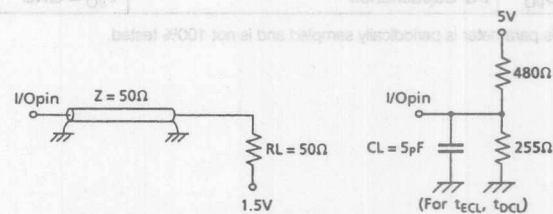
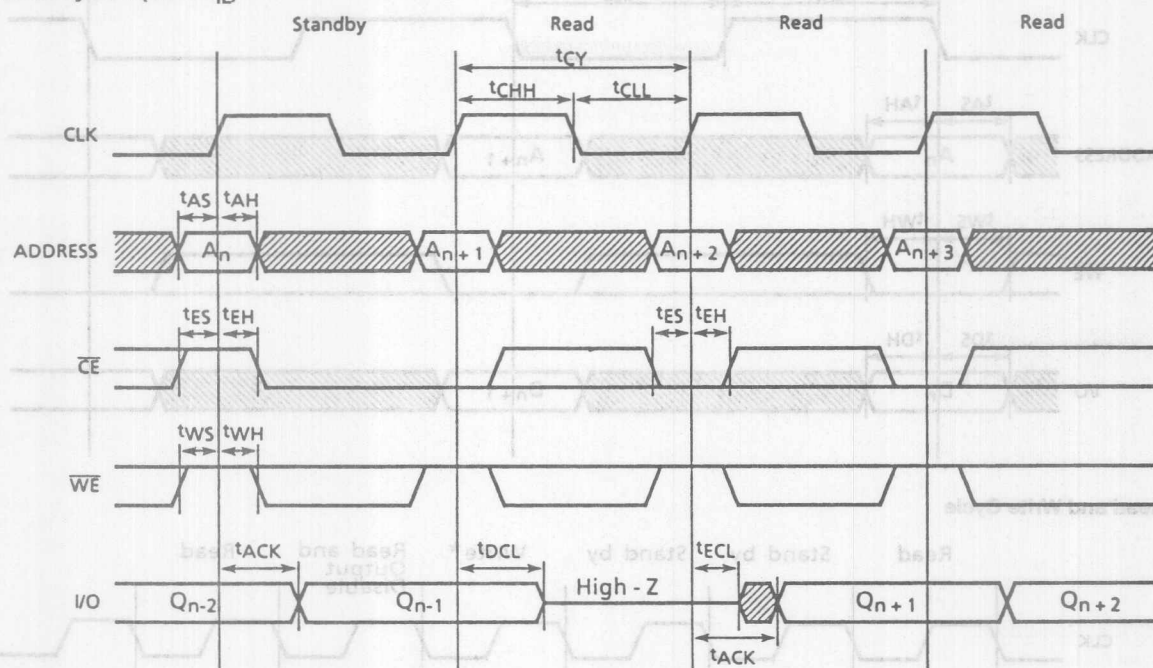
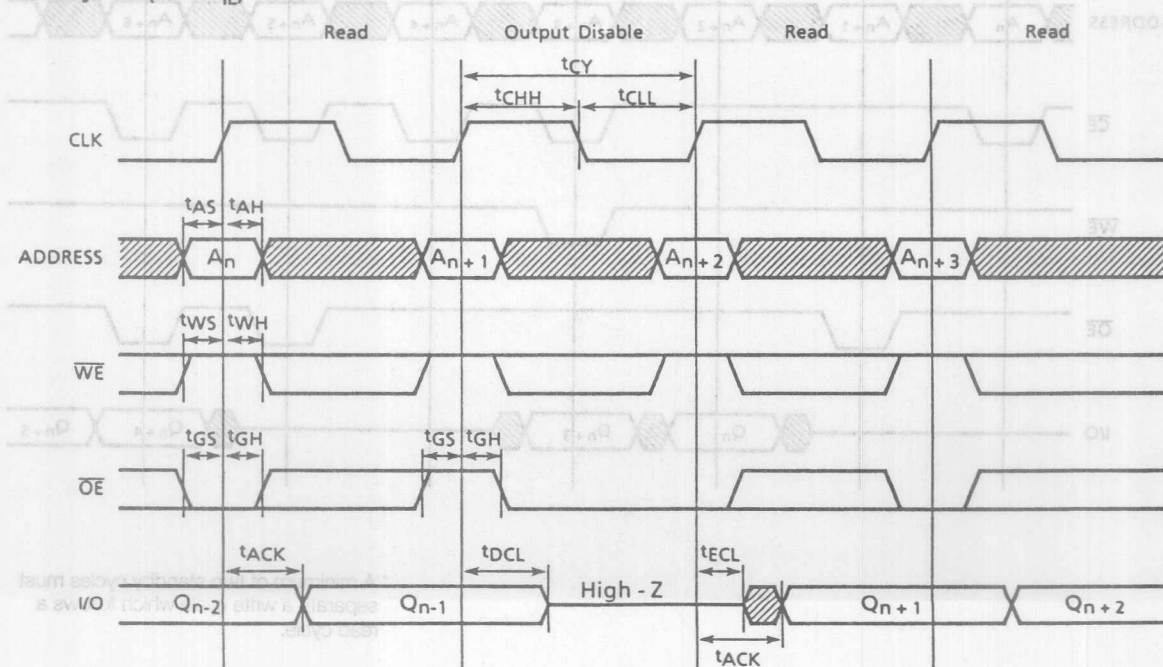
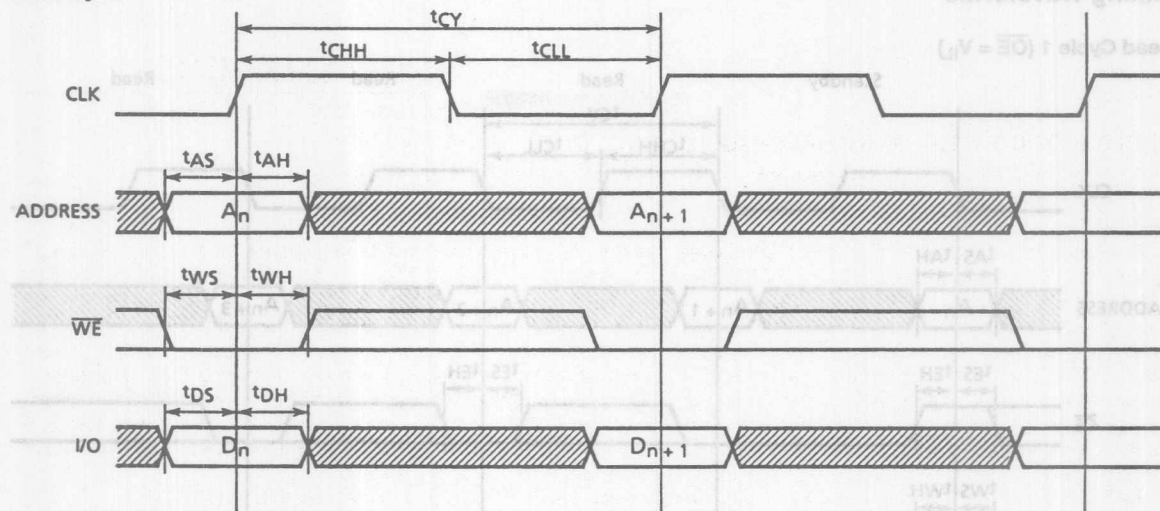


Figure 1.

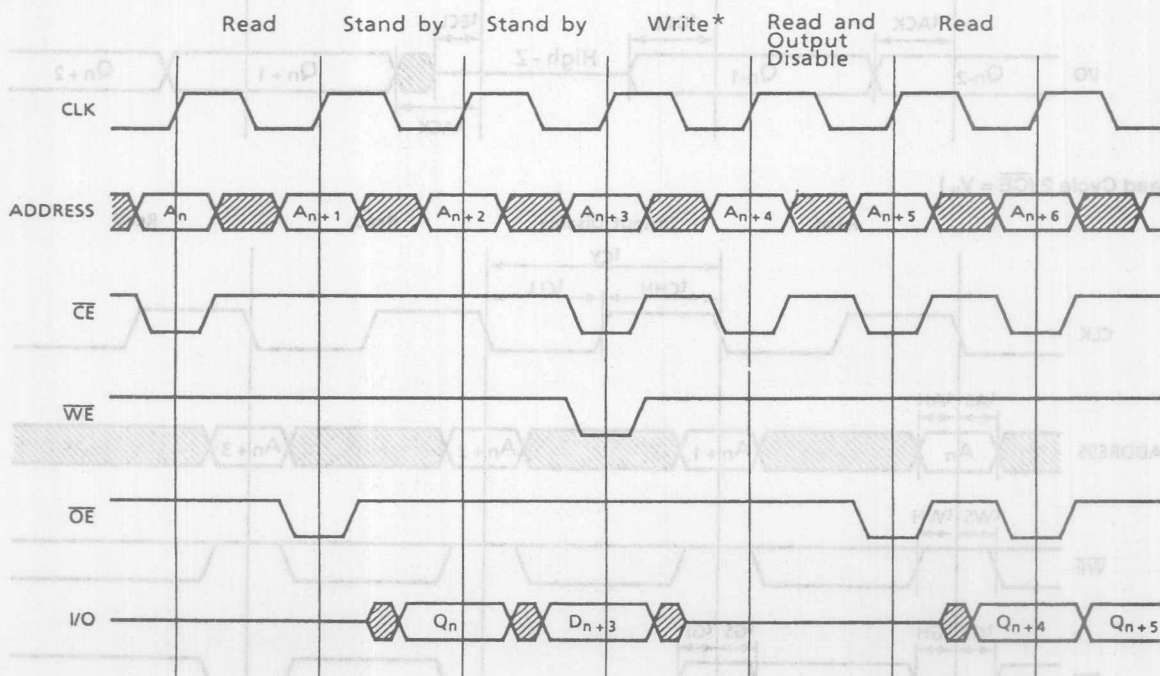
Timing Waveforms

Read Cycle 1 ($\overline{OE} = V_{IL}$)Read Cycle 2 ($\overline{CE} = V_{IL}$)

Write Cycle



Read and Write Cycle



* A minimum of two standby cycles must separate a write cycle which follows a read cycle.

TC55BS8128J-10/12

PRELIMINARY

131,072 WORD x 8 BIT SYNCHRONOUS STATIC RAM

with Input Registers, Output Registers and Pass-Through Feature

Description

The TC55BS8128J is a 1,048,576 bit synchronous static random access memory fabricated using BiCMOS technology and organized as 131,072 words by 8 bits. The TC55BS8128J is similar to the TC55BS8125J but has separate data inputs and outputs and a write-cycle pass-through feature.

Designed for pipelined architectures, this device has internal input and output registers which latch on the positive edge of an external clock (CLK). All address, data, and control signals are latched. The setup and hold times for the inputs are 2ns and 1ns respectively. Synchronous SRAMs can lead to faster, more robust system operation by virtually eliminating the timing skew problems associated with conventional asynchronous SRAMs. For example, write operations are internally self-timed when initiated - eliminating the need for accurate write pulse generation and timing by the memory controller or microprocessor. A pass-through feature during write cycles allows the outputs to follow the inputs with a one clock cycle delay. For read cycles, data is available one clock cycle after the address is latched. All inputs and outputs are TTL compatible.

The TC55BS8128J is available in a 40-pin, 400mil SOJ package suitable for high density assembly.

Features

- Fast cycle time
 - TC55BS8128J-10 10ns (max.)
 - TC55BS8128J-12 12ns (max.)
- Fast clock access time
 - TC55BS8128J-10 5ns (max.)
 - TC55BS8128J-12 6ns (max.)
- Input and output registers for synchronous operation
- Data pass-through for write cycles
- Single power supply: 5V±10%
- Separate data inputs and outputs
- Package: JEDEC standard pinout
 - 40-pin, 400mil SOJ: SOJ40-P-400

Pin Names

A0 ~ A16	Address Inputs
D0 ~ D7	Data Inputs
Q0 ~ Q7	Data Outputs
CLK	Clock Input
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
V _{DD}	Power (+5V)
GND	Ground

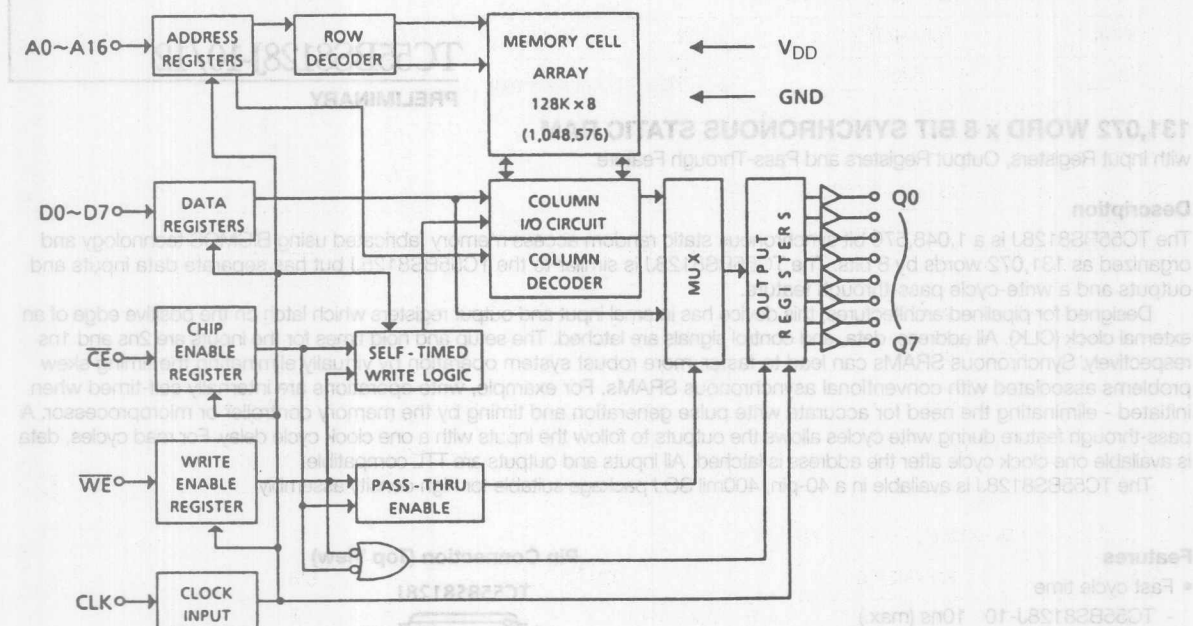
Pin Connection (Top View)

TC55BS8128J

A3	1	40	A4
A2	2	39	A5
A1	3	38	A6
A0	4	37	A7
\overline{CE}	5	36	A8
D0	6	35	D7
D1	7	34	D6
Q0	8	33	Q7
Q1	9	32	Q6
V _{DD}	10	31	GND
GND	11	30	V _{DD}
Q2	12	29	Q5
Q3	13	28	Q4
D2	14	27	D5
D3	15	26	D4
\overline{WE}	16	25	CLK
A16	17	24	A9
A15	18	23	A10
A14	19	22	A11
A13	20	21	A12

(SOJ)

Block Diagram



Operating Mode

MODE	WE	CE	D	Q (next Cycle)
Write, Pass-Through	L	L	Valid	D _{OUT}
Pass-Through	L	H	Valid	D _{OUT}
Read	H	L	*	D _{OUT}
Standby	H	H	*	High - Z

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V _{IN}	Input Voltage	-2.0 ~ 7.0	V
V _{OUT}	Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1500	mW
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-65 ~ 150	°C
T _{OPR}	Operating Temperature	-10 ~ 85	°C

Pin Names	
A0 - A16	Address Inputs
D0 - D7	Data Inputs
Q0 - Q7	Data Outputs
CLK	Clock Input
CE	Chip Enable Input
WE	Write Enable Input
V _{DD}	Power (+5V)
GND	Ground

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5	—	0.8	V

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $WE = V_{IL}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	-4	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	8	—	—	mA
I_{DDO}	Operating Current	$t_{\text{cycle}} = \text{Min cycle}$, $\overline{CE} = V_{IL}$ $I_{OUT} = 0 \text{ mA}$ Other Inputs = V_{IH}/V_{IL}	-10	—	230	mA
			-12	—	220	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
C_{CLK}	Clock Input Capacitance	$V_{CLK} = \text{GND}$	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	8	pF

* This parameter is periodically sampled and is not 100% tested.

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	UNIT	TC55BS8128J-10		TC55BS8128J-12		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{CY}	Cycle Time	ns	10	—	12	—	
t_{CHH}	Clock Pulse High Width	ns	3	—	3	—	
t_{CLL}	Clock Pulse Low Width	ns	3	—	3	—	
t_{AS}	Address Setup Time	ns	2	—	2	—	
t_{DS}	Data Input Setup Time	ns	2	—	2	—	
t_{ES}	Chip Enable Input Setup Time	ns	2	—	2	—	
t_{WS}	Write Enable Input Setup Time	ns	2	—	2	—	
t_{AH}	Address Hold Time	ns	1	—	1	—	
t_{DH}	Data Input Hold Time	ns	1	—	1	—	
t_{EH}	Chip Enable Input Hold Time	ns	1	—	1	—	
t_{WH}	Write Enable Input Hold Time	ns	1	—	1	—	
t_{ACK}	Clock Access Time	ns	1	5	1	6	
$t_{ECL(2)}$	Output Enable Time from Clock	ns	1	5	1	6	
$t_{DCL(2)}$	Output Disable Time from Clock	ns	1	5	1	6	

(1) : The operating temperature (T_a) is guaranteed with transverse air flow exceeding 500 linear feet per minute.(2) : Transition is measured $\pm 200\text{mV}$ from steady voltage with the loading in Fig.1.

AC Test Conditions

Input Pulse Levels	3.0/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig.1

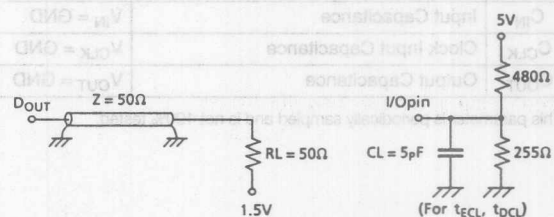
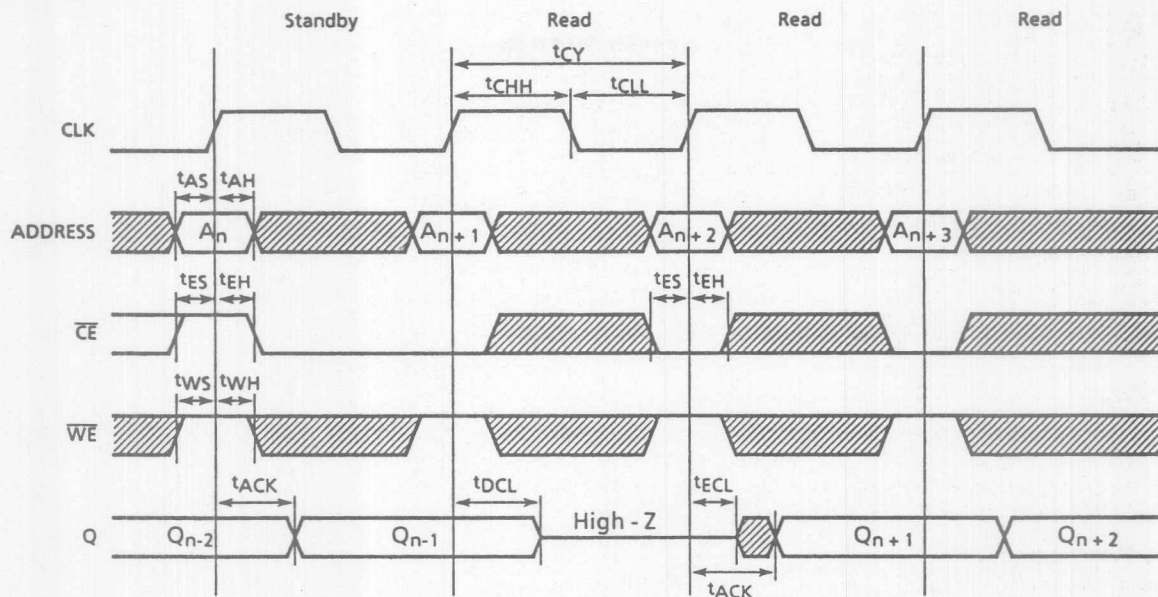


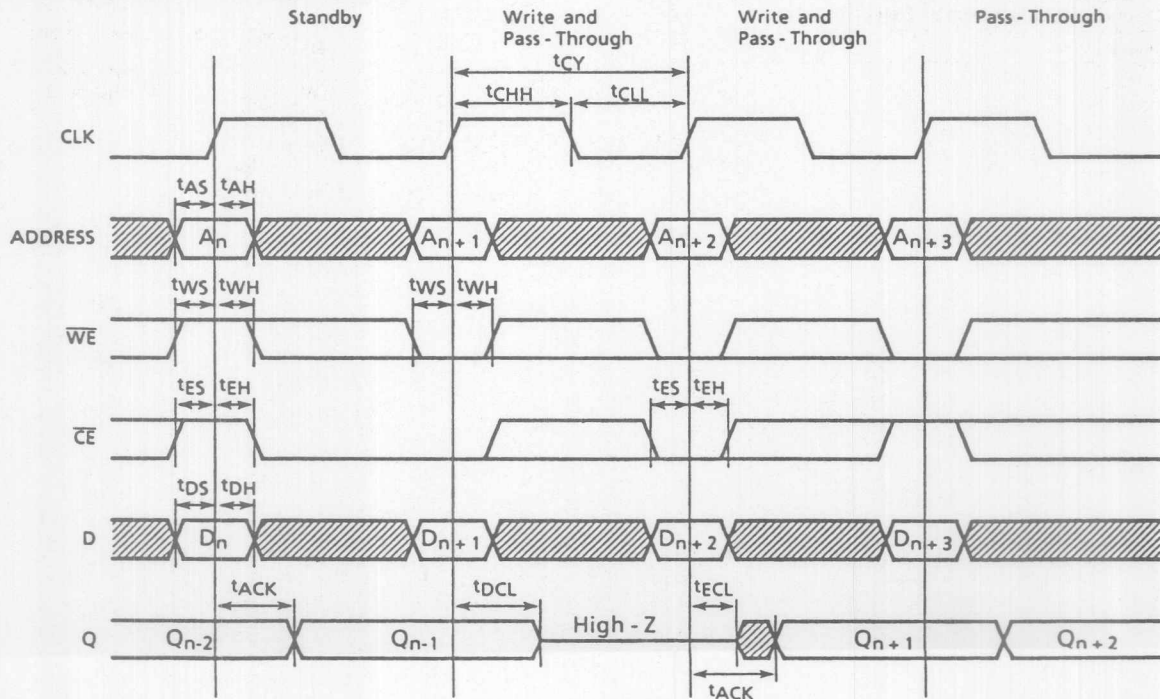
Figure 1.

Timing Waveforms

Read Cycle



Write Cycle and Pass-Through Mode



Pseudo Static SRAM

Part Number	Speed (ns)	Package	Organization	Density
D-1	70, 85, 100	P, F, SP	812K x 8	812K
D-9	70, 85, 100	P, F	812K x 8	812K
D-19	70, 85, 100	F, FT	812K x 8	812K
D-23	80, 100, 120	P, F, SP, FW, FT	128K x 8	1M
D-43	80, 100, 120	P, F, FW, FT	128K x 8	1M
D-57	70, 80, 100	P, F, SP, FW, FT	128K x 8	1M
D-67	70, 80, 100	P, F, FW, FT	128K x 8	1M
D-87	70, 80, 100	P, F, SP, FW, FT	128K x 8	1M
D-91	80, 100, 120	P, F, SP, FW, FT	128K x 8	1M
D-101	80, 100, 120	P, F, FW, FT	128K x 8	1M
D-115	70, 80, 100	FW	128K x 8	1M
D-125	80, 100	FW	128K x 8	1M
D-135	80, 100	FW	128K x 8	1M
D-145	70, 80, 100	P, FW, FT	128K x 8	1M
D-155	70, 80, 100	P, F, FT, TR	812K x 8	4M
D-167	70, 80, 100	P, F, FT, TR	812K x 8	4M
D-175	70, 80, 100	P, F, FT, TR	812K x 8	4M
D-185	70, 80, 100	P, F, FT, TR	812K x 8	4M
D-197	80, 100	P, F	812K x 8	4M
D-205	120, 150	F, FT, TR	812K x 8	4M

Pseudo SRAM

Package: P = Plastic DIP, F = Flat package (SOP), SP = Slim Plastic DIP, FW = Flat Wide package
FT = Forward band, TR = Reverse band, TSP

Pseudo Static SRAM

	Density	Organization	Package	Speed (ns)	Features	Page
TC51832A	256K	32K x 8	P, F, SP	70, 85, 100		D-1
TC51864	512K	64K x 8	P, F	85, 100		D-9
TC511632	512K	32K x 16	F, FT	70, 85, 100		D-19
TC518128A	1M	128K x 8	P, F, SP, FW, FT	80, 100, 120	CE1/CE2	D-33
TC518128A-LV	1M	128K x 8	P, F, FW, FT	80, 100, 120	CE1/CE2, Low Voltage	D-43
TC518128B	1M	128K x 8	P, F, SP, FW, FT	70, 80, 100	CE1/CE2	D-57
TC518128B-V	1M	128K x 8	P, F, FW, FT	70, 80, 100	CE1/CE2, Low Voltage	D-67
TC518128C	1M	128K x 8	P, F, SP, FW, FT	70, 80, 100	CE1/CE2	D-81
TC518129A	1M	128K x 8	P, F, SP, FW, FT	80, 100, 120	CE/CS	D-91
TC518129A-LV	1M	128K x 8	P, F, FW, FT	80, 100, 120	CE/CS, Low Voltage	D-101
TC518129AI	1M	128K x 8	FW	100	CE/CS, Ind. Temp.	D-115
TC518129B	1M	128K x 8	P, F, SP, FW, FT	70, 80, 100	CE/CS	D-125
TC518129B-V	1M	128K x 8	P, F, FW, FT	70, 80, 100	CE/CS, Low Voltage	D-135
TC518129C	1M	128K x 8	P, FW, FT	70, 80, 100	CE/CS	D-149
TC518512	4M	512K x 8	P, F, FT, TR	70, 80, 100		D-159
TC518512-(LT)	4M	512K x 8	P, F, FT, TR	70, 80, 100	Low Temp	D-167
TC518512-(DR)	4M	512K x 8	P, F, FT, TR	70, 80, 100	Data Retention	D-175
TC518512-LV	4M	512K x 8	P, F, FT, TR	70, 80, 100	Low Voltage	D-185
TC518512I	4M	512K x 8	P, F	80, 100	Industrial Temp.	D-197
TC51V8512A	4M	512K x 8	F, FT, TR	120, 150	3V Operation	D-205

Package: P = Plastic DIP, F = Flat package (SOP), SP = Slim Plastic DIP, FW = Flat Wide package
 FT = Forward bend TSOP, TR = Reverse bend TSOP

TC51832AP/ASP/AF-70/85/10 TC51832APL/ASPL/AFL-70/85/10

SILICON GATE CMOS

32,768 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC51832AP is a 256K bit high speed CMOS pseudo static RAM organized as 32,768 words by 8 bits. The TC51832AP utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC51832AP operates from a single 5V power supply. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC51832AP features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

The TC51832AP is pin-compatible with the 256K bit CMOS static RAM JEDEC standard and is available in a 28-pin, 0.6 inch and 0.3 inch width plastic DIP, and a small outline plastic flat package.

Features

- Organization: 32,768 words x 8 bits
- Single 5V power supply
- Fast access time

	TC51832A Family		
	-70	-85	-10
t _{CEA} CE Access Time	70ns	85ns	100ns
t _{OE} OE Access Time	30ns	35ns	40ns
t _{RC} Cycle Time	115ns	135ns	160ns
Power Dissipation	385mW	303mW	248mW
Self Refresh Current	1mA/100µA		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 256 refresh cycles/4ms
- Pin compatible: 256K SRAM (JEDEC)
- Package
 - TC51832AP/APL : DIP28-P-600
 - TC51832ASP/ASPL : DIP28-P-300B
 - TC51832AF/AFL : SOP28-P-450

Pin Names

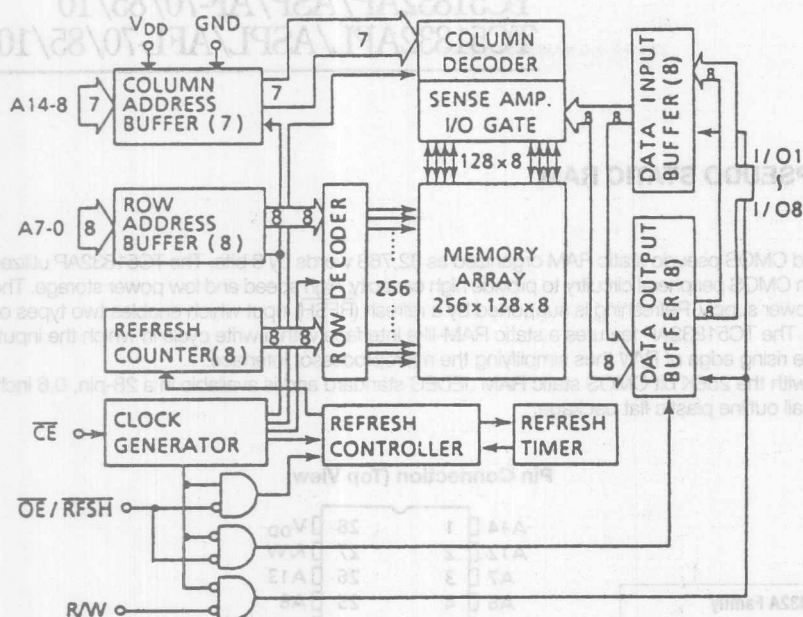
A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
OE/RFSH	Output Enable Input Refresh Input
CE	Chip Enable Input
I/O1 ~ I/O8	Data Inputs/Outputs
V _{DD}	Power
GND	Ground

Pin Connection (Top View)

A14	1	28	V _{DD}
A12	2	27	R/W
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	OE / RFSH
A2	8	21	A10
A1	9	10	CE
A0	10	19	I/O8
I/O1	11	18	I/O7
I/O2	12	17	I/O6
I/O3	13	16	I/O5
GND	14	15	I/O4

SYMBOL	ITEM	RATING	UNIT
V _{in}	Input Voltage	-1.0 ~ 7.0	V
V _{out}	Output Voltage	-1.0 ~ 7.0	V
V _{cc}	Power Supply Voltage	-1.0 ~ 7.0	V
T _{op}	Operating Temperature	0 ~ 70	°C
T _{stg}	Storage Temperature	-55 ~ 150	°C
T _{sol}	Soldering Temperature - Time	260 ± 10	°C × sec
P _d	Power Dissipation	600	mW
I _{out}	Short Circuit Output Current	50	mA

Block Diagram



Operating Mode

MODE	PIN	CE	OE/ RFSH	R/W	A0 ~ A14	I/O1 ~ 8
Read		L	L	H	V*	OUT
Write		L	H	L	V*	IN
CE only Refresh		L	H	H	V*	HZ
Auto/Self Refresh		H	L	*	*	HZ
Standby		H	H	*	*	HZ

H = High level input (V_{IH})

L = Low level input (V_{IL})

* = V_{IH} or V_{IL}

V* = At the falling edge of \overline{CE} , all address inputs are latched. At all other times, the address inputs are

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1.0$	V	2
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC \min}$.	70ns version	—	35	70	mA 3,4
		85ns version	—	30	55	
		100ns version	—	25	45	
I_{DDS1}	Standby Current $\overline{CE} = V_{IH}$, $\overline{OE}/\overline{RFSH} = V_{IH}$	TC1832AP/ASP/AF	—	—	1	mA
		TC1832APL/ASPL/AFL	—	—	1	
I_{DDS2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$, $\overline{OE}/\overline{RFSH} = V_{DD} - 0.2V$	TC1832AP/ASP/AF	—	—	1	mA
		TC1832APL/ASPL/AFL	—	—	100	
I_{DDF1}	Self Refresh Current (Average) $\overline{CE} = V_{IH}$, $\overline{OE}/\overline{RFSH} = V_{IL}$	TC1832AP/ASP/AF	—	—	1	mA
		TC1832APL/ASPL/AFL	—	—	1	
I_{DDF2}	Self Refresh Current (Average) $\overline{CE} = V_{DD} - 0.2V$, $\overline{OE}/\overline{RFSH} = 0.2V$	TC1832AP/ASP/AF	—	—	1	mA
		TC1832APL/ASPL/AFL	—	60	100	
I_{IL}	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = $0V$	—	—	± 10	μA	
I_{OL}	Output Leakage Current Output Disabled ($\overline{CE} = V_{IH}$ or $\overline{OE}/\overline{RFSH} = V_{IH}$ or $R/W = V_{IL}$) $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level $I_{OH} = -1mA$	2.4	—	—	V	
V_{OL}	Output Low Level $I_{OL} = 2.1mA$	—	—	0.4	V	

Capacitance* ($V_{DD} = 5V$, $T_a = 25^\circ\text{C}$, $f = 1MHz$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A14)	—	5	pF
C_{I2}	Input Capacitance (\overline{CE} , $\overline{OE}/\overline{RFSH}$, R/W)	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	NOTES
t_{RC}	Random Read, Write Cycle Time	115	—	135	—	160	—		
t_{RMW}	Read Modify Write Cycle Time	175	—	190	—	220	—		
t_{CE}	\overline{CE} Pulse Width	70	10,000	85	10,000	100	10,000		
t_p	\overline{CE} Precharge Time	35	—	40	—	50	—		
t_{CEA}	\overline{CE} Access Time	—	70	—	85	—	100		
t_{OEA}	\overline{OE} Access Time	—	30	—	35	—	40		
t_{CLZ}	\overline{CE} to Output in Low -Z	20	—	20	—	20	—		
t_{OLZ}	\overline{OE} to Output in Low -Z	0	—	0	—	0	—		
t_{WLZ}	Output Active from End of Write	0	—	0	—	0	—		
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	25	0	30		9
t_{OHZ}	\overline{OE} Disable to Output in High-Z	0	25	0	25	0	30		9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	25	0	30		9
t_{OSC}	\overline{OE} Setup Time Referenced to \overline{CE}	10	—	10	—	10	—		9
t_{OHC}	\overline{OE} Hold Time Referenced to \overline{CE}	0	—	0	—	0	—		9
t_{RCS}	Read Command Setup Time	0	—	0	—	0	—		
t_{RCH}	Read Command Hold Time	0	—	0	—	0	—	ns	
t_{WP}	Write Pulse Width	25	—	25	—	25	—		
t_{WCH}	Write Command Hold Time	40	—	40	—	40	—		
t_{CWL}	Write Command to \overline{CE} Lead Time	25	—	25	—	25	—		
t_{DSW}	Data Setup Time from R/W	20	—	20	—	20	—		10
t_{DSC}	Data Setup Time from \overline{CE}	20	—	20	—	20	—		10
t_{DHW}	Data Hold Time from R/W	0	—	0	—	0	—		10
t_{DHC}	Data Hold Time from \overline{CE}	0	—	0	—	0	—		10
t_{ASC}	Address Setup Time	0	—	0	—	0	—		11
t_{AHC}	Address Hold Time	20	—	20	—	20	—		11
t_{FC}	Auto Refresh Cycle Time	115	—	135	—	160	—		
t_{RFD}	\overline{RFSH} Delay Time from \overline{CE}	35	—	40	—	50	—		
t_{FAP}	\overline{RFSH} Pulse Width (Auto Refresh)	80	8,000	80	8,000	80	8,000		12
t_{FP}	\overline{RFSH} Precharge Time	30	—	30	—	30	—		12
t_{FAS}	\overline{RFSH} Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—		12
t_{FRS}	\overline{CE} Delay Time from \overline{RFSH} (Self Refresh)	115	—	135	—	160	—		12
t_{REF}	Refresh Period (256 cycles, A0 ~ A7)	—	4	—	4	—	4	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

Notes:

- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DDO} depends on the cycle time.
- 4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

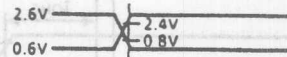
7) Timing reference levels

Input Levels

$$: V_{IH} = 2.6V$$

$$V_{IL} = 0.6V$$

INPUT

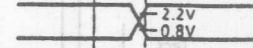


Input Reference Levels

$$: V_{IH} = 2.4V$$

$$V_{IL} = 0.8V$$

OUTPUT



Output Reference Levels

$$: V_{OH} = 2.2V$$

$$V_{OL} = 0.8V$$

INPUT REFERENCE LEVELS OUTPUT REFERENCE LEVELS

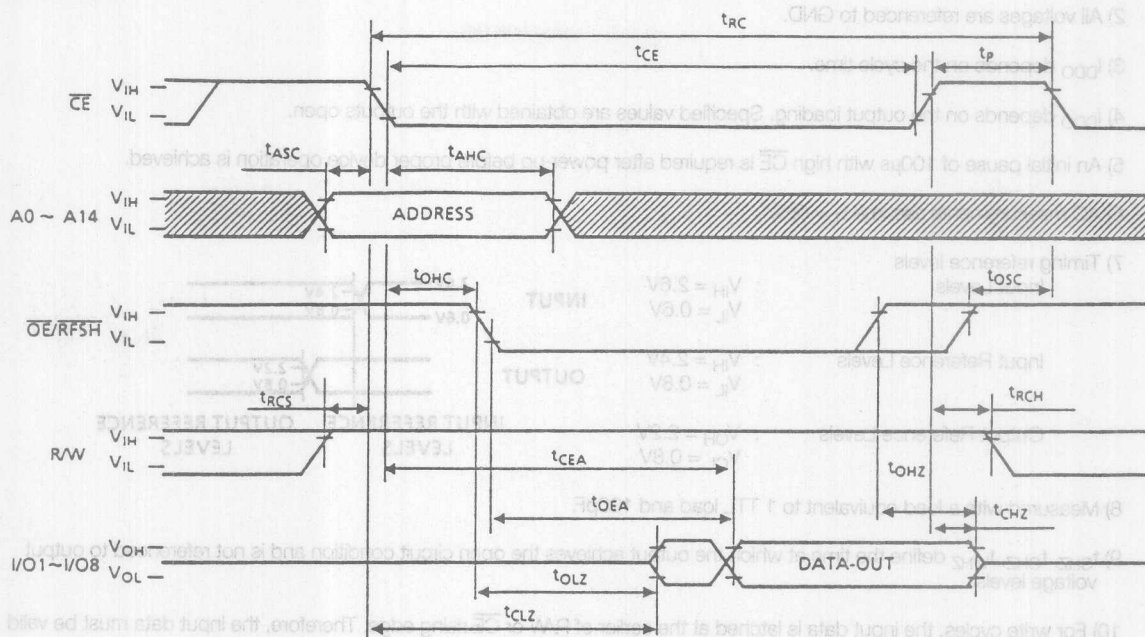
- 8) Measured with a load equivalent to 1 TTL load and 100pF.
- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) For write cycles, the input data is latched at the earlier of $R\overline{W}$ or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
- 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.
 Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

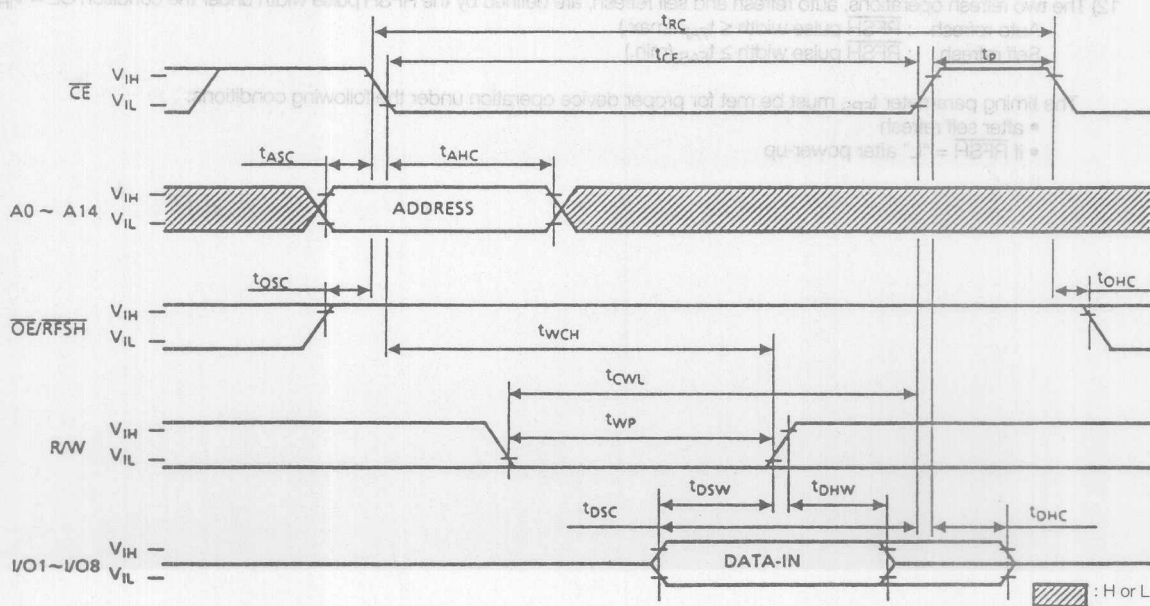
- after self refresh
- if $\overline{RFSH} = "L"$ after power-up

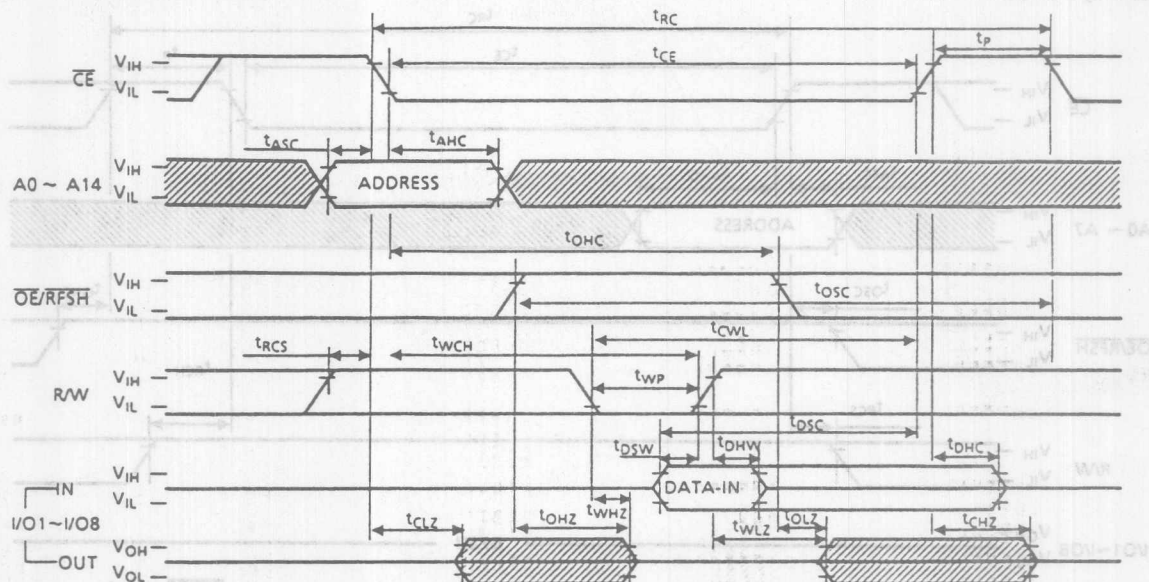
Timing Waveforms

Read Cycle

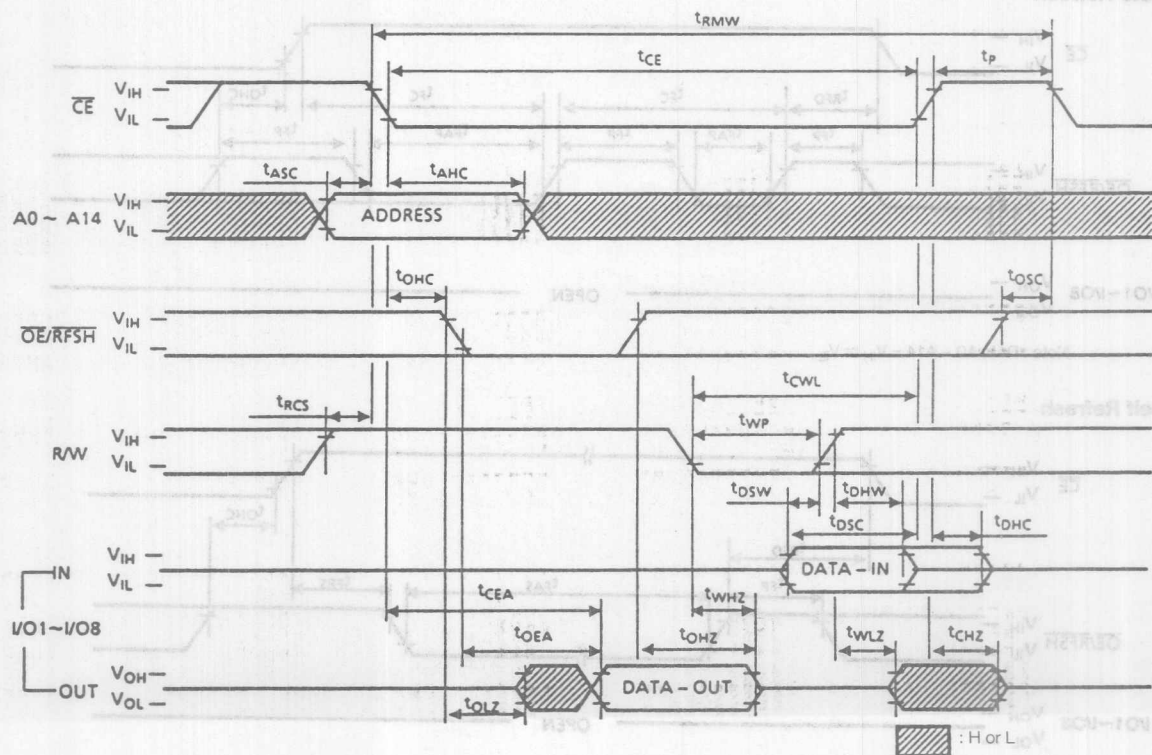


Read Modify Write Cycle

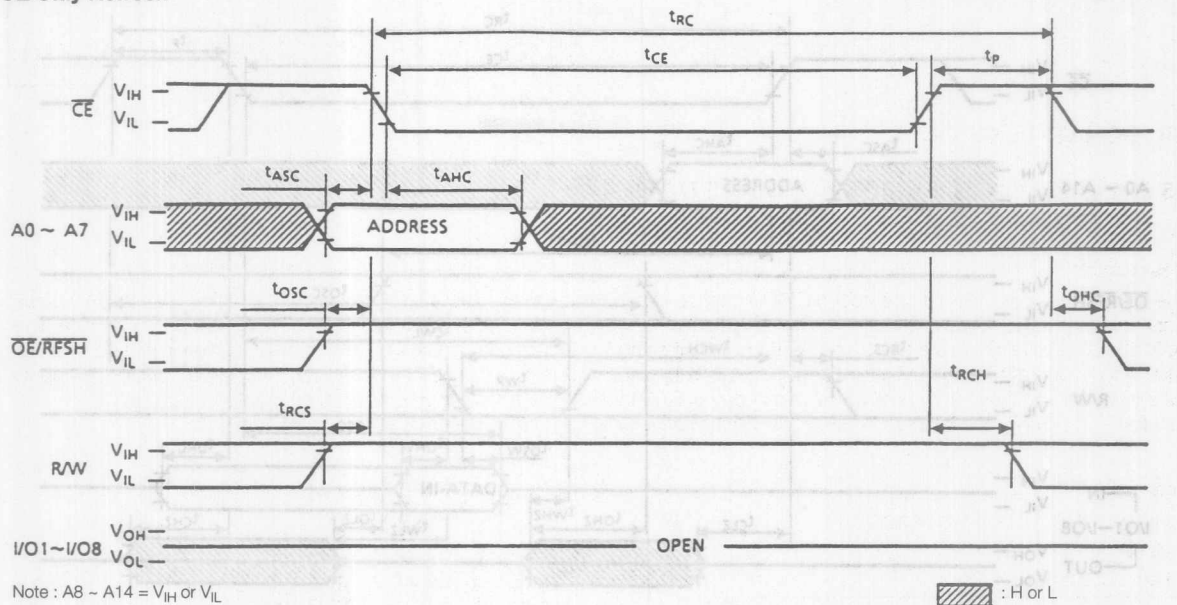


Write Cycle 2 (\overline{OE} Clocked)

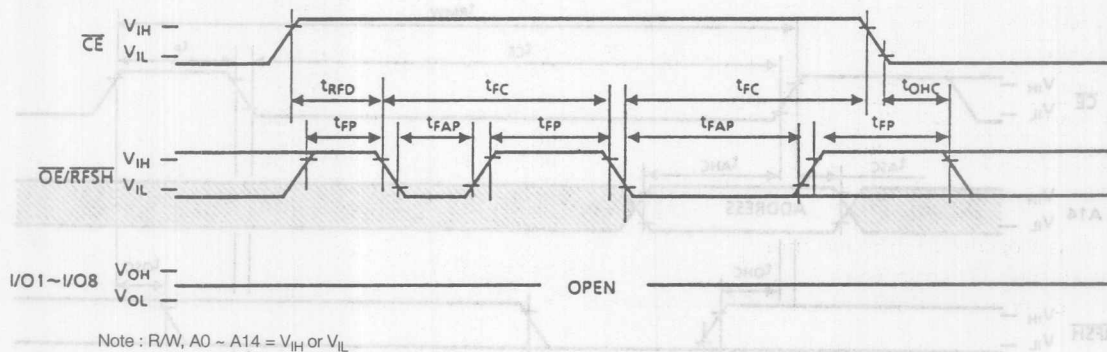
Read Modify Write Cycle



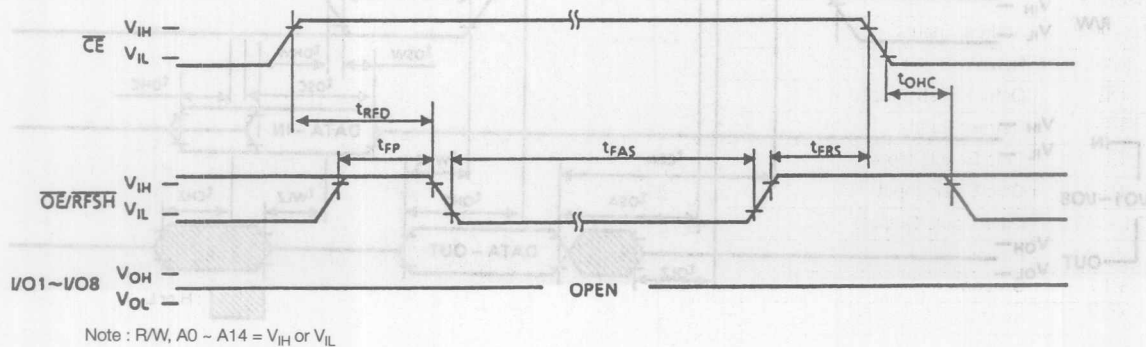
CE Only Refresh



Auto Refresh



Self Refresh



TC51864PL/FL-85/10

PRELIMINARY

SILICON GATE CMOS

65,536 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC51864PL is a 512K bit high speed CMOS pseudo static RAM organized as 65,536 words by 8 bits. The TC51864PL utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC51864PL operates from a single 5V power supply. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC51864PL features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

The TC51864PL is available in a 32-pin, 0.6 inch width plastic DIP, and a small outline plastic flat package.

Features

- Organization: 65,536 words x 8 bits
- Single 5V power supply
- Fast access time

	TC51864 Family	
	-85	-10
t_{CEA} \overline{CE} Access Time	85ns	100ns
t_{OEA} \overline{OE} Access Time	35ns	40ns
t_{RC} Cycle Time	135ns	160ns
Power Dissipation	385mW	330mW
Self Refresh Current	100 μ A	

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 256 refresh cycles/4ms
- Package
 - TC51864PL: DIP32-P-600
 - TC51864FL: SOP32-P-525

Pin Connection (Top View)

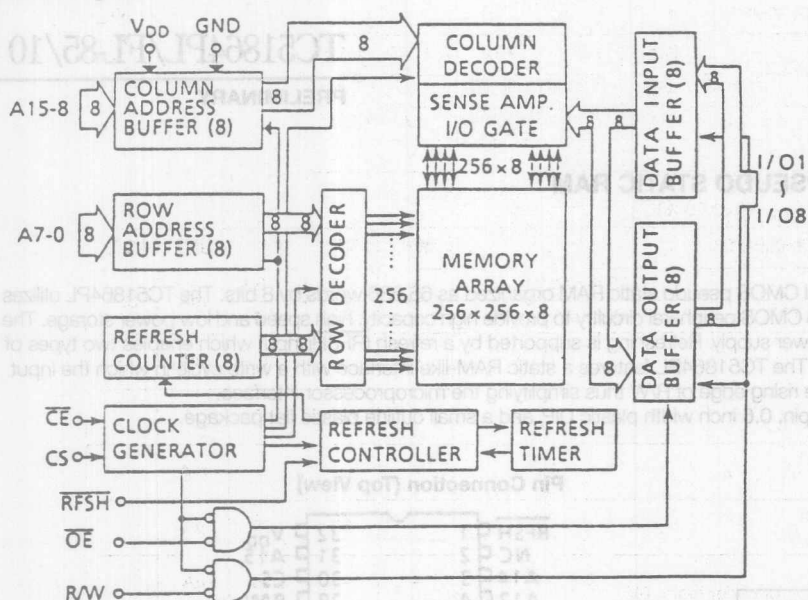
RFSH	1	32	V _{DD}
NC	2	31	A15
A14	3	30	CS
A12	4	29	R/W
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	OE
A2	10	23	A10
A1	11	22	CE
A0	12	21	I/O8
I/O1	13	20	I/O7
I/O2	14	19	I/O6
I/O3	15	18	I/O5
GND	16	17	I/O4

Pin Names

A0 ~ A15	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
RFSH	Refresh Input
\overline{CE}	Chip Enable Input
CS	Chip Select Input
I/O1 ~ I/O8	Data Inputs/Outputs
V _{DD}	Power
GND	Ground
NC	No Connect

SYMBOL	ITEM	RATING	UNIT	NOTE
V _{DD}	Supply Voltage	4.5 - 5.5	V	
V _{OUT}	Output Voltage	4.5 - 5.5	V	
V _{DD}	Power Supply Voltage	4.5 - 5.5	V	
T _{OP}	Operating Temperature	0 - 70	°C	
T _{STG}	Storage Temperature	-55 - 150	°C	
T _{SOBJ}	Soldering Temperature - Time	260 - 10	°C - sec	
P _D	Power Dissipation	385	mW	
I _{OUT}	Output Current	50	mA	

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	CS	\overline{OE}	R/W	RFSH	A0 ~ A15	I/O1 ~ 8
Read		L	H	L	H	*	V*	OUT
Write		L	H	*	L	*	V*	IN
\overline{CE} only Refresh		L	H	H	H	*	V*	HZ
CS Standby		L	L	*	*	*	*	HZ
Auto/Self Refresh		H	*	*	*	L	*	HZ
Standby		H	*	*	*	H	*	HZ

H = High level input (V_{IH})L = Low level input (V_{IL})* = V_{IH} or V_{IL} V* = At the falling edge of \overline{CE} , all address inputs are latched. At all other times, the address inputs are "**.

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1.0$	V	
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) CE, Address cycling: $t_{RC} = t_{RC \text{ min.}}$	85ns version	—	50	70	mA 3, 4
		100ns version	—	40	60	
I_{DDS1}	Standby Current $\overline{CE} = V_{IH}$, $RFSH = V_{IH}$	—	—	1	mA	
I_{DDS2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$, $RFSH = V_{DD} - 0.2V$	—	—	100	μA	
I_{DDF1}	Self Refresh Current (Average) $\overline{CE} = V_{IH}$, $RFSH = V_{IL}$	—	—	1	mA	
I_{DDF2}	Self Refresh Current (Average) $\overline{CE} = V_{DD} - 0.2V$, $RFSH = 0.2V$	—	50	100	μA	
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = $0V$	—	—	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disabled ($\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $R/W = V_{IL}$) $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level $I_{OH} = -1mA$	2.4	—	—	V	
V_{OL}	Output Low Level $I_{OL} = 2.1mA$	—	—	0.4	V	

Capacitance* ($V_{DD} = 5V$, $T_a = 25^\circ\text{C}$, $f = 1MHz$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 - A15)	—	5	pF
C_{I2}	Input Capacitance (\overline{CE} , CS, \overline{OE} , R/W, RFSH)	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

SYMBOL	PARAMETER	-85		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	135	—	160	—		
t_{RMW}	Read Modify Write Cycle Time	190	—	220	—		
t_{CE}	\overline{CE} Pulse Width	85	10,000	100	10,000		
t_P	\overline{CE} Precharge Time	40	—	50	—		
t_{CEA}	\overline{CE} Access Time	—	85	—	100		
t_{OEA}	\overline{OE} Access Time	—	35	—	40		
t_{CLZ}	\overline{CE} to Output in Low -Z	20	—	20	—		
t_{OLZ}	\overline{OE} to Output in Low -Z	0	—	0	—		
t_{WLZ}	Output Active from End of Write	0	—	0	—		
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30		9
t_{OHZ}	\overline{OE} Disable to Output in High-Z	0	25	0	30		9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30		9
t_{ODS}	\overline{OE} Output Disable Setup Time	0	—	0	—		
t_{ODH}	\overline{OE} Output Disable Hold Time	10	—	10	—		
t_{RCS}	Read Command Setup Time	0	—	0	—		
t_{RCH}	Read Command Hold Time	0	—	0	—		
t_{CSS}	Chip Select Setup Time	0	—	0	—		
t_{CSH}	Chip Select Hold Time	20	—	20	—	ns	
t_{WP}	Write Pulse Width	25	—	25	—		
t_{WCH}	Write Command Hold Time	40	—	40	—		
t_{CWL}	Write Command to \overline{CE} Lead Time	25	—	25	—		
t_{DSW}	Data Setup Time from R/W	20	—	20	—		10
t_{DSC}	Data Setup Time from \overline{CE}	20	—	20	—		10
t_{DHW}	Data Hold Time from R/W	0	—	0	—		10
t_{DHC}	Data Hold Time from \overline{CE}	0	—	0	—		10
t_{ASC}	Address Setup Time	0	—	0	—		11
t_{AHC}	Address Hold Time	20	—	20	—		11
t_{RHC}	RFSH Command Hold Time	15	—	15	—		
t_{FC}	Auto Refresh Cycle Time	135	—	160	—		
t_{RFD}	RFSH Delay Time from \overline{CE}	40	—	50	—		
t_{FAP}	RFSH Pulse Width (Auto Refresh)	80	8,000	80	8,000		12
t_{FP}	RFSH Precharge Time	30	—	30	—		12
t_{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	8,000	—		12
t_{FRS}	\overline{CE} Delay Time from RFSH (Self Refresh)	135	—	160	—		12
t_{REF}	Refresh Period (256 cycles, A0 ~ A7)	—	4	—	4	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	

Notes:

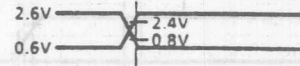
- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DDO} depends on the cycle time.
- 4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

7) Timing reference levels

Input Levels

$$\begin{aligned} &: V_{IH} = 2.6V \\ &V_{IL} = 0.6V \end{aligned}$$

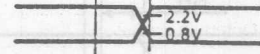
INPUT



Input Reference Levels

$$\begin{aligned} &: V_{IH} = 2.4V \\ &V_{IL} = 0.8V \end{aligned}$$

OUTPUT



Output Reference Levels

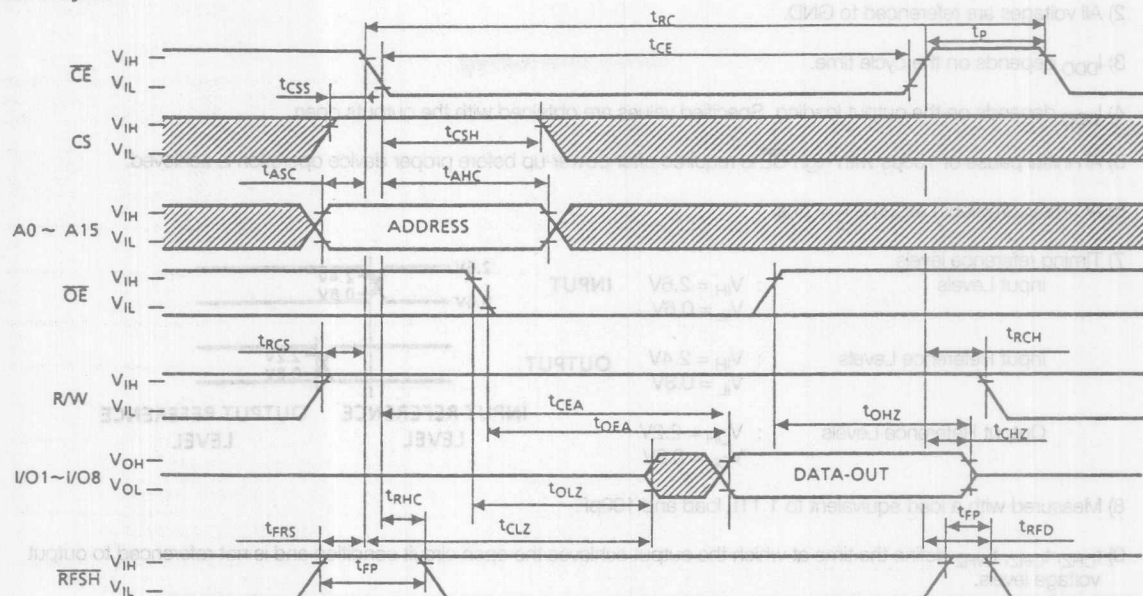
$$\begin{aligned} &: V_{OH} = 2.2V \\ &V_{OL} = 0.8V \end{aligned}$$

INPUT REFERENCE
LEVELOUTPUT REFERENCE
LEVEL

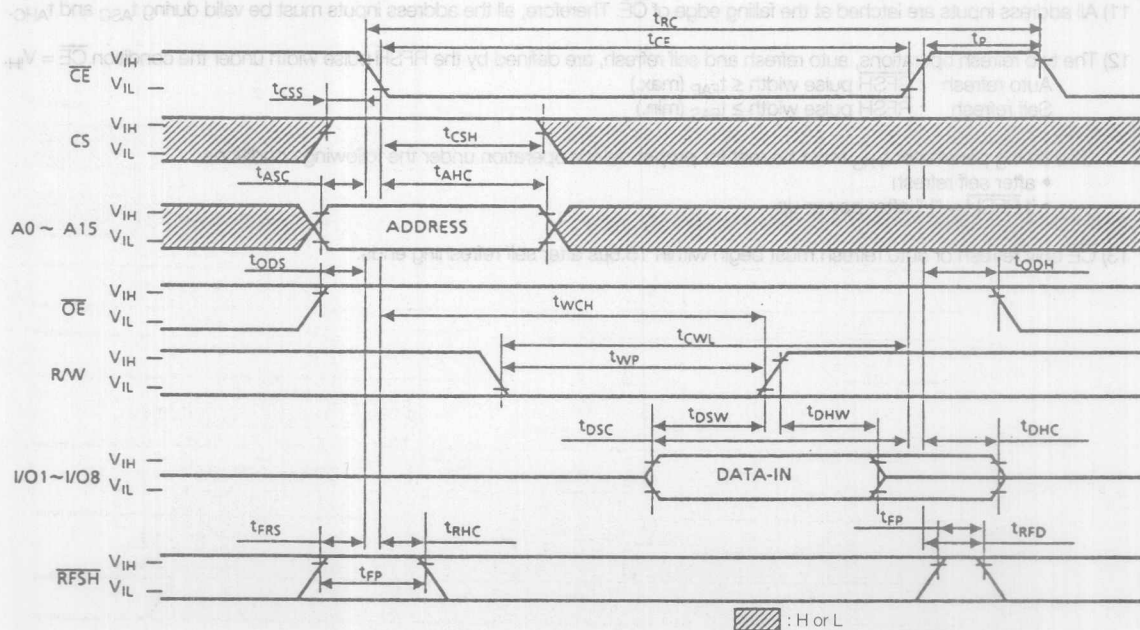
- 8) Measured with a load equivalent to 1 TTL load and 100pF.
 - 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 - 10) For write cycles, the input data is latched at the earlier of R/W or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
 - 11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
 - 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.
 Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)
- The timing parameter t_{FRS} must be met for proper device operation under the following conditions:
- after self refresh
 - if $\overline{RFSH} = "L"$ after power-up
- 13) \overline{CE} only refresh or auto refresh must begin within 15.6 μ s after self refreshing ends.

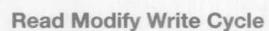
Timing Waveforms

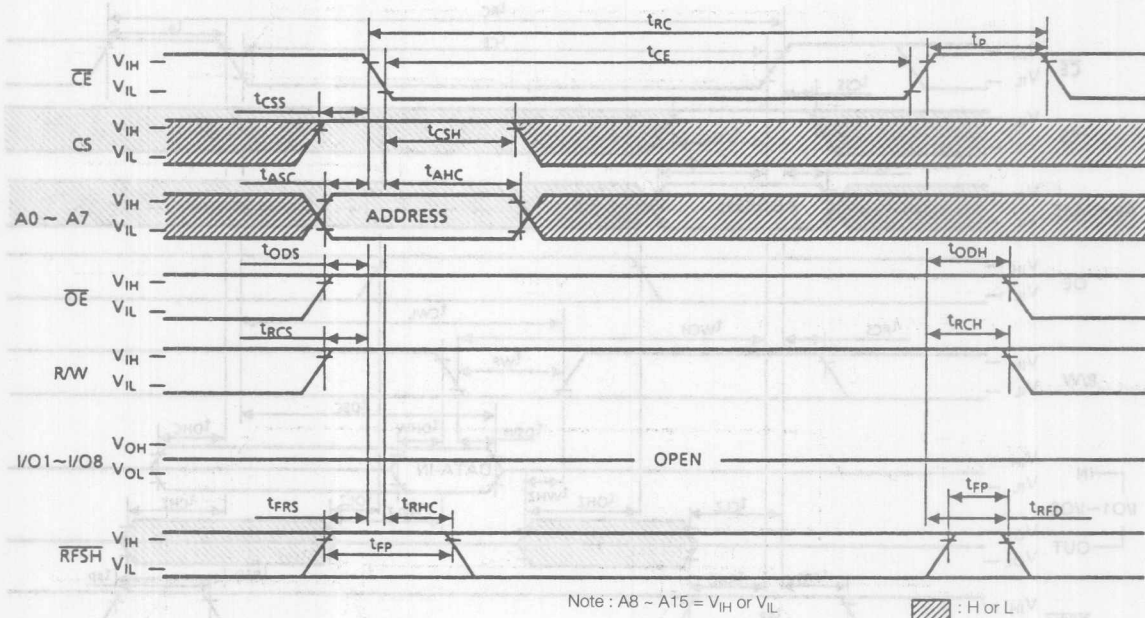
Read Cycle



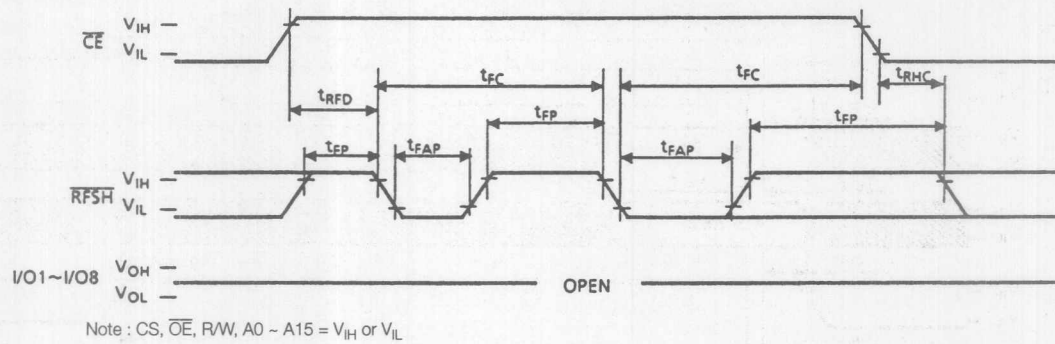
Write Cycle 1 ($\overline{\text{OE}}$ Fixed High)



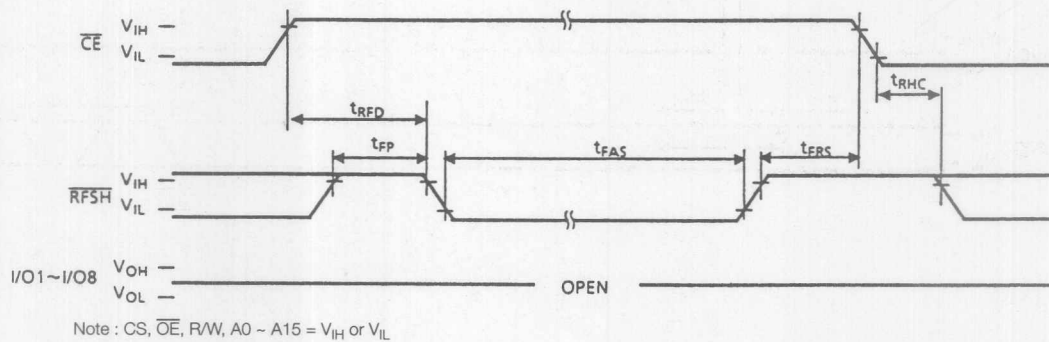


\overline{CE} Only Refresh

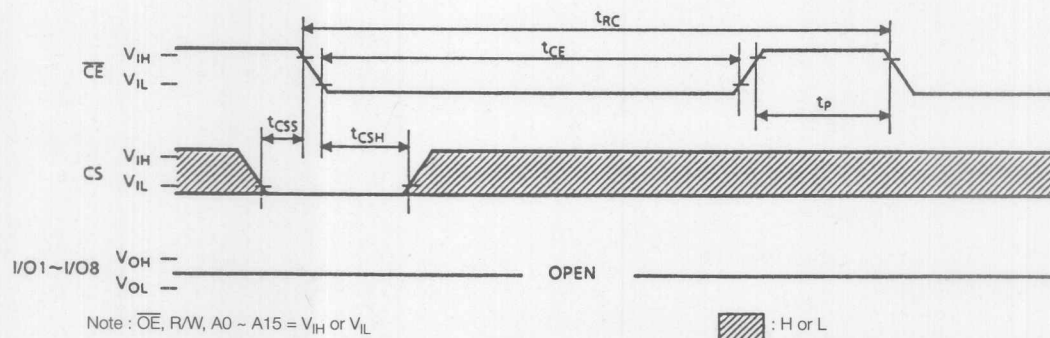
Auto Refresh



Self Refresh



CS Standby Mode



Static RAM

Notes

TC511632FL/FTL-70/85/10

PRELIMINARY

SILICON GATE CMOS

32,768 WORD x 16 BIT CMOS PSEUDO STATIC RAM

Description

The TC511632FL/FTL is a 512K bit high speed CMOS pseudo static RAM organized as 32,768 words by 16 bits. The TC511632FL/FTL utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC511632FL/FTL operates from a single 5V power supply. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC511632FL/FTL features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of WE thus simplifying the microprocessor interface.

The TC511632FL/FTL is available in a 40-pin small outline plastic flat package and a 44-pin outline (40 actual pins) plastic thin small outline package (forward type).

Features

- Organization: 32,768 words x 16 bits
- Single 5V power supply
- Fast access time

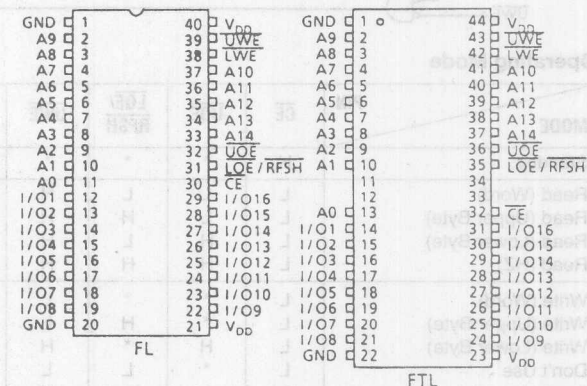
	TC511632FL/FTL		
	-70	-85	-10
t_{CEA} \overline{CE} Access Time	70ns	85ns	100ns
t_{OEA} \overline{OE} Access Time	30ns	35ns	40ns
t_{RC} Cycle Time	115ns	135ns	160ns
Power Dissipation	440mW	385mW	330mW
Self Refresh Current	100 μ A		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 256 refresh cycles/4ms
- Package
 - TC511632FL: SOP40-P-525
 - TC511632FTL: TSOP44-P-400B

Pin Names

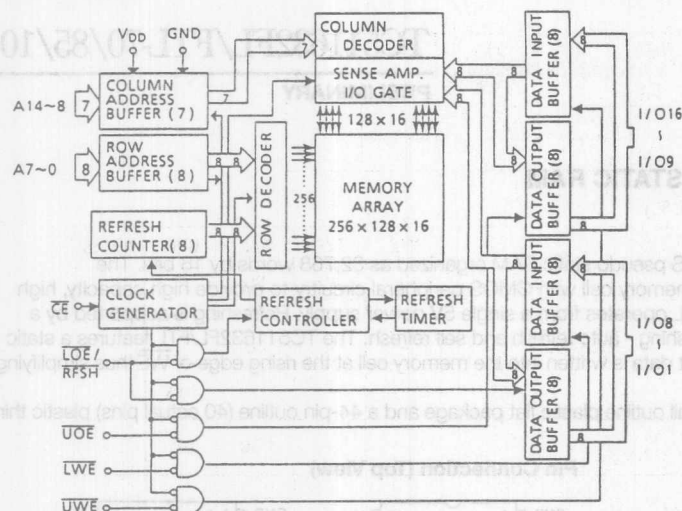
A0 ~ A14	Address Inputs
\overline{UWE}	Upper Byte Write Enable Input
\overline{LWE}	Lower Byte Write Enable Input
\overline{UOE}	Upper Byte Output Enable Input
$\overline{LOE/RFSH}$	Lower Byte Output Enable Input Refresh Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O16	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

Pin Connection (Top View)



SYMBOL	ITEM	RATING	UNIT	NOTES
V_{in}	Input Voltage	-0.5 ~ 5.5	V	
V_{out}	Output Voltage	-0.5 ~ 5.5	V	
V_{DD}	Power Supply Voltage	-0.5 ~ 5.5	V	
T_{op}	Operating Temperature	0 ~ 70	$^{\circ}$ C	
T_{stg}	Storage Temperature	-55 ~ 125	$^{\circ}$ C	
T_{sol}	Soldering Temperature - Time	260 \pm 10	$^{\circ}$ C * sec	
P_d	Power Dissipation	440	mW	
I_{out}	Static Output Current	50	μ A	

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{UOE}	$\overline{LOE/RFSH}$	\overline{UWE}	\overline{LWE}	A0 ~ A14	I/O9 ~ 16	I/O1 ~ 8
Standby		H	*	*	*	*	*	HZ	HZ
Read (Word)		L	L	L	H	H	V*	D _{OUT}	D _{OUT}
Read (Upper Byte)		L	L	H	H	H	V*	D _{OUT}	HZ
Read (Lower Byte)		L	H	L	H	H	V*	HZ	D _{OUT}
Read (HZ)		L	H	H	H	H	V*	HZ	HZ
Write (Word)		L	*	*	L	L	V*	D _{IN}	D _{IN}
Write (Upper Byte)		L	*	H	L	H	V*	D _{IN}	*
Write (Lower Byte)		L	H	*	H	L	V*	*	D _{IN}
Don't Use		L	*	L	L	H	*	-	-
Don't Use		L	L	*	H	L	*	-	-
\overline{CE} only Refresh		\overline{H}	H	H	H	H	V*	HZ	HZ
Auto/Self Refresh		H	*	\overline{H}	*	*	V*	HZ	HZ

H = High level input (V_{IH})L = Low level input (V_{IL})* = V_{IH} or V_{IL} V* = At the falling edge of \overline{CE} , all address inputs are latched. At all other times, the address inputs are **.

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V _{IH}	Input High Voltage	2.4	—	V _{DD} + 1.0	V	
V _{IL}	Input Low Voltage	-0.5	—	0.8	V	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I _{DDO}	Operating Current (Average) CE, Address cycling: t _{RC} = t _{RC} min.	70ns version	—	60	80	mA 3, 4
		85ns version	—	50	70	
		100ns version	—	40	60	
I _{DDs1}	Standby Current CE = V _{IH} , All other pins = V _{IH} or V _{IL}	—	—	1	mA	
I _{DDs2}	Standby Current CE = V _{DD} - 0.2V, All other pins = V _{DD} - 0.2V or 0.2V	—	—	100	μA	
I _{DDF1}	Self Refresh Current (Average) CE = V _{IH} , LOE/RFSH = V _{IL} , All other pins = V _{IH} or V _{IL}	—	—	1	mA	
I _{DDF2}	Self Refresh Current (Average) CE = V _{DD} - 0.2V, LOE/RFSH = 0.2V, All other pins = V _{DD} - 0.2V or 0.2V	—	50	100	μA	
I _{I(L)}	Input Leakage Current 0V ≤ V _{IN} ≤ V _{DD} , All other inputs not under test = 0V	—	—	±10	μA	
I _{O(L)}	Output Leakage Current Output Disabled (CE = V _{IH} or LOE/RFSH = V _{IH} or UOE = V _{IH} , UWE = V _{IL}) 0V ≤ V _{OUT} ≤ V _{DD}	—	—	±10	μA	
V _{OH}	Output High Level I _{OH} = -1mA	2.4	—	—	V	
V _{OL}	Output Low Level I _{OL} = 2.1mA	—	—	0.4	V	

Capacitance* (V_{DD} = 5V, Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{I1}	Input Capacitance (A0 ~ A14)	—	5	pF
C _{I2}	Input Capacitance (CE, LOE/RFSH, UOE, LWE, UWE)	—	7	
C _{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%) (Notes: 5, 6, 7, 8, 13)

SYMBOL	PARAMETER	-70		-85		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	115	—	135	—	160	—		
t _{RMW}	Read Modify Write Cycle Time	175	—	190	—	220	—		
t _{CE}	$\overline{\text{CE}}$ Pulse Width	70	10,000	85	10,000	100	10,000		
t _p	$\overline{\text{CE}}$ Precharge Time	35	—	40	—	50	—		
t _{CEA}	$\overline{\text{CE}}$ Access Time	—	70	—	85	—	100		
t _{OEa}	$\overline{\text{OE}}$ Access Time	—	30	—	35	—	40		
t _{CLZ}	$\overline{\text{CE}}$ to Output in Low -Z	20	—	20	—	20	—		
t _{OLZ}	$\overline{\text{OE}}$ to Output in Low -Z	0	—	0	—	0	—		
t _{WLZ}	Output Active from End of Write	0	—	0	—	0	—		
t _{CHZ}	Chip Disable to Output in High-Z	0	25	0	25	0	30	9	
t _{OHZ}	$\overline{\text{OE}}$ Enable to Output in High-Z	0	25	0	25	0	30	9	
t _{WHZ}	Write Enable to Output in High-Z	0	25	0	25	0	30	9	
t _{OSC}	$\overline{\text{OE}}$ Setup Time Referenced to $\overline{\text{CE}}$	10	—	10	—	10	—	9	
t _{LOHC}	$\overline{\text{LOE}}$ Hold Time Referenced to $\overline{\text{CE}}$	0	t _{CE}	0	t _{CE}	0	t _{CE}	9	
t _{UOHC}	$\overline{\text{UOE}}$ Hold Time Referenced to $\overline{\text{CE}}$	0	—	0	—	0	—	9	
t _{LWED}	From $\overline{\text{LOE}}$ Disable to $\overline{\text{LWE}}$ Enable	0	—	0	—	0	—	9	
t _{UWED}	From $\overline{\text{LOE}}$ Disable to $\overline{\text{UWE}}$ Enable	0	—	0	—	0	—	9	
t _{RCS}	Read Command Setup Time	0	—	0	—	0	—	ns	
t _{RCH}	Read Command Hold Time	0	—	0	—	0	—		
t _{WP}	Write Pulse Width	25	—	25	—	25	—		
t _{WCH}	Write Command Hold Time	40	—	40	—	40	—		
t _{CWL}	Write Command to $\overline{\text{CE}}$ Lead Time	25	—	25	—	25	—		
t _{DSW}	Data Setup Time from R/W	20	—	20	—	20	—	10	
t _{DSC}	Data Setup Time from $\overline{\text{CE}}$	20	—	20	—	20	—	10	
t _{DHW}	Data Hold Time from R/W	0	—	0	—	0	—	10	
t _{DHC}	Data Hold Time from $\overline{\text{CE}}$	0	—	0	—	0	—	10	
t _{ASC}	Address Setup Time	0	—	0	—	0	—	11	
t _{AHC}	Address Hold Time	20	—	20	—	20	—	11	
t _{FC}	Auto Refresh Cycle Time	115	—	135	—	160	—		
t _{RFD}	$\overline{\text{RFSH}}$ Delay Time from $\overline{\text{CE}}$	35	—	40	—	50	—		
t _{FAP}	$\overline{\text{RFSH}}$ Pulse Width (Auto Refresh)	80	8,000	80	8,000	80	8,000	12	
t _{FP}	$\overline{\text{RFSH}}$ Precharge Time	30	—	30	—	30	—	12	
t _{FAS}	$\overline{\text{RFSH}}$ Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—	12	
t _{FRS}	$\overline{\text{CE}}$ Delay Time from $\overline{\text{RFSH}}$ (Self Refresh)	115	—	135	—	160	—	12	
t _{REF}	Refresh Period (256 cycles, A0 ~ A7)	—	4	—	4	—	4	ms	
t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.

2) All voltages are referenced to GND.

3) I_{DDO} depends on the cycle time.

4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.

5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.

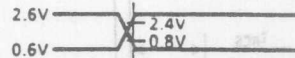
6) AC measurements assume $t_T = 5$ ns.

7) Timing reference levels

Input Levels

: $V_{IH} = 2.6V$
 $V_{IL} = 0.6V$

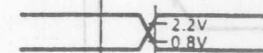
INPUT



Input Reference Levels

: $V_{IH} = 2.4V$
 $V_{IL} = 0.8V$

OUTPUT



Output Reference Levels

: $V_{OH} = 2.2V$
 $V_{OL} = 0.8V$

INPUT REFERENCE
LEVEL

OUTPUT REFERENCE
LEVEL

8) Measured with a load equivalent to 1 TTL load and 100pF.

9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10) For write cycles, the input data is latched at the earlier of \overline{WE} or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).

11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .

12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.

Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)

Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

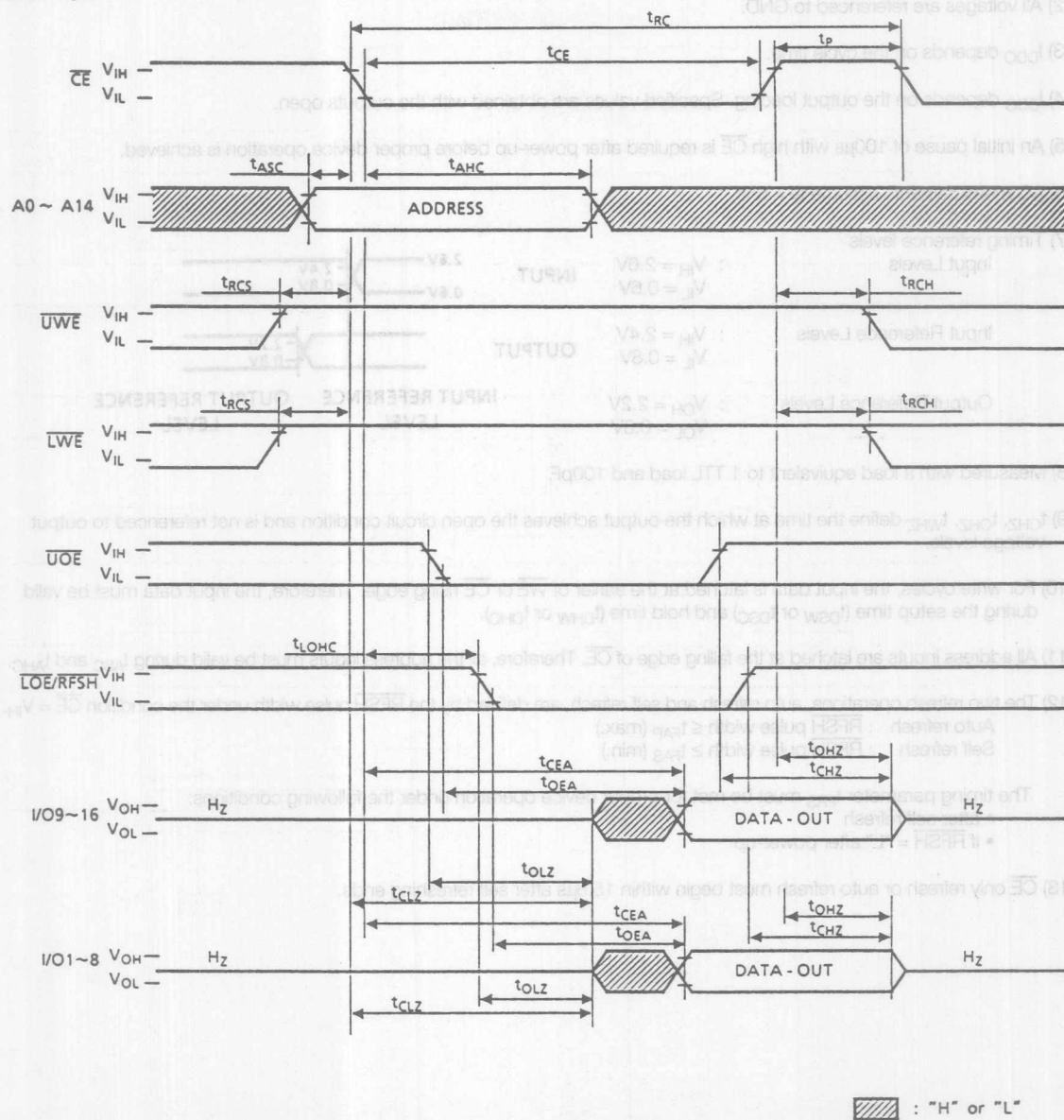
The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

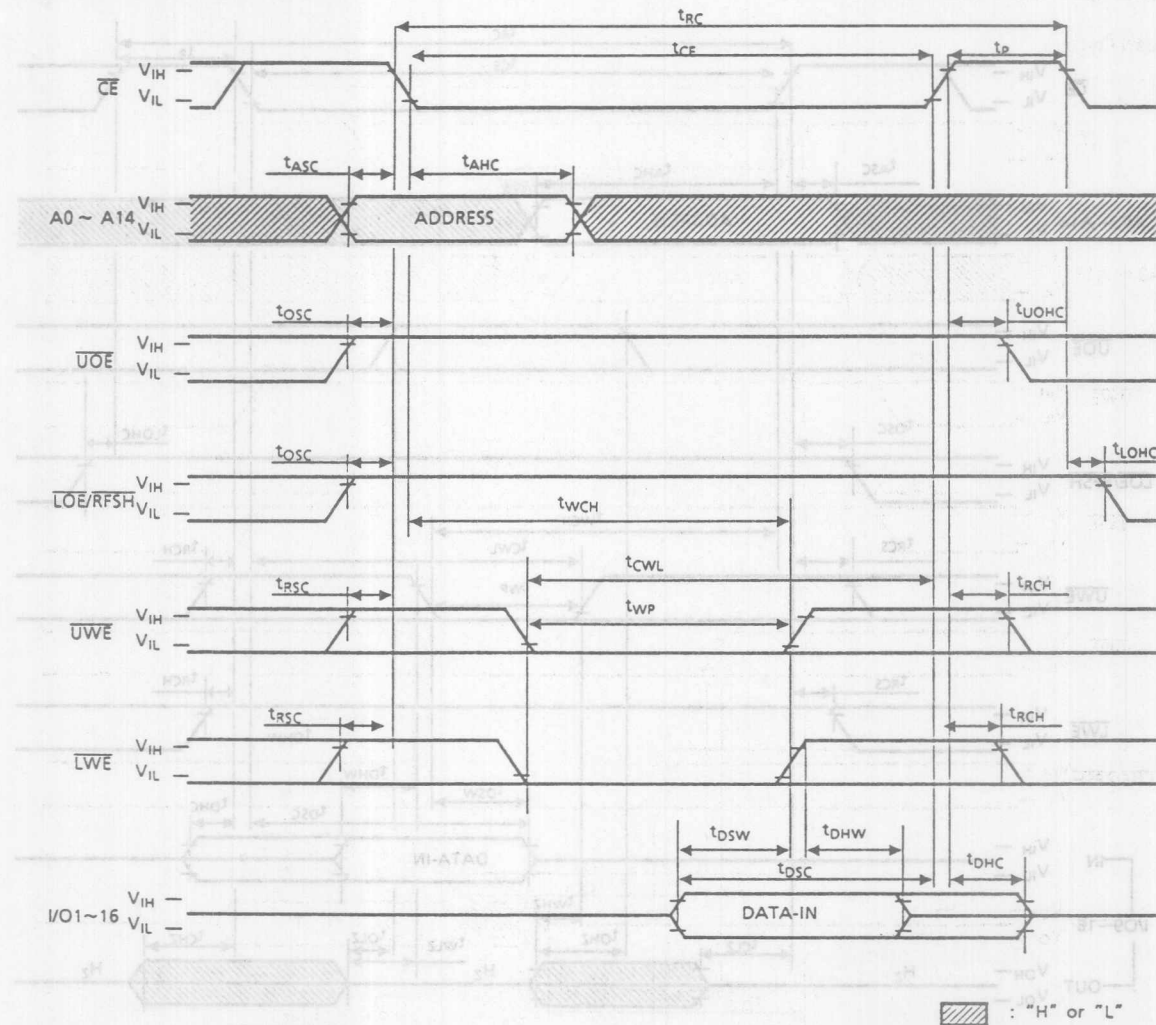
- after self refresh
- if $\overline{RFSH} = "L"$ after power-up

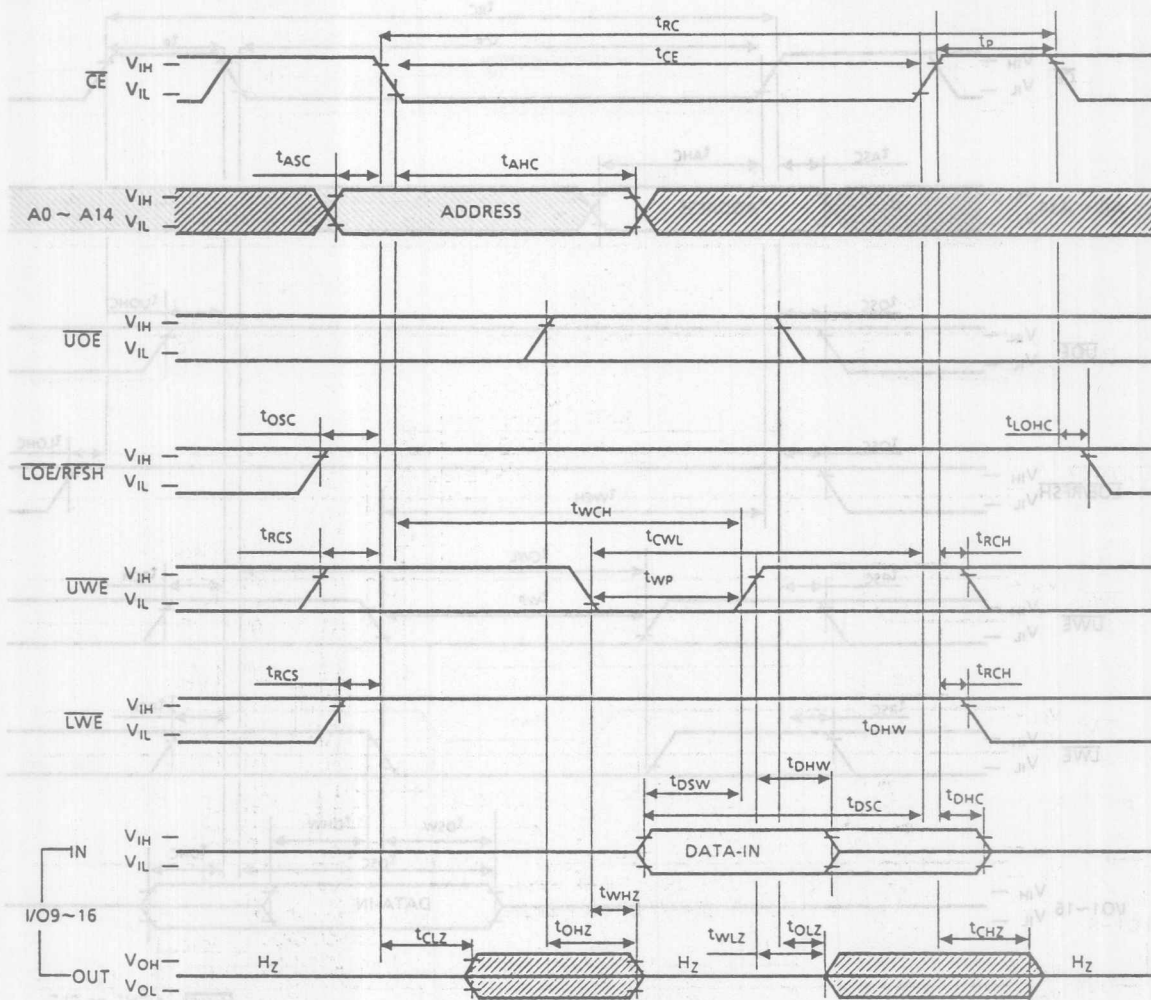
13) \overline{CE} only refresh or auto refresh must begin within 15.6 μ s after self refreshing ends.

Timing Waveforms

Read Cycle

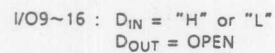



Write Cycle 1 (\overline{OE} Fixed High)

Upper Byte Write Cycle 2 ($\overline{\text{OE}}$ Clocked)

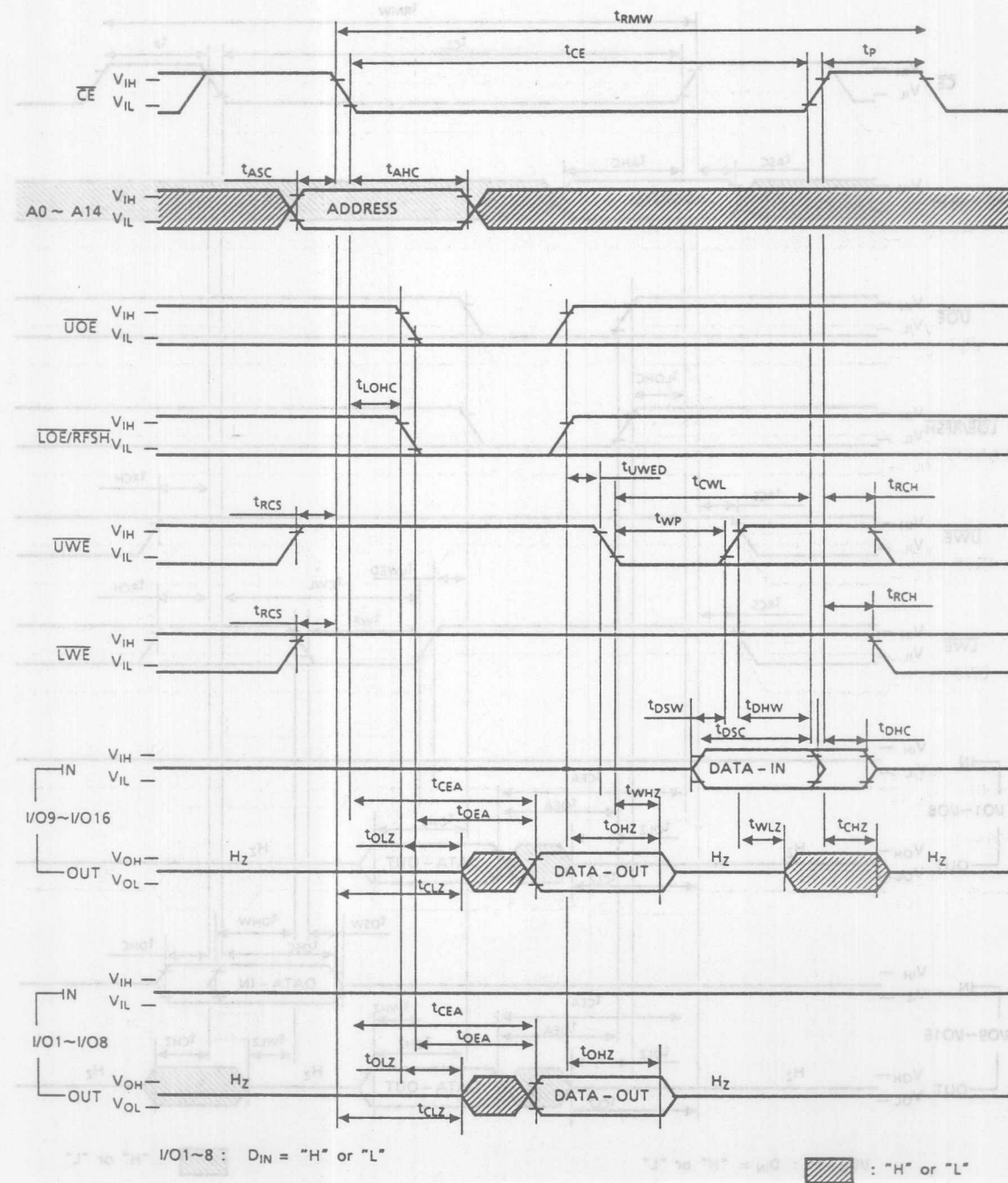
I/O1~8 : D_{IN} = "H" or "L"
 D_{OUT} = OPEN

▨ : "H" or "L"

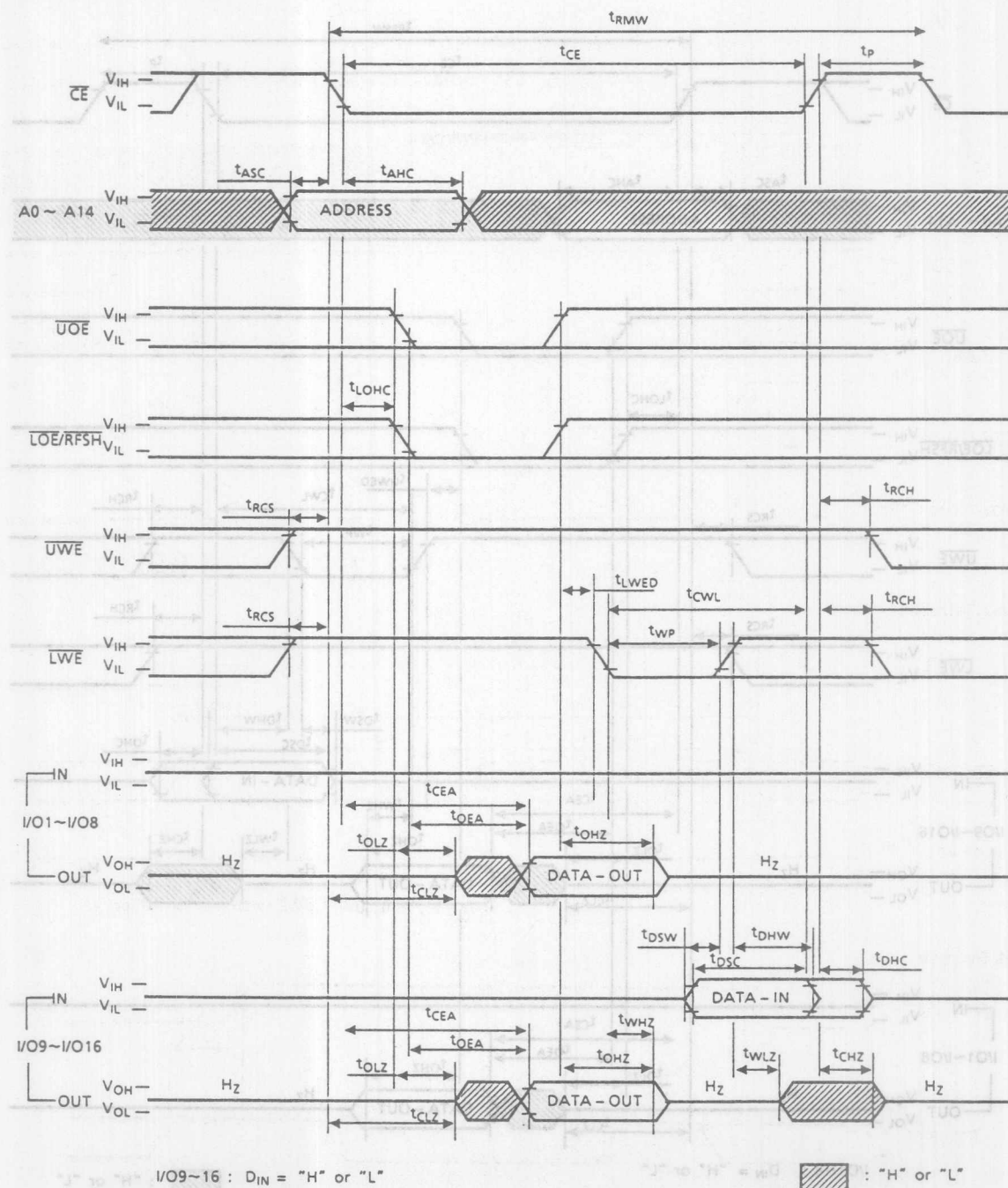


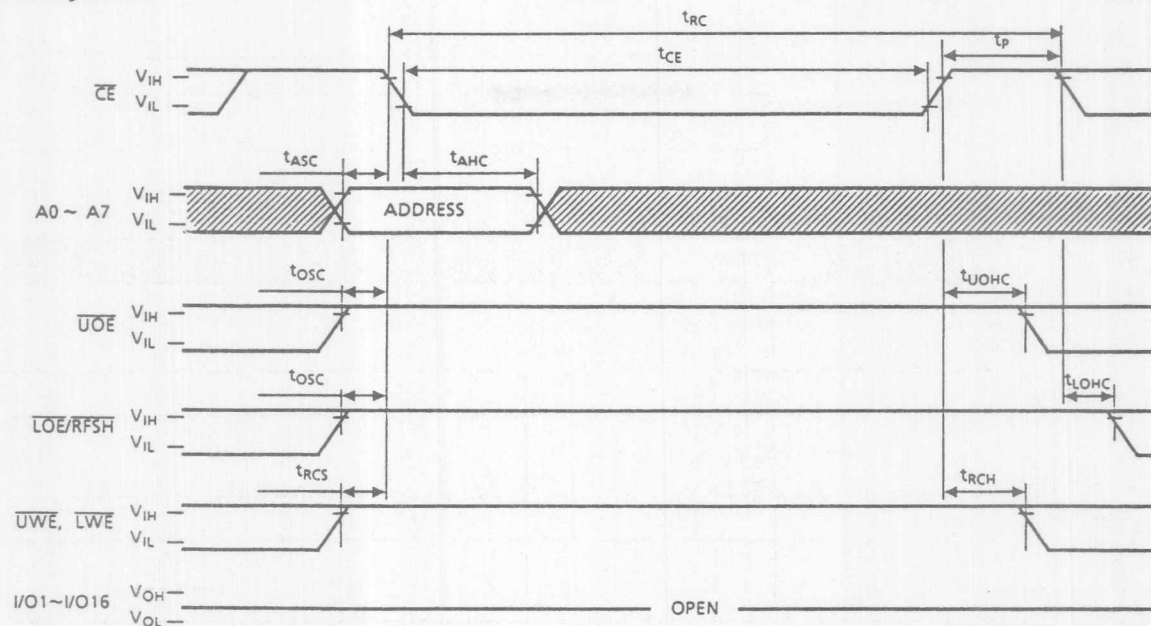

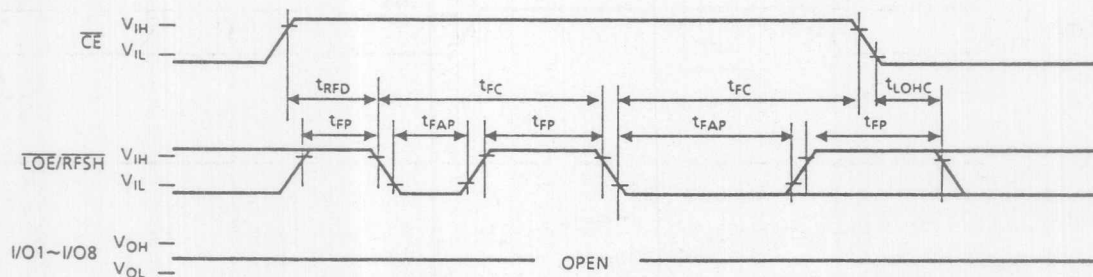
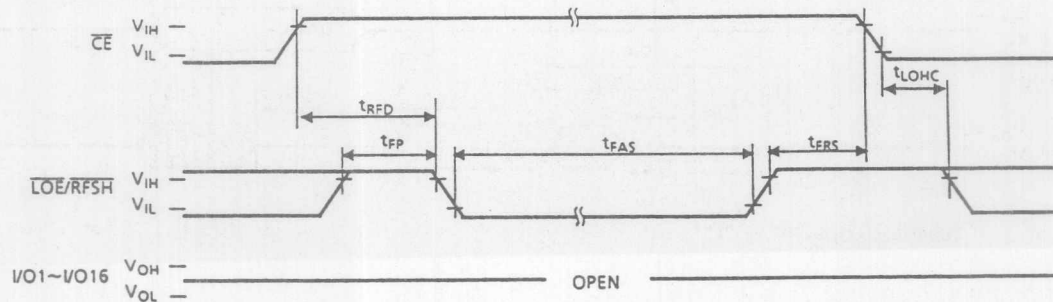
 : "H" or "L"

Upper Byte Read Modify Write Cycle



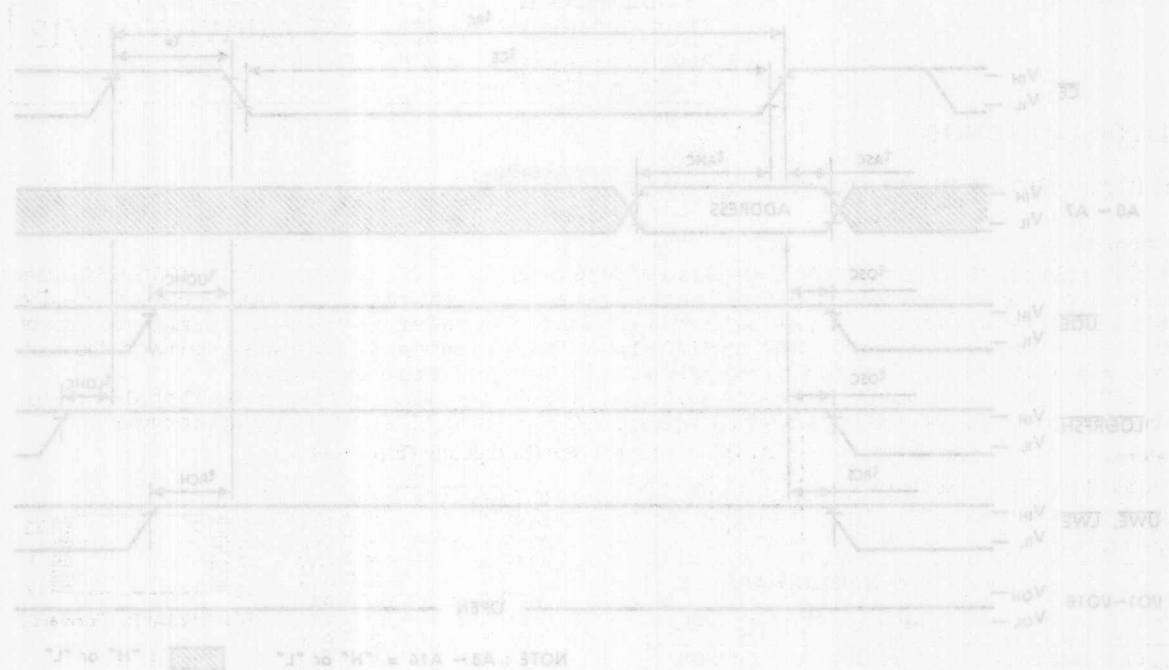
Lower Byte Read Modify Write Cycle



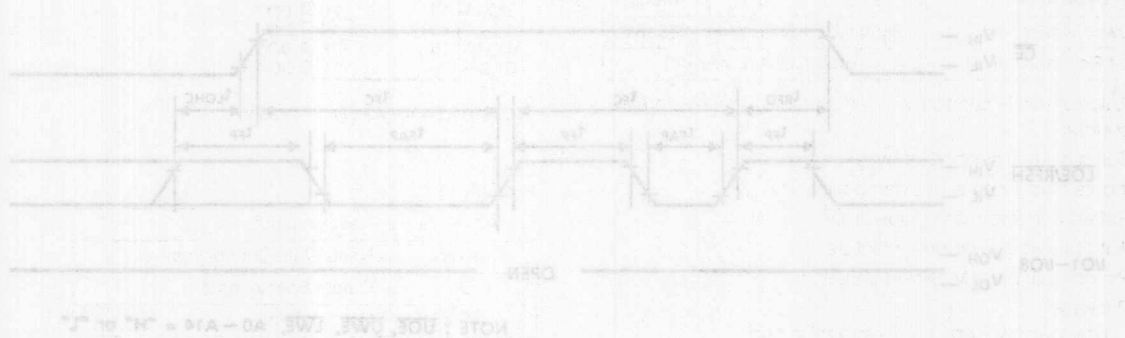
\overline{CE} Only RefreshNOTE : A8 ~ A14 = "H" or "L"  : "H" or "L"**Auto Refresh**NOTE : $\overline{UOE}, \overline{UWE}, \overline{LWE}, A0 \sim A14$ = "H" or "L"**Self Refresh**NOTE : $\overline{UOE}, \overline{UWE}, \overline{LWE}, A0 \sim A14$ = "H" or "L"

Notes

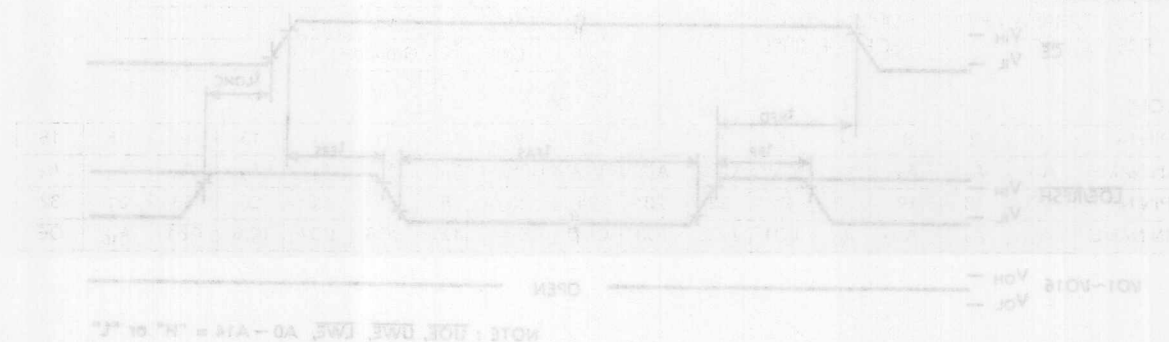
CE Only Refresh



Auto Refresh



Self Refresh



TOSHIBA

TC518128AP/ASP/AF/AFW-80/10/12 TC518128APL/ASPL/AFL/AFWL-80/10/12 TC518128AFTL-80/10/12

SILICON GATE CMOS

131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518128A is a 1M bit high speed CMOS pseudo static RAM organized as 131,072 words by 8 bits. The TC518128A utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518128A operates from a single 5V power supply. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC518128A features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

The TC518128A is pin-compatible with the 1M bit CMOS static RAM JEDEC standard and is available in a 32-pin, 0.6 inch and 0.3 inch width plastic DIP, a small outline plastic flat package, and a 32-pin thin small outline plastic package (forward type).

Features

- Organization: 131,072 words x 8 bits
- Single 5V power supply
- Fast access time

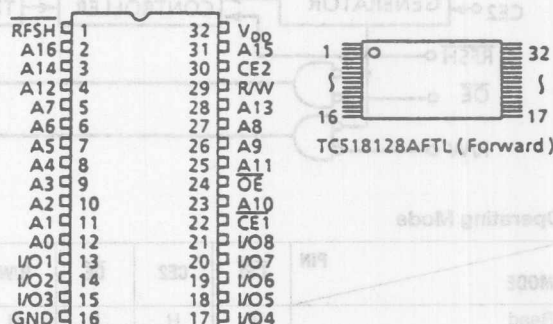
	TC518128A Family		
	-80	-10	-12
t _{CEA} CE Access Time	80ns	100ns	120ns
t _{OE} OE Access Time	35ns	40ns	50ns
t _{RC} Cycle Time	130ns	160ns	190ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	1mA/200μA (L version)		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 512 refresh cycles/8ms
- Auto refresh power down feature
- Pin compatible: 1M SRAM (JEDEC)
- Package
 - TC518128AP/APL : DIP32-P-600
 - TC518128AF/AFL : SOP32-P-450
 - TC518128ASP/ASPL : DIP32-P-300
 - TC518128AFW/AFWL : SOP32-P-525
 - TC518128AFTL : TSOP32-P-0820

(TSOP)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CE2	A ₁₅	V _{DD}	RFSH	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	CE1	A ₁₀	OE

Pin Connection (Top View)



TC518128APL / AFL / ASPL / AFWL

Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
OE	Output Enable Input
RFSH	Refresh Input
CE1, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
V _{DD}	Power
GND	Ground

The block diagram illustrates the internal structure of the 256K16 DRAM. It features a central **MEMORY ARRAY** with dimensions $512 \times 256 \times 8$. Addressing is managed by a **ROW ADDRESS BUFFER (9)** and a **COLUMN ADDRESS BUFFER (8)**, which feed into a **ROW DECODER** and a **COLUMN DECODER** respectively. The row decoder outputs 512 signals to the memory array, while the column decoder outputs 8 signals to the **SENSE AMP. I/O GATE**. Data is transferred between the memory array and the **DATA INPUT BUFFER (8)** and **DATA OUTPUT BUFFER (8)** through this gate. Control logic includes a **CLOCK GENERATOR** (receiving $\overline{CE1}$ and $\overline{CE2}$), a **REFRESH CONTROLLER**, and a **REFRESH TIMER**. The refresh controller is also influenced by \overline{RFSH} and \overline{OE} signals (via an AND gate) and the R/W signal (via an OR gate). The refresh counter (9) provides feedback to the row decoder. The data buffers are connected to the system's $I/O1$ and $I/O8$ lines.

MODE \ PIN	$\overline{CE1}$	CE2	\overline{OE}	R/W	\overline{RFSH}	A0 ~ A16	I/O1 ~ 8
Read	L	H	L	H	*	V*	OUT
Write	L	H	*	L	*	V*	IN
CE only Refresh	L	H	H	H	*	V*	HZ
Auto/Self Refresh	H	*	*	*	L	*	HZ
Auto/Self Refresh	*	L	*	*	L	*	HZ
Standby	H	*	*	*	H	*	HZ
Standby	*	L	*	*	H	*	HZ

HZ = High impedance

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1.0$	V	2
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics (Ta = 0 ~ 70°C, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) CE1, CE2, Address cycling: $t_{RC} = t_{RC \text{ min.}}$	80ns version	—	50	70	mA 3,4
		100ns version	—	40	60	
		120ns version	—	35	50	
I_{DDS1}	Standby Current CE1 = V_{IH} or CE2 = V_{IL} , $\overline{RFSH} = V_{IH}$	Normal version	—	—	2	mA
		L version	—	—	1	
I_{DDS2}	Standby Current CE1 = $V_{DD} - 0.2V$ or CE2 = 0.2V, $\overline{RFSH} = V_{DD} - 0.2V$	Normal version	—	—	1	mA
		L version	—	100	200	
I_{DDF1}	Self Refresh Current (Average) CE1 = V_{IH} or CE2 = V_{IL} , $\overline{RFSH} = V_{IL}$	Normal version	—	—	2	mA
		L version	—	—	1	
I_{DDF2}	Self Refresh Current (Average) CE1 = $V_{DD} - 0.2V$ or CE2 = 0.2V, $\overline{RFSH} = 0.2V$	Normal version	—	—	1	mA
		L version	—	100	200	
I_{DDF3}	Auto Refresh Current (Average) \overline{RFSH} cycling: $t_{FC} = t_{FC \text{ min}}$	—	—	2	mA	
I_{DDF4}	CE only Refresh Current (Average) CE1, CE2, Address cycling: $t_{RC} = t_{RC \text{ min.}}$	80ns version	—	50	70	mA 3
		100ns version	—	40	60	
		120ns version	—	35	50	
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = 0V	—	—	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disabled (CE1 = V_{IH} or CE2 = V_{IL} or $\overline{OE} = V_{IH}$ or $R/W = V_{IL}$), $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level $I_{OH} = -5mA$	2.4	—	—	V	
V_{OL}	Output Low Level $I_{OL} = 4.2mA$	—	—	0.4	V	

Note: For I_{DDS1} and I_{DDF1} with CE1 = V_{IH} (CE2 = V_{IL}), the specified limits are guaranteed under the condition CE2 = V_{IH} or CE2 = V_{IL} .
(CE1 = V_{IH} or CE1 = V_{IL}).
For I_{DDS2} and I_{DDF2} with CE1 $\geq V_{DD} - 0.2V$ (CE2 $\leq 0.2V$), the specified limits are guaranteed under the condition CE2 $\geq V_{DD} - 0.2V$ or CE2 $\leq 0.2V$.
(CE1 $\geq V_{DD} - 0.2V$ or CE1 $\leq 0.2V$).

Capacitance* ($V_{DD} = 5V$, Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	—	5	pF
C_{I2}	Input Capacitance (CE1, CE2, \overline{OE} , R/W, \overline{RFSH})	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	130	—	160	—	190	—		
t _{RMW}	Read Modify Write Cycle Time	195	—	235	—	280	—		
t _{CE}	CE Pulse Width	80	10,000	100	10,000	120	10,000		13
t _p	CE Precharge Time	40	—	50	—	60	—		
t _{CEA}	CE Access Time	—	80	—	100	—	120		
t _{OEA}	OE Access Time	—	35	—	40	—	50		
t _{CLZ}	CE to Output in Low -Z	30	—	30	—	30	—		
t _{OLZ}	OE to Output in Low -Z	0	—	0	—	0	—		
t _{WLZ}	Output Active from End of Write	0	—	0	—	0	—		
t _{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35		9
t _{OHZ}	OE Disable to Output in High-Z	0	25	0	30	0	35		9
t _{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35		9
t _{ODS}	OE Output Disable Setup Time	0	—	0	—	0	—		
t _{ODH}	OE Output Disable Hold Time	10	—	10	—	10	—		
t _{RCS}	Read Command Setup Time	0	—	0	—	0	—		
t _{RCH}	Read Command Hold Time	0	—	0	—	0	—		
t _{WP}	Write Pulse Width	60	—	70	—	85	—	ns	
t _{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000		
t _{CWL}	Write Command to CE Lead Time	60	10,000	70	10,000	85	10,000		
t _{DSW}	Data Setup Time from R/W	30	—	35	—	45	—		10
t _{DSC}	Data Setup Time from CE	30	—	35	—	45	—		10
t _{DHW}	Data Hold Time from R/W	0	—	0	—	0	—		10
t _{DHC}	Data Hold Time from CE	0	—	0	—	0	—		10
t _{ASC}	Address Setup Time	0	—	0	—	0	—		11
t _{AHC}	Address Hold Time	20	—	25	—	30	—		11
t _{RHC}	RFSH Command Hold Time	15	—	15	—	15	—		
t _{FC}	Auto Refresh Cycle Time	130	—	160	—	190	—		
t _{RFD}	RFSH Delay Time from CE	40	—	50	—	60	—		
t _{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000		12
t _{FP}	RFSH Precharge Time	30	—	30	—	30	—		12
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—		12
t _{FRS}	CE Delay Time from RFSH (Self Refresh)	160	—	190	—	225	—		12
t _{REF}	Refresh Period (512 cycles, A0 ~ A8)	—	8	—	8	—	8	ms	
t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	
t _{CES}	CE2 Low Setup Time	5	—	5	—	5	—	ns	14
t _{CEH}	CE2 Low Hold Time	5	—	5	—	5	—	ns	14

Notes:

- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DDO} and I_{DDF4} depend on the cycle time.
- 4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high $\overline{CE1}$ or low CE2 is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

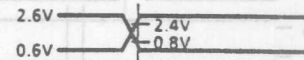
7) Timing reference levels

Input Levels

$$: V_{IH} = 2.6V$$

$$V_{IL} = 0.6V$$

INPUT



Input Reference Levels

$$: V_{IH} = 2.4V$$

$$V_{IL} = 0.8V$$

OUTPUT



Output Reference Levels

$$: V_{OH} = 2.2V$$

$$V_{OL} = 0.8V$$

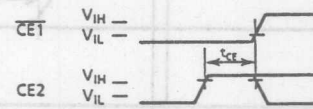
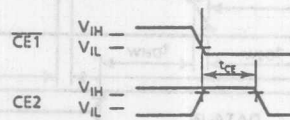
INPUT REFERENCE
LEVELOUTPUT REFERENCE
LEVEL

- 8) Measured with a load equivalent to 2 TTL loads and 100pF.
- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) For write cycles, the input data is latched at the earlier of R/W or $\overline{CE1}$ rising edge (CE2 falling edge). Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 11) All address inputs are latched at the falling edge of $\overline{CE1}$ (rising edge of CE2). Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
- 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$.
 - Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 - Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

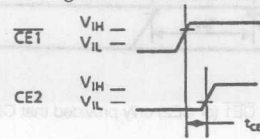
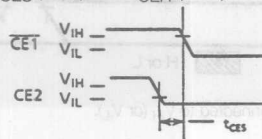
The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

- after self refresh
- if $\overline{RFSH} = "L"$ after power-up

- 13) The timings, t_{CE} (min.) and t_{CE} (max.) must be met for proper device operation.

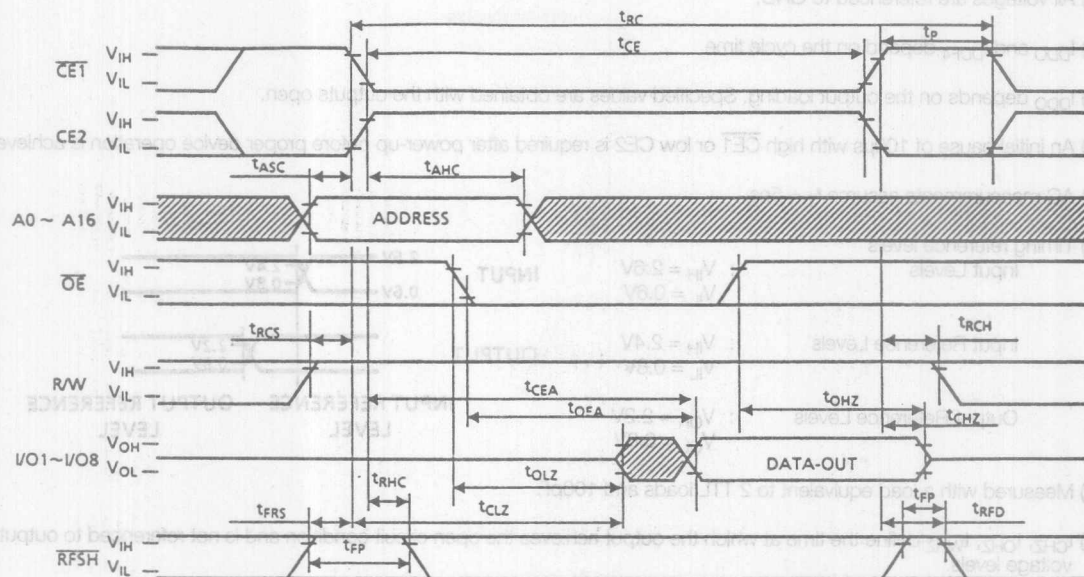
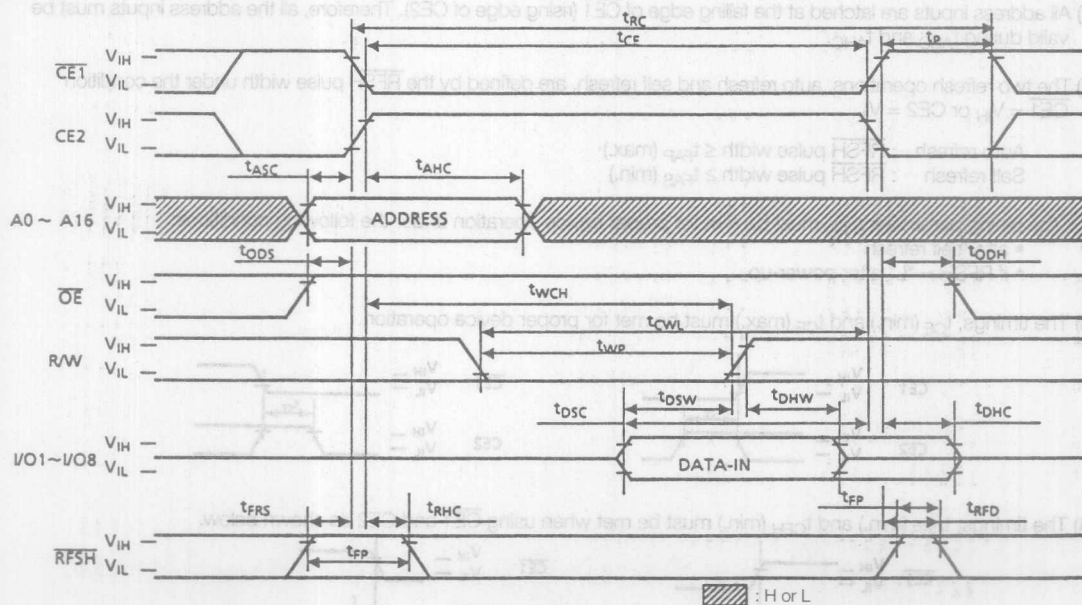


- 14) The timings, t_{CES} (min.) and t_{CEH} (min.) must be met when using $\overline{CE1}$ and CE2 as shown below.

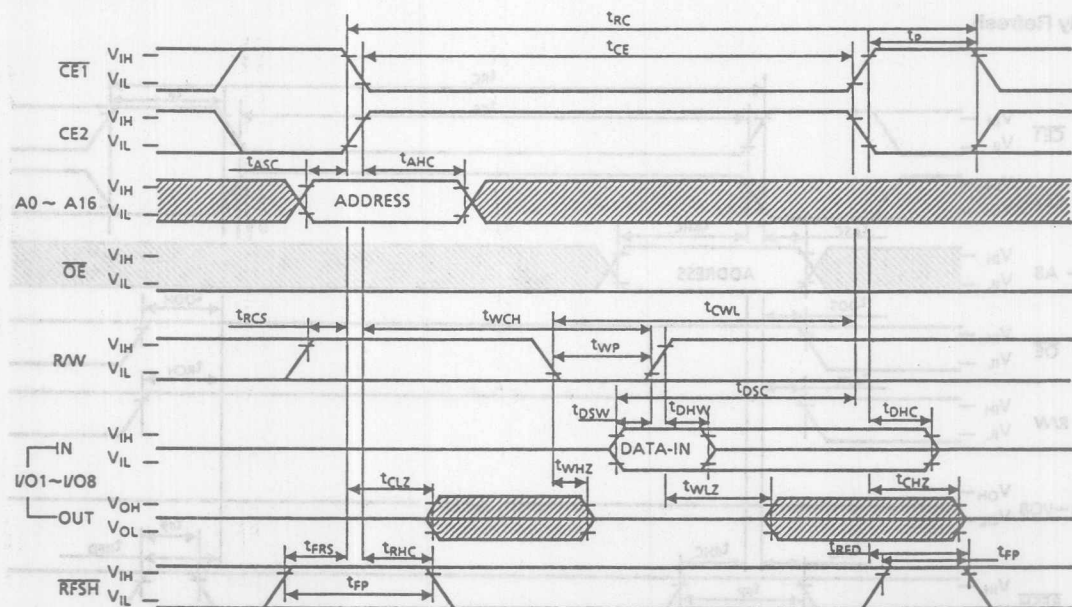
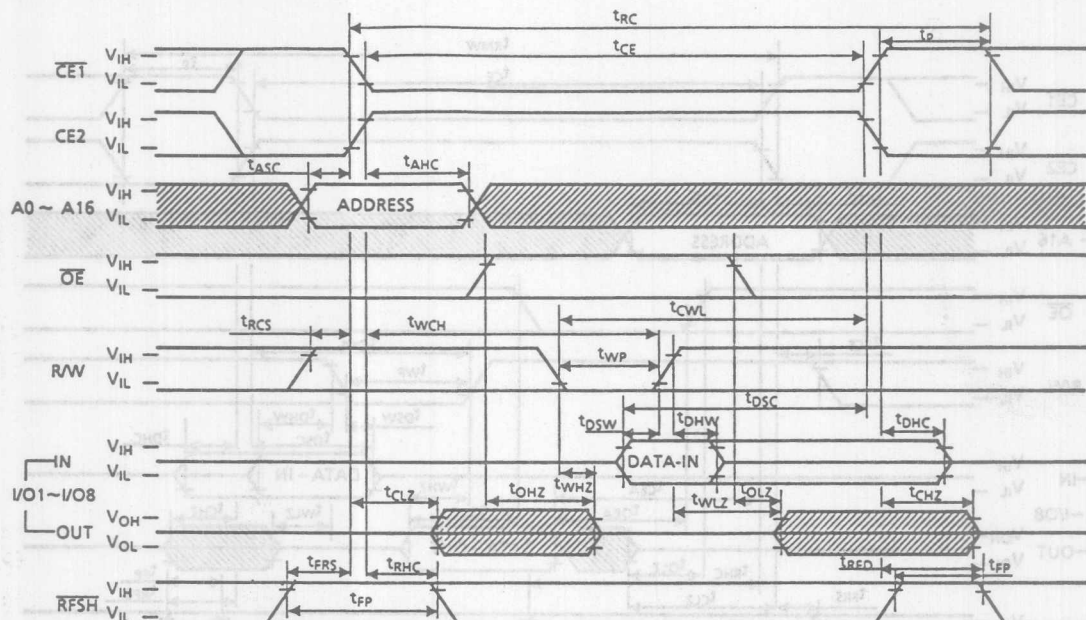


Timing Waveforms

Read Cycle

Write Cycle 1 (\overline{OE} Fixed High)

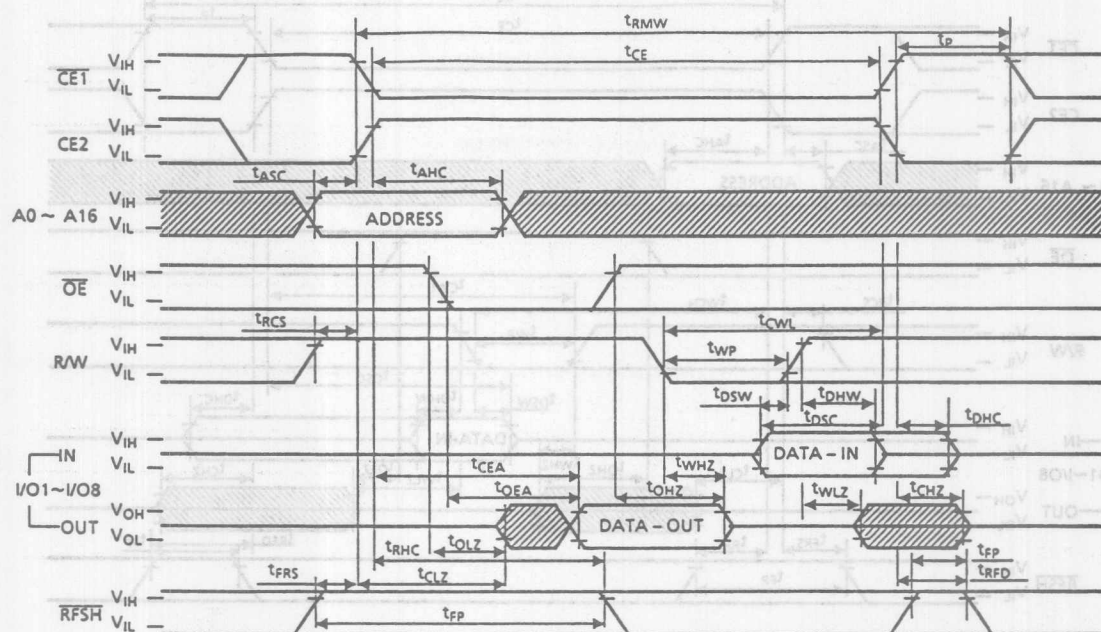
Note: The device can be operated by cycling $\overline{CE1}$ (or $\overline{CE2}$) only provided that $\overline{CE2}$ (or $\overline{CE1}$) is connected to V_{IH} (or V_{IL}).



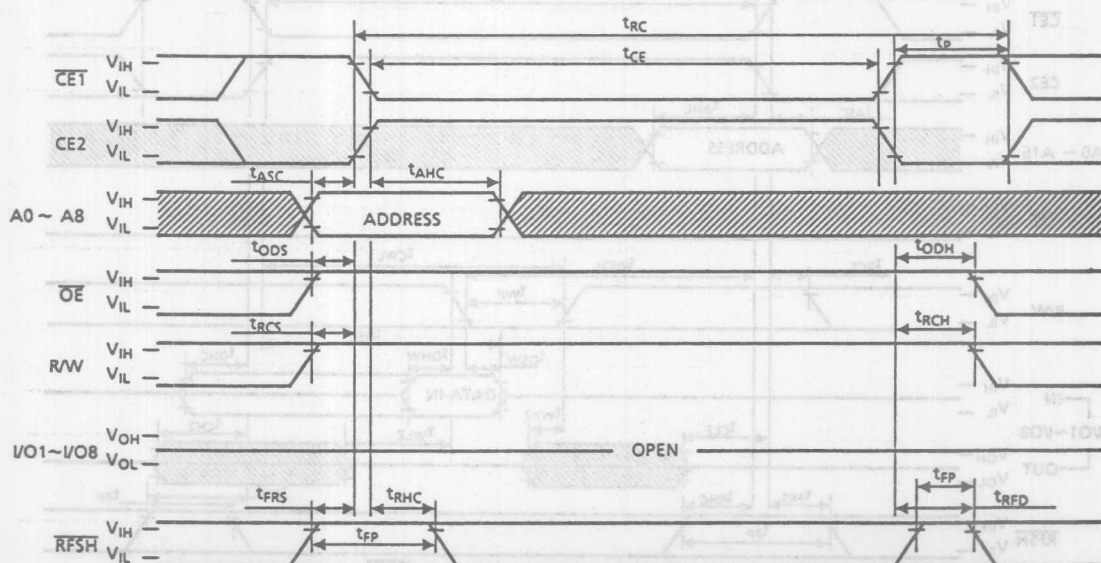
 : H or L

Note: The device can be operated by cycling $\overline{\text{CE1}}$ (or CE2) only provided that CE2 (or $\overline{\text{CE1}}$) is connected to V_{IH} (or V_{IL}).

Read Modify Write Cycle



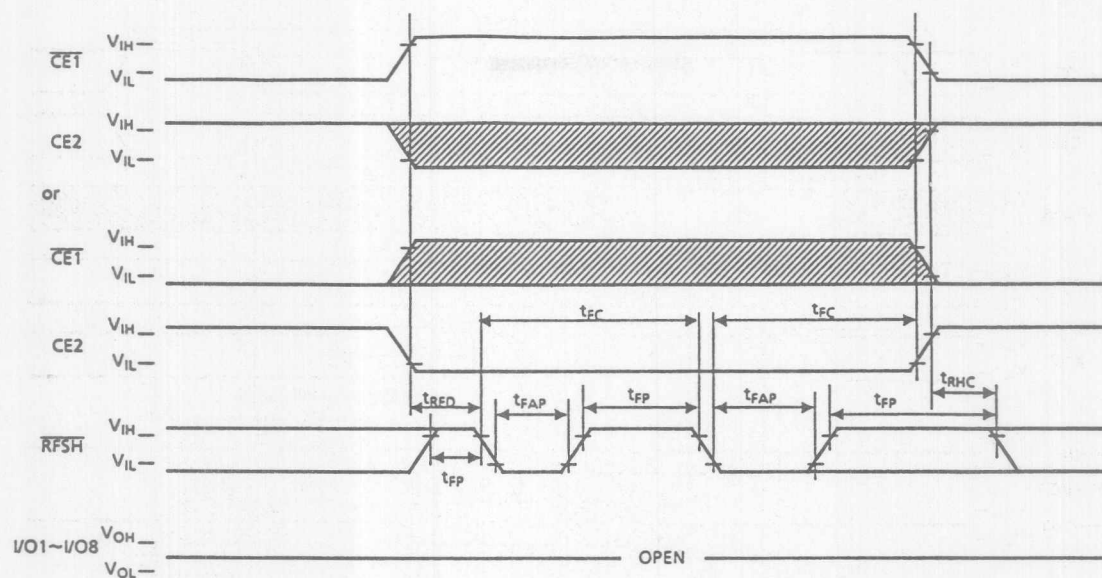
CE Only Refresh

Note : A9 ~ A16 = V_{IH} or V_{IL}

: H or L

Note: The device can be operated by cycling $\overline{CE1}$ (or $\overline{CE2}$) only provided that $\overline{CE2}$ (or $\overline{CE1}$) is connected to V_{IH} (or V_{IL}).

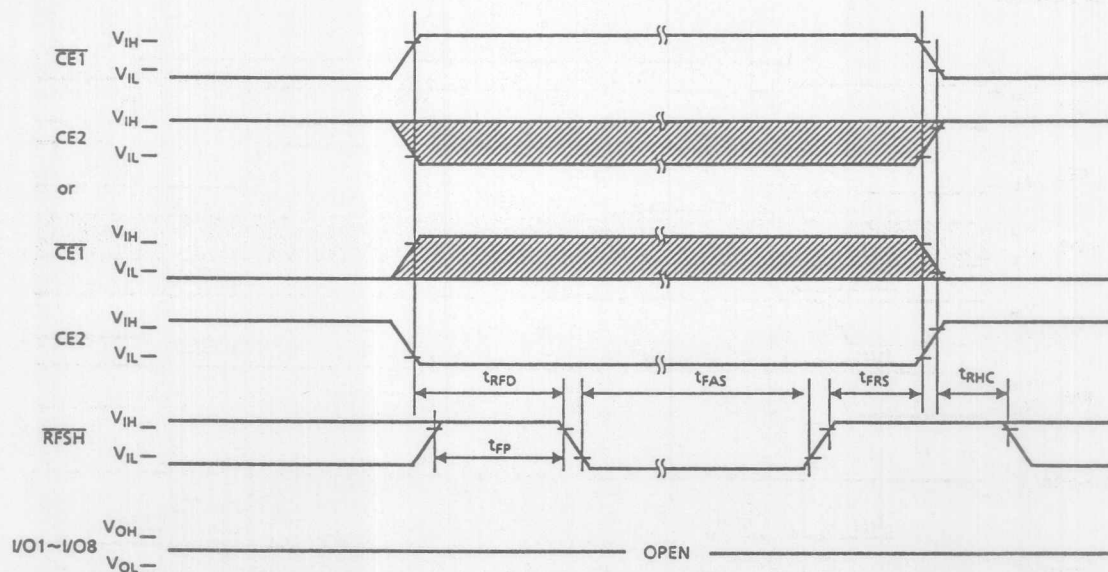
Auto Refresh



Note : \overline{OE} , R/W , $A0 \sim A16 = V_{IH}$ or V_{IL}

▨ : H or L

Self Refresh



Note : \overline{OE} , R/W , $A0 \sim A16 = V_{IH}$ or V_{IL}

▨ : H or L

TC518128APL/AFL/AFWL-80LV/10LV/12LV TC518128AFTL-80LV/10LV/12LV

SILICON GATE CMOS

131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518128A-LV is a 1M bit high speed CMOS pseudo static RAM organized as 131,072 words by 8 bits. The TC518128A-LV utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518128A-LV operates from a single power supply of 3.135 ~ 5.5V. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC518128A-LV features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

The TC518128A is pin-compatible with the 1M bit CMOS static RAM JEDEC standard and is available in a 32-pin, 0.6 inch width plastic DIP, a small outline plastic flat package, and a 32-pin thin small outline plastic package (forward type).

Features

- Organization: 131,072 words x 8 bits
- Low voltage operation: 3.135V ~ 5.5V
- Data retention supply voltage: 3.0V ~ 5.5V
- Fast access time

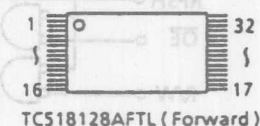
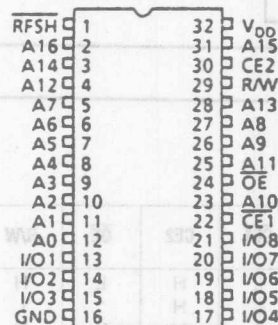
	TC518128A-LV Family		
	-80	-10	-12
t _{CEA} CE Access Time	80ns	100ns	120ns
t _{OEa} OE Access Time	35ns	40ns	50ns
t _{RC} Cycle Time	130ns	160ns	190ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	5.5V	200µA	
	3.0V	100µA	

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 512 refresh cycles/8ms
- Auto refresh power down feature
- Pin compatible: 1M SRAM (JEDEC)
- Package
 - TC518128APL: DIP32-P-600
 - TC518128AFL: SOP32-P-450
 - TC518128AFWL: SOP32-P-525
 - TC518128AFTL: TSOP32-P-0820

(TSOP)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CE2	A ₁₅	V _{DD}	RFSH	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	CE1	A ₁₀	OE

Pin Connection (Top View)

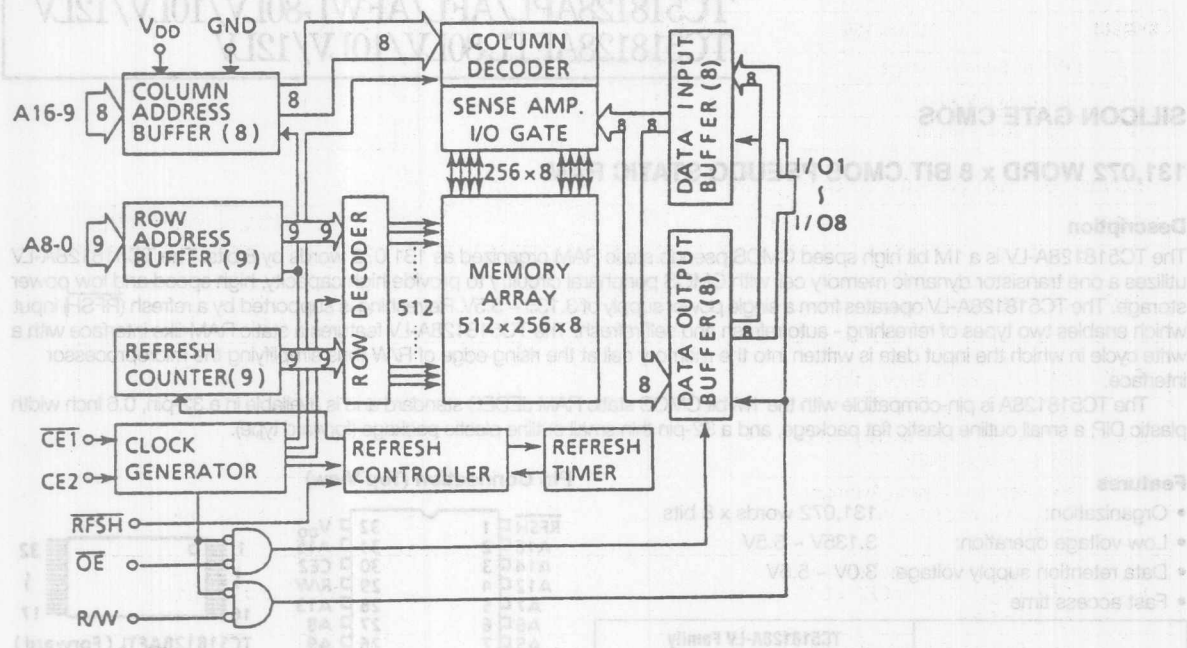


TC518128APL/AFL/AFWL

Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
OE	Output Enable Input
RFSH	Refresh Input
CE1, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
V _{DD}	Power
GND	Ground

Block Diagram



Operating Mode

MODE	PIN	$\overline{CE1}$	CE2	\overline{OE}	R/W	\overline{RFSH}	A0 ~ A16	I/O1 ~ 8
Read		L	H	L	H	*	V*	OUT
Write		L	H	*	L	*	V*	IN
CE only Refresh		L	H	H	H	*	V*	HZ
Auto/Self Refresh		H	*	*	*	L	*	HZ
Auto/Self Refresh		*	L	*	*	L	*	HZ
Standby		H	*	*	*	H	*	HZ
Standby		*	L	*	*	H	*	HZ

H = High level input (V_{IH})L = Low level input (V_{IL})* = V_{IH} or V_{IL} V* = At the falling edge of $\overline{CE1}$ ($CE2 = H$) or the rising edge of $CE2$ ($\overline{CE1} = L$), all address inputs are latched. At all other times, the address inputs are "**".

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1.0$	V	2
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) $\overline{CE1}$, $\overline{CE2}$, Address cycling: $t_{RC} = t_{RC \text{ min.}}$	80ns version	—	50	70	mA 3,4
		100ns version	—	40	60	
		120ns version	—	35	50	
I_{DDs1}	Standby Current $\overline{CE1} = V_{IH}$ or $\overline{CE2} = V_{IL}$, $\overline{RFSH} = V_{IH}$	—	—	1	mA	
I_{DDs2}	Standby Current $\overline{CE1} = V_{DD} - 0.2V$ or $\overline{CE2} = 0.2V$, $\overline{RFSH} = V_{DD} - 0.2V$	—	100	200	μA	
I_{DDF1}	Self Refresh Current (Average) $\overline{CE1} = V_{IH}$ or $\overline{CE2} = V_{IL}$, $\overline{RFSH} = V_{IL}$	—	—	1	mA	
I_{DDF2}	Self Refresh Current (Average) $\overline{CE1} = V_{DD} - 0.2V$ or $\overline{CE2} = 0.2V$, $\overline{RFSH} = 0.2V$	—	100	200	μA	
I_{DDF3}	Auto Refresh Current (Average) \overline{RFSH} cycling: $t_{FC} = t_{FC \text{ min}}$	—	—	2	mA	
I_{DDF4}	CE only Refresh Current (Average) $\overline{CE1}$, $\overline{CE2}$, Address cycling: $t_{RC} = t_{RC \text{ min.}}$	80ns version	—	50	70	mA 3
		100ns version	—	40	60	
		120ns version	—	35	50	
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = $0V$	—	—	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disabled ($\overline{CE1} = V_{IH}$ or $\overline{CE2} = V_{IL}$ or $\overline{OE} = V_{IH}$ or $R/W = V_{IL}$), $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level $I_{OH} = -5mA$	2.4	—	—	V	
V_{OL}	Output Low Level $I_{OL} = 4.2mA$	—	—	0.4	V	

Note: For I_{DDs1} and I_{DDF1} with $\overline{CE1} = V_{IH}$ ($\overline{CE2} = V_{IL}$), the specified limits are guaranteed under the condition $\overline{CE2} = V_{IH}$ or $\overline{CE2} = V_{IL}$ ($\overline{CE1} = V_{IH}$ or $\overline{CE1} = V_{IL}$).
For I_{DDs2} and I_{DDF2} with $\overline{CE1} \geq V_{DD} - 0.2V$ ($\overline{CE2} \leq 0.2V$), the specified limits are guaranteed under the condition $\overline{CE2} \geq V_{DD} - 0.2V$ or $\overline{CE2} \leq 0.2V$ ($\overline{CE1} \geq V_{DD} - 0.2V$ or $\overline{CE1} \leq 0.2V$).

Capacitance* ($V_{DD} = 5V$, $T_a = 25^\circ\text{C}$, $f = 1MHz$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	—	5	pF
C_{I2}	Input Capacitance ($\overline{CE1}$, $\overline{CE2}$, \overline{OE} , R/W , \overline{RFSH})	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	130	—	160	—	190	—		
t_{RMW}	Read Modify Write Cycle Time	195	—	235	—	280	—		
t_{CE}	CE Pulse Width	80	10,000	100	10,000	120	10,000		13
t_P	CE Precharge Time	40	—	50	—	60	—		
t_{CEA}	CE Access Time	—	80	—	100	—	120		
t_{OEA}	\overline{OE} Access Time	—	35	—	40	—	50		
t_{CLZ}	CE to Output in Low -Z	30	—	30	—	30	—		
t_{OLZ}	\overline{OE} to Output in Low -Z	0	—	0	—	0	—		
t_{WLZ}	Output Active from End of Write	0	—	0	—	0	—		
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35		9
t_{OHZ}	\overline{OE} Disable to Output in High-Z	0	25	0	30	0	35		9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35		9
t_{ODS}	\overline{OE} Output Disable Setup Time	0	—	0	—	0	—		
t_{ODH}	\overline{OE} Output Disable Hold Time	10	—	10	—	10	—		
t_{RCS}	Read Command Setup Time	0	—	0	—	0	—		
t_{RCH}	Read Command Hold Time	0	—	0	—	0	—		
t_{WP}	Write Pulse Width	60	—	70	—	85	—	ns	
t_{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000		
t_{CWL}	Write Command to CE Lead Time	60	10,000	70	10,000	85	10,000		
t_{DSW}	Data Setup Time from R/W	30	—	35	—	45	—		10
t_{DSC}	Data Setup Time from CE	30	—	35	—	45	—		10
t_{DHW}	Data Hold Time from R/W	0	—	0	—	0	—		10
t_{DHC}	Data Hold Time from CE	0	—	0	—	0	—		10
t_{ASC}	Address Setup Time	0	—	0	—	0	—		11
t_{AHC}	Address Hold Time	20	—	25	—	30	—		11
t_{RHC}	RFSH Command Hold Time	15	—	15	—	15	—		
t_{FC}	Auto Refresh Cycle Time	130	—	160	—	190	—		
t_{RFD}	RFSH Delay Time from CE	40	—	50	—	60	—		
t_{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000		12
t_{FP}	RFSH Precharge Time	30	—	30	—	30	—		12
t_{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—		12
t_{FRS}	CE Delay Time from RFSH (Self Refresh)	160	—	190	—	225	—		12
t_{REF}	Refresh Period (512 cycles, A0 ~ A8)	—	8	—	8	—	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50		
t_{CES}	CE2 Low Setup Time	5	—	5	—	5	—	ns	14
t_{CEH}	CE2 Low Hold Time	5	—	5	—	5	—		14

3.3V Operation

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	3.135	3.3	3.465	V	2
V_{IH}	Input High Voltage	$V_{DD} - 0.2V$	—	$V_{DD} + 1.0V$	V	
V_{IL}	Input Low Voltage	-0.5	—	0.2	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 3.3V \pm 5\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) CE1, CE2, Address cycling: $t_{RC} = t_{RC} \text{ min.}$	—	15	20	mA	3,4
I_{DDS2}	Standby Current	—	50	100	μA	
I_{DDF2}	Self Refresh Current (Average)	—	50	100	μA	
I_{DDF3}	Auto Refresh Current (Average) RFSH cycling: $t_{FC} = t_{FC} \text{ min.}$	—	—	2	mA	
I_{DDF4}	CE only Refresh Current (Average) CE1, CE2, Address cycling: $t_{RC} = t_{RC} \text{ min.}$	—	15	20	mA	3
I_{IL}	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = $0V$	—	—	± 10	μA	
I_{OL}	Output Leakage Current Output Disable, $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level	$I_{OH} = -1\text{mA}$	2.4	—	V	
		$I_{OH} = -100\mu\text{A}$	$V_{DD} - 0.2V$	—		
V_{OL}	Output Low Level	$I_{OL} = 2.1\text{mA}$	—	0.4	V	
		$I_{OL} = 100\mu\text{A}$	—	0.2		

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 3.3V±5%) (Notes: 5, 6, 8)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t _{RC}	Random Read, Write Cycle Time	300	—	—	
t _{RMW}	Read Modify Write Cycle Time	405	—	—	
t _{CE}	CE Pulse Width	200	10,000	—	13
t _p	CE Precharge Time	90	—	—	
t _{CEA}	CE Access Time	—	200	—	
t _{OEa}	\overline{OE} Access Time	—	80	—	
t _{CLZ}	CE to Output in Low -Z	40	—	—	
t _{OLZ}	\overline{OE} to Output in Low -Z	5	—	—	
t _{WLZ}	Output Active from End of Write	5	—	—	
t _{CHZ}	Chip Disable to Output in High-Z	0	50	—	9
t _{OHZ}	\overline{OE} Disable to Output in High-Z	0	50	—	9
t _{WHZ}	Write Enable to Output in High-Z	0	50	—	9
t _{ODS}	\overline{OE} Output Disable Setup Time	0	—	—	
t _{ODH}	\overline{OE} Output Disable Hold Time	10	—	—	
t _{RCS}	Read Command Setup Time	0	—	—	
t _{RCH}	Read Command Hold Time	0	—	ns	
t _{WP}	Write Pulse Width	100	—	—	
t _{WCH}	Write Command Hold Time	100	10,000	—	
t _{CWL}	Write Command to CE Lead Time	100	10,000	—	
t _{DSW}	Data Setup Time from R/W	50	—	—	10
t _{DSC}	Data Setup Time from CE	50	—	—	10
t _{DHW}	Data Hold Time from R/W	0	—	—	10
t _{DHC}	Data Hold Time from CE	0	—	—	10
t _{ASC}	Address Setup Time	0	—	—	11
t _{AHC}	Address Hold Time	35	—	—	11
t _{RHC}	RFSH Command Hold Time	15	—	—	
t _{FC}	Auto Refresh Cycle Time	300	—	—	
t _{RFD}	RFSH Delay Time from CE	90	—	—	
t _{FAP}	RFSH Pulse Width (Auto Refresh)	50	8,000	—	12
t _{FP}	RFSH Precharge Time	50	—	—	12
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	—	12
t _{FRS}	CE Delay Time from RFSH (Self Refresh)	300	—	—	12
t _{REF}	Refresh Period (512 cycles, A0 ~ A8)	—	8	ms	
t _T	Transition Time (Rise and Fall)	3	50	—	
t _{CES}	CE2 Low Setup Time	10	—	ns	14
t _{CEH}	CE2 Low Hold Time	10	—	—	14

Timing Reference Levels:

Input Reference Levels: 1.5V/1.5V

Output Reference Levels: 1.5V/1.5V

Notes:

- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DDO} and I_{DDF4} depend on the cycle time.
- 4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high $\overline{CE1}$ or low CE2 is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

7) Timing reference levels

Input Levels

$$\begin{aligned} &: V_{IH} = 2.6V \\ &V_{IL} = 0.6V \end{aligned}$$

Input Reference Levels

$$\begin{aligned} &: V_{IH} = 2.4V \\ &V_{IL} = 0.8V \end{aligned}$$

Output Reference Levels

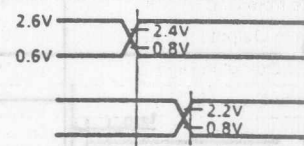
$$\begin{aligned} &: V_{OH} = 2.2V \\ &V_{OL} = 0.8V \end{aligned}$$

INPUT

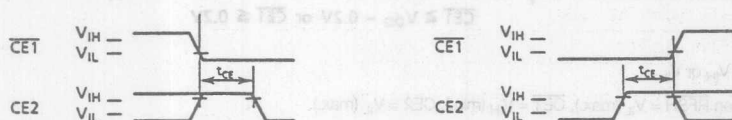
OUTPUT

INPUT REFERENCE LEVEL

OUTPUT REFERENCE LEVEL



- 8) Measured with a load equivalent to 2 TTL loads and 100pF.
 - 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 - 10) For write cycles, the input data is latched at the earlier of R/W or $\overline{CE1}$ rising edge (CE2 falling edge). Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
 - 11) All address inputs are latched at the falling edge of $\overline{CE1}$ (rising edge of CE2). Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
 - 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$.
 - Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 - Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)
- The timing parameter t_{FRS} must be met for proper device operation under the following conditions:
- after self refresh
 - if $\overline{RFSH} = "L"$ after power-up
- 13) The timings, t_{CE} (min.) and t_{CE} (max.) must be met for proper device operation.



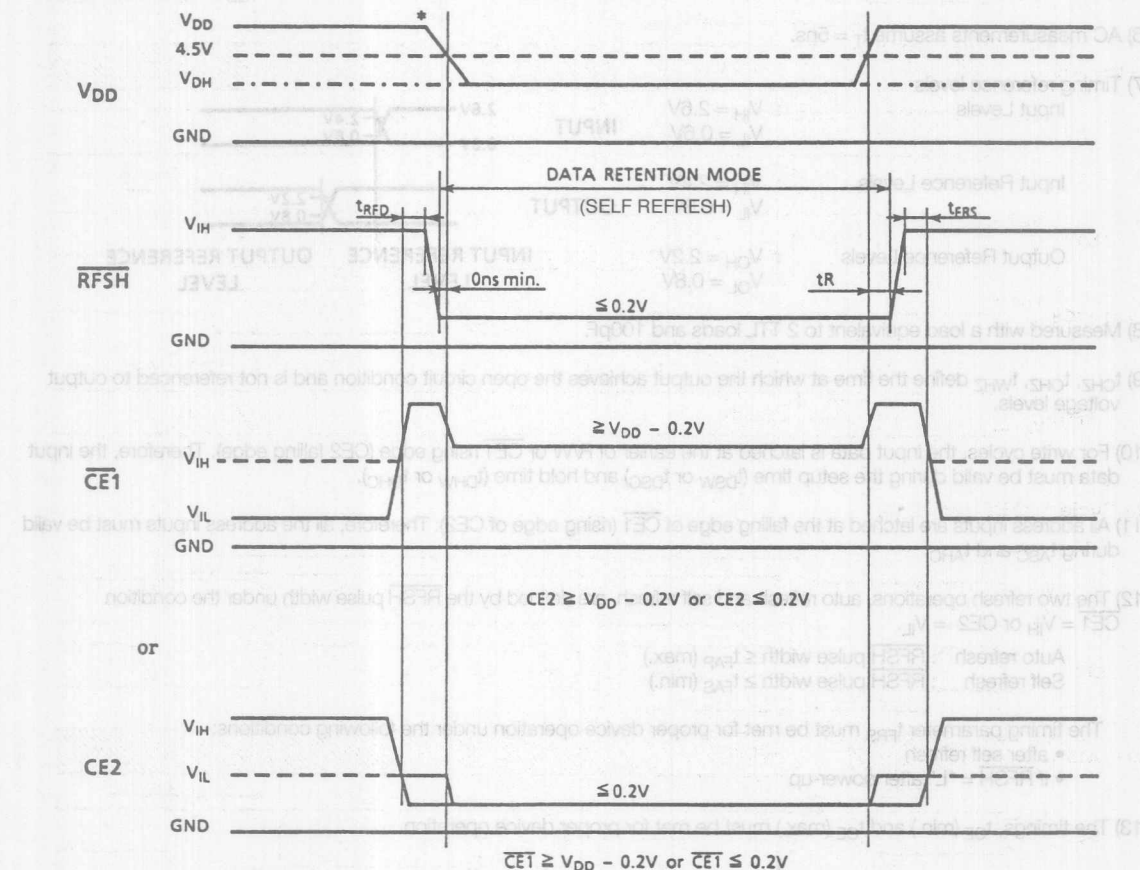
- 14) The timings, t_{CES} (min.) and t_{CEH} (min.) must be met when using $\overline{CE1}$ and CE2 as shown below.



Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	3.0	—	5.5	V
I_{DDF2}	Self Refresh Current	$V_{DH} = 3.0V$	—	40	μA
		$V_{DH} = 5.5V$	—	100	
t_R	Recovery Time	5	—	—	ms

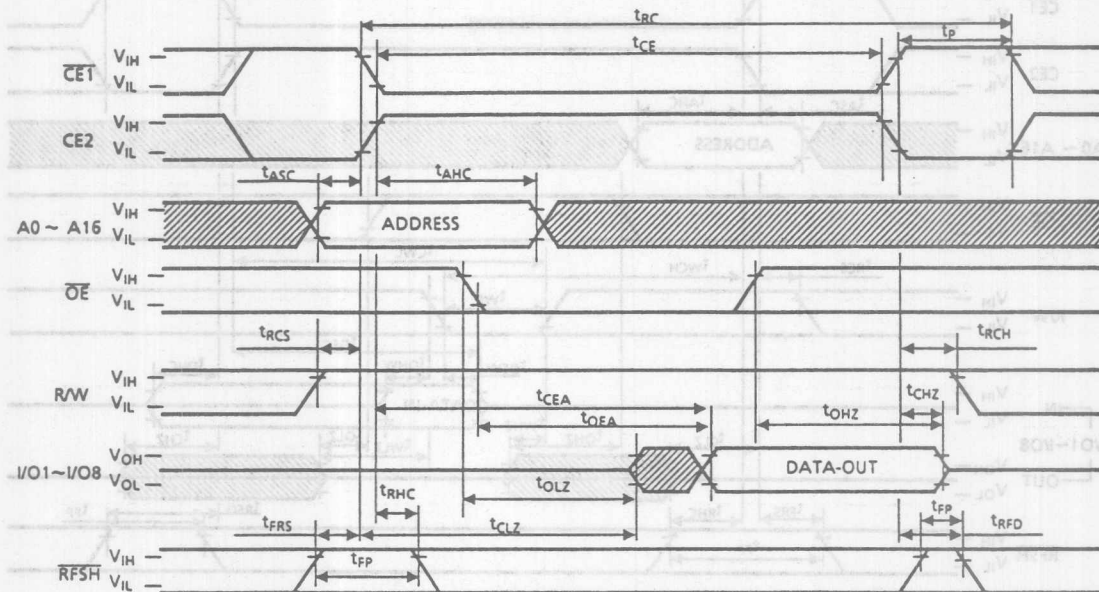
*The falling slope of V_{DD} must be more than 50ms for proper device operation (20ms/V).



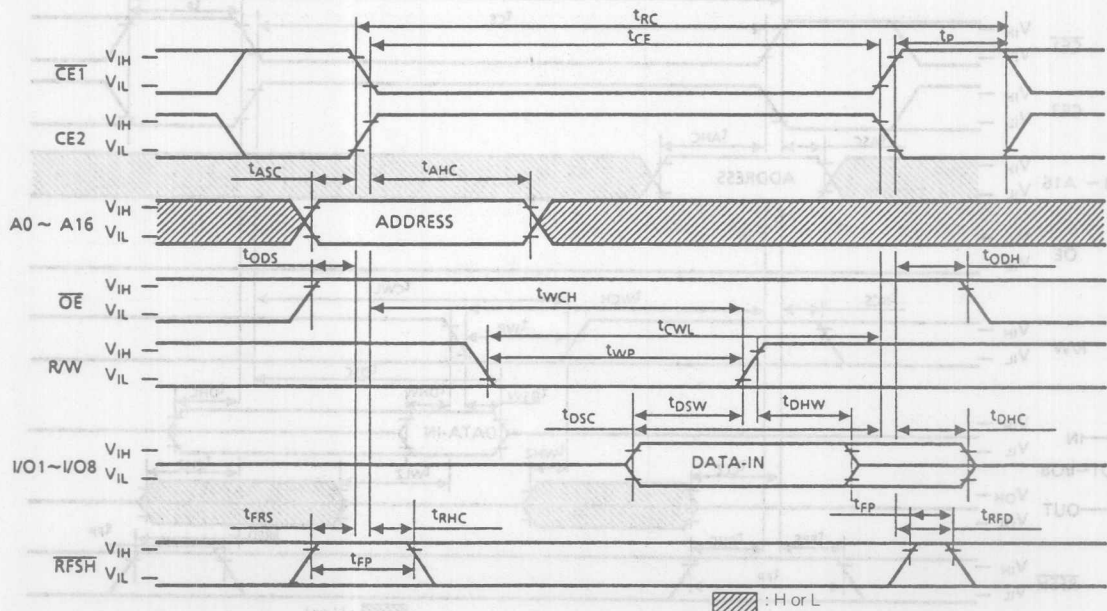
Notes: \overline{OE} , RW , $A0 \sim A16 = V_{IH}$ or V_{IL} .
 I_{DDF1} is applicable when $RFSH = V_{IL}$ (max.), $\overline{CE1} = V_{IH}$ (min.), $CE2 = V_{IL}$ (max.).

Timing Waveforms

Read Cycle

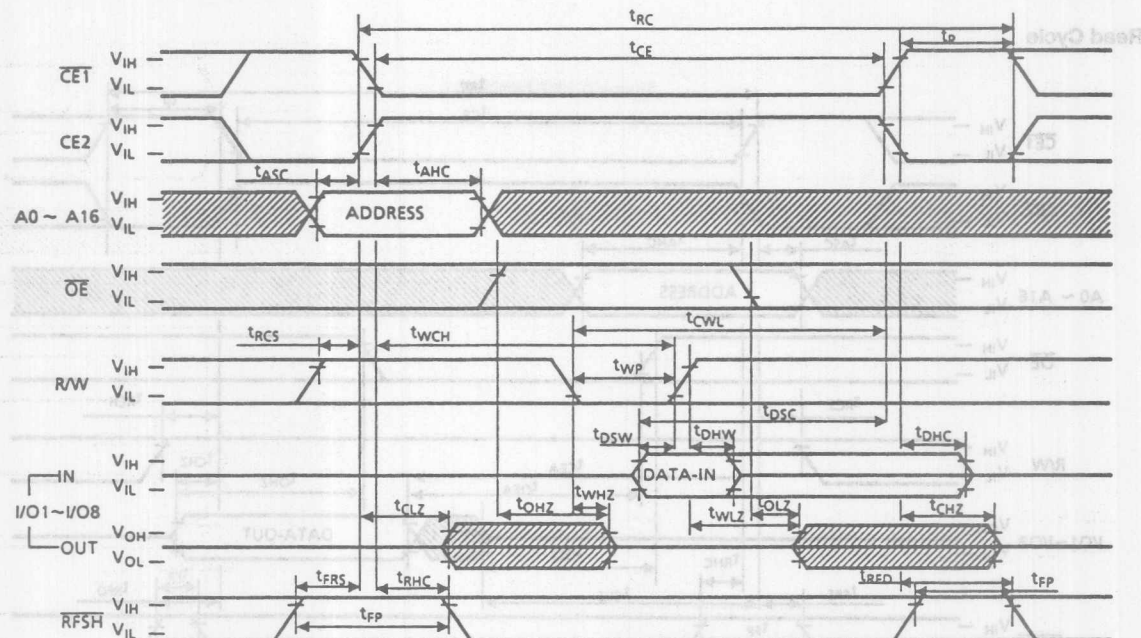


Write Cycle 1 (\overline{OE} Fixed High)

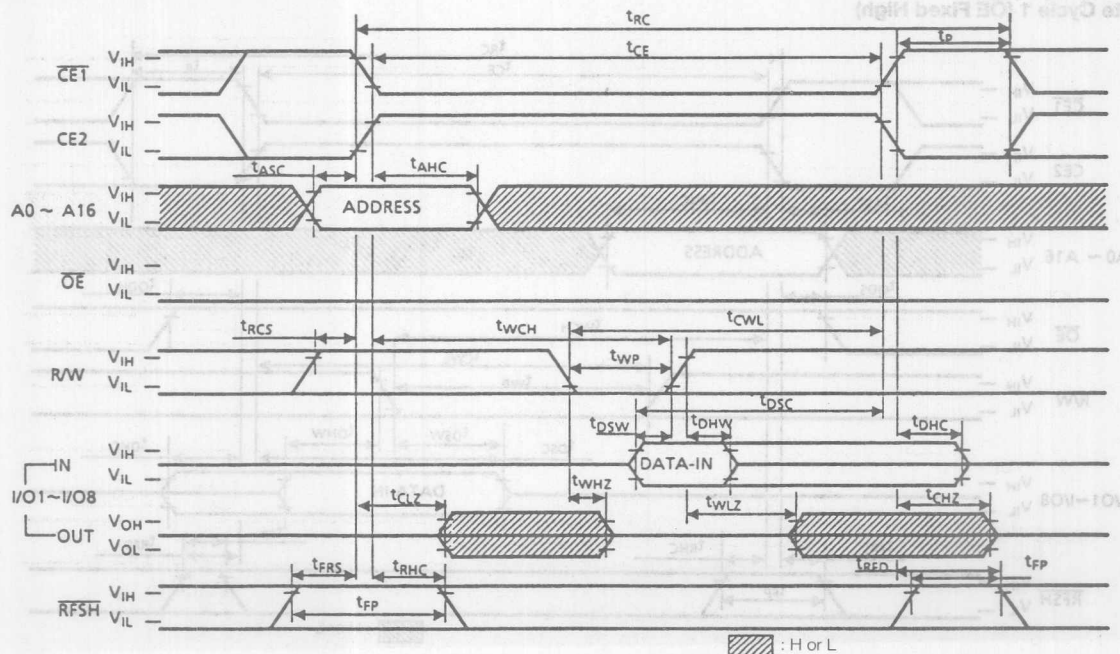


Note: The device can be operated by cycling $\overline{CE1}$ (or $\overline{CE2}$) only provided that $\overline{CE2}$ (or $\overline{CE1}$) is connected to V_{IH} (or V_{IL}).

Write Cycle 2 (\overline{OE} Clocked)



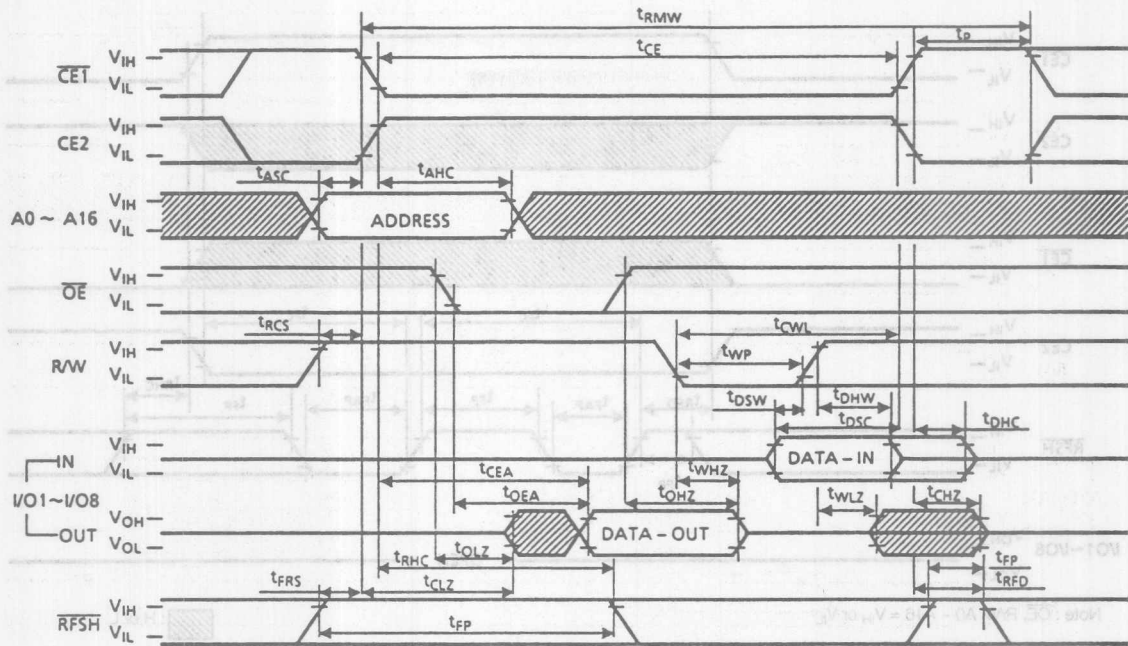
Write Cycle 3 (\overline{OE} Fixed Low)



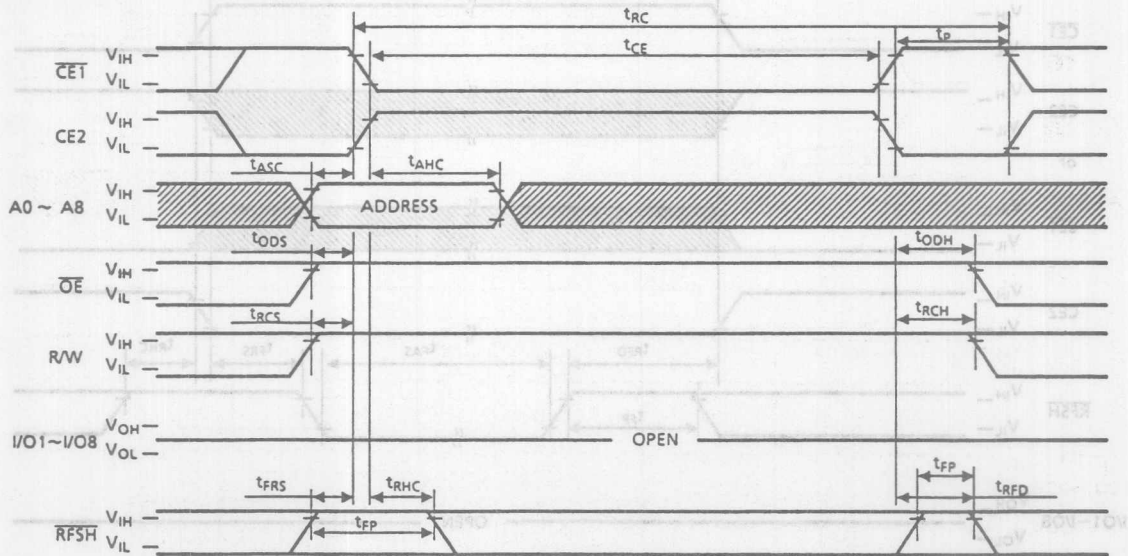
■ : H or L

Note: The device can be operated by cycling $\overline{CE1}$ (or $\overline{CE2}$) only provided that $\overline{CE2}$ (or $\overline{CE1}$) is connected to V_{IH} (or V_{IL}).

Read Modify Write Cycle



CE Only Refresh

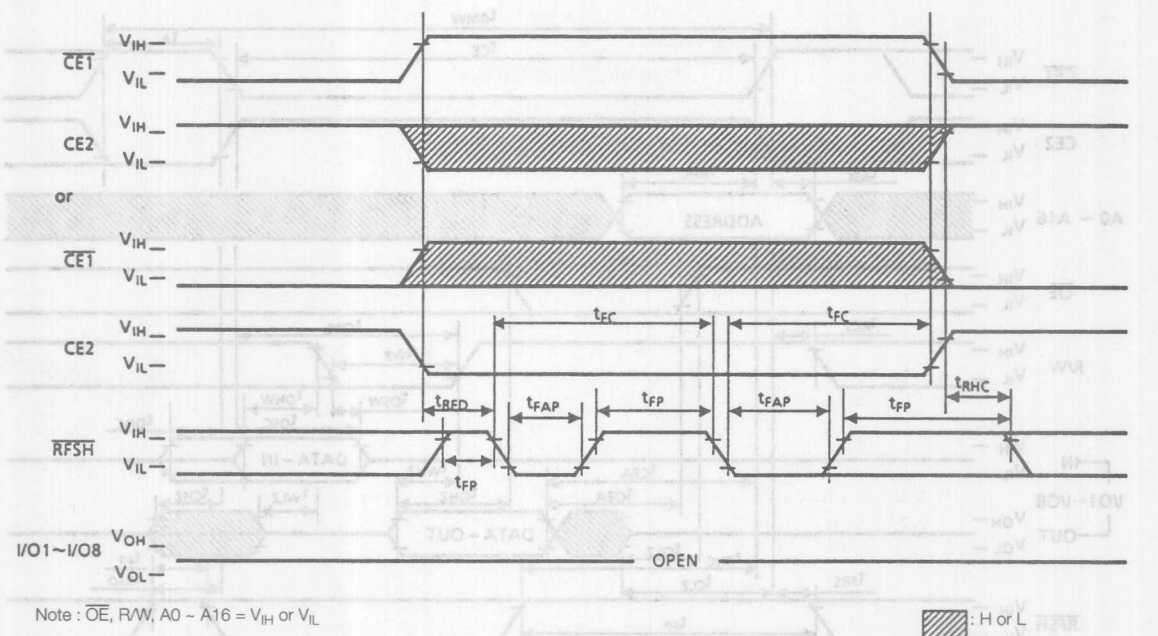


Note : A9 ~ A16 = V_{IH} or V_{IL}

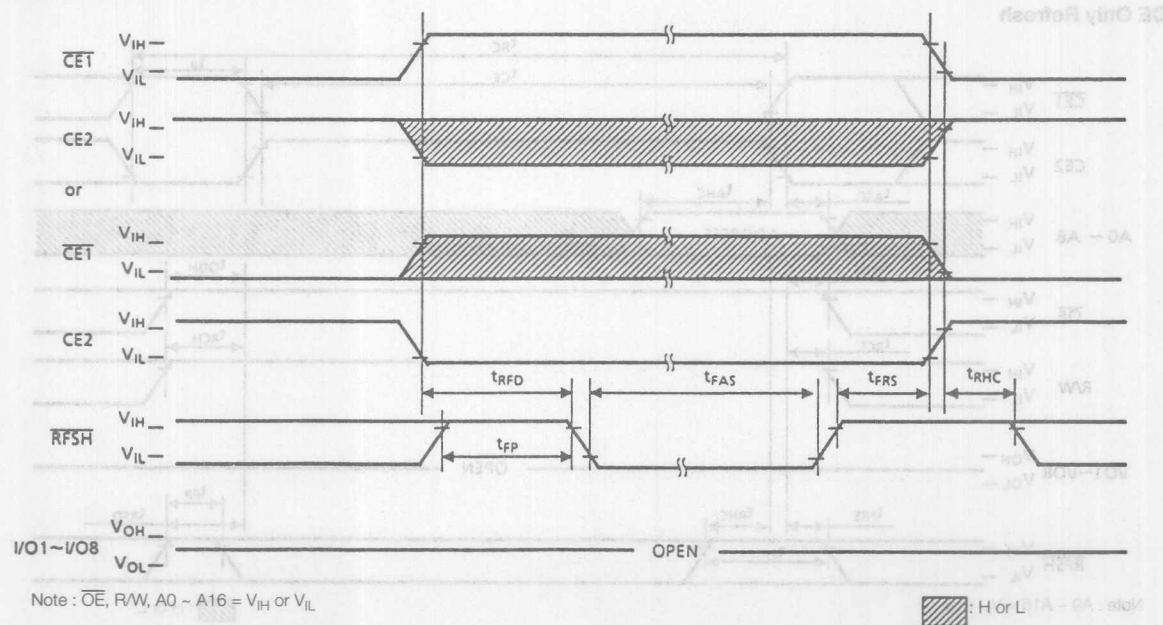
▨ : H or L

Note: The device can be operated by cycling $\overline{CE1}$ (or CE2) only provided that CE2 (or $\overline{CE1}$) is connected to V_{IH} (or V_{IL}).

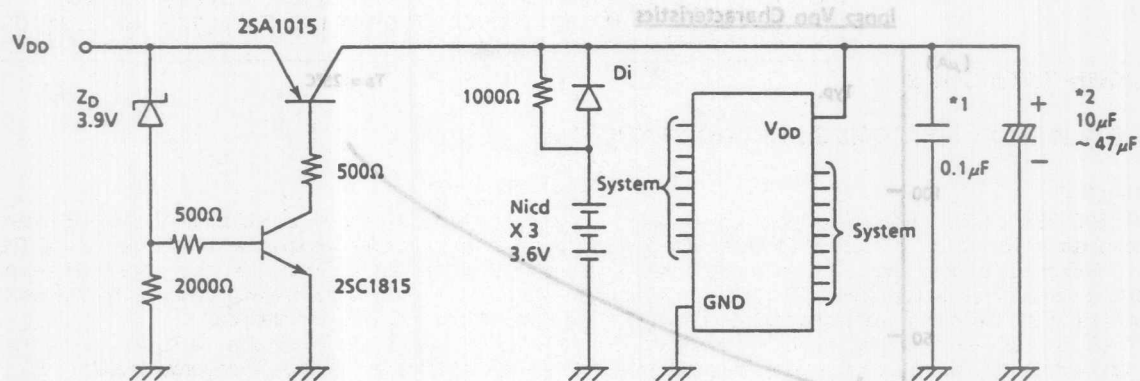
Auto Refresh



Self Refresh



Battery Backup Application Example

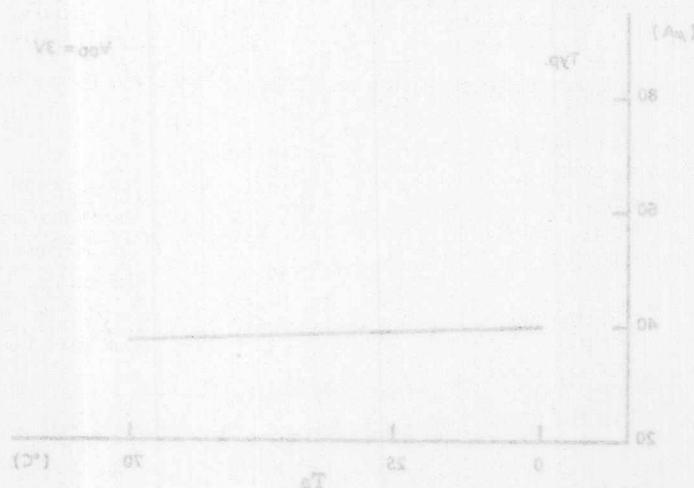


*1: Ceramic condenser

*2: Tantalum condenser

(A large bypass condenser is preferable to absorb noise when the power supply is switched.)

This circuit does not have memory protection. Therefore, rapid turnoff of the power supply must be avoided. Enter the Self Refresh mode before changing to the battery backup power supply.



TC518128BPL/BSPL/BFL/BFWL/BFTL-70/80/10 TC518128BPL/BSPL/BFL/BFWL/BFTL-70L/80L/10L

SILICON GATE CMOS

131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518128B is a 1M bit high speed CMOS pseudo static RAM organized as 131,072 words by 8 bits. The TC518128B utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518128B operates from a single 5V power supply. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC518128B features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

The TC518128B is pin-compatible with the 1M bit CMOS static RAM JEDEC standard and is available in a 32-pin, 0.6 inch and 0.3 inch width plastic DIP, a small outline plastic flat package, and a 32-pin thin small outline plastic package (forward type).

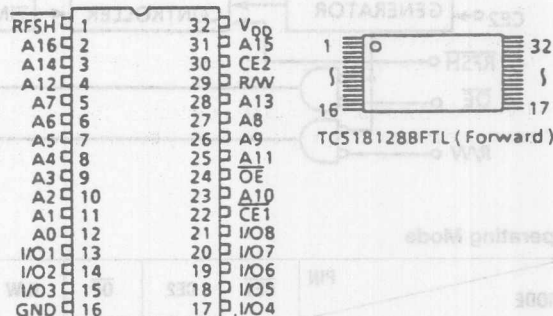
Features

- Organization: 131,072 words x 8 bits
- Single 5V power supply
- Fast access time

	TC518128B Family		
	-70	-80	-10
t _{CEA} CE Access Time	70ns	80ns	100ns
t _{OE} OE Access Time	25ns	30ns	40ns
t _{RC} Cycle Time	115ns	130ns	160ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	200µA (L version) 50µA (LL version)		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 512 refresh cycles/8ms
- Auto refresh power down feature
- Pin compatible: 1M SRAM (JEDEC)
- Package
 - TC518128BPL : DIP32-P-600
 - TC518128BFL : SOP32-P-450
 - TC518128BSPL : DIP32-P-300
 - TC518128BFWL : SOP32-P-525
 - TC518128BFTL : TSOP32-P-0820

Pin Connection (Top View)



TC518128BPL / BFL / BSPL / BFWL

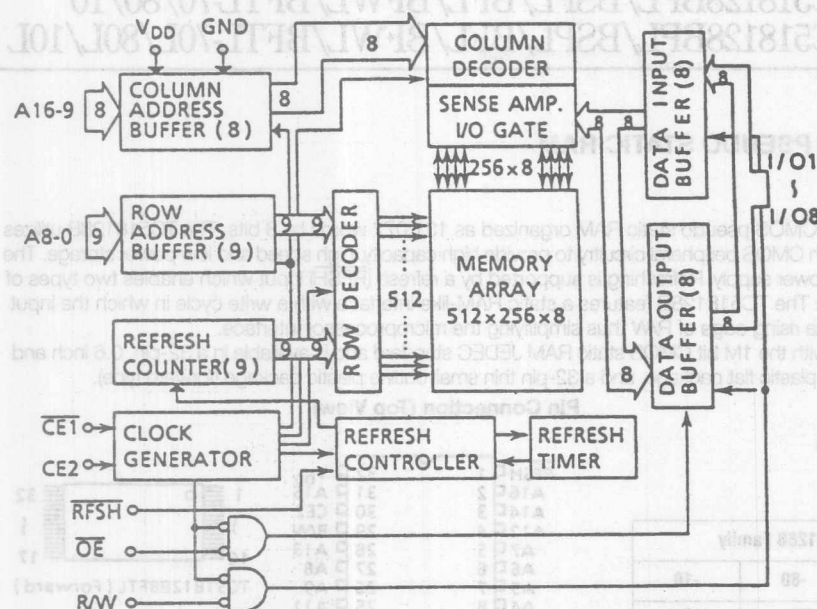
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
OE	Output Enable Input
RFSH	Refresh Input
CE1, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
V _{DD}	Power
GND	Ground

(TSOP)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CE2	A ₁₅	V _{DD}	RFSH	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	CE1	A ₁₀	OE

Block Diagram



Operating Mode

MODE	PIN	CE1	CE2	OE	R/W	RFSH	A0 ~ A16	I/O1 ~ 8
Read		L	H	L	H	*	V*	OUT
Write		L	H	*	L	*	V*	IN
CE only Refresh		L	H	H	H	*	V*	HZ
Auto/Self Refresh		H	*	*	*	L	*	HZ
Auto/Self Refresh		*	L	*	*	L	*	HZ
Standby		H	*	*	*	H	*	HZ
Standby		*	L	*	*	H	*	HZ

H = High level input (V_{IH})

L = Low level input (V_{IL})

* = V_{IH} or V_{IL}

V* = At the falling edge of CE1 (CE2 = H) or the rising edge of CE2 (CE1 = L), all address inputs are latched. At all other times, the address inputs are "H".

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V _{IH}	Input High Voltage	2.4	—	V _{DD} + 1.0	V	
V _{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I _{DDO}	Operating Current (Average) CE1, CE2, Address cycling: t _{RC} = t _{RC} min.	70ns version	—	50	70	3,4
		80ns version	—	40	60	
		100ns version	—	35	50	
I _{DDs1}	Standby Current CE1 = V _{IH} or CE2 = V _{IL} , RFSH = V _{IH}	—	—	1	mA	
I _{DDs2}	Standby Current CE1 = V _{DD} - 0.2V or CE2 = 0.2V, RFSH = V _{DD} - 0.2V	L version	—	100	200	μA
		LL version	—	35	50	μA
I _{DDf1}	Self Refresh Current (Average) CE1 = V _{IH} or CE2 = V _{IL} , RFSH = V _{IL}	—	—	1	mA	
I _{DDf2}	Self Refresh Current (Average) CE1 = V _{DD} - 0.2V or CE2 = 0.2V, RFSH = 0.2V	L version	—	100	200	μA
		LL version	—	35	50	μA
I _{DDf3}	Auto Refresh Current (Average) RFSH cycling: t _{FC} = t _{FC} min	—	—	2	mA	
I _{DDf4}	CE only Refresh Current (Average) CE1, CE2, Address cycling: t _{RC} = t _{RC} min.	70ns version	—	50	70	3
		80ns version	—	40	60	
		100ns version	—	35	50	
I _{I(L)}	Input Leakage Current 0V ≤ V _{IN} ≤ V _{DD} , All other Inputs not under test = 0V	—	—	±10	μA	
I _{O(L)}	Output Leakage Current Output Disabled (CE1 = V _{IH} or CE2 = V _{IL} or OE = V _{IH} or R/W = V _{IL}), 0V ≤ V _{OUT} ≤ V _{DD}	—	—	±10	μA	
V _{OH}	Output High Level I _{OH} = -1mA	2.4	—	—	V	
V _{OL}	Output Low Level I _{OL} = 2.1mA	—	—	0.4	V	

Note: For I_{DDs1} and I_{DDf1} with CE1 = V_{IH} (CE2 = V_{IL}), the specified limits are guaranteed under the condition CE2 = V_{IH} or CE2 = V_{IL}.
(CE1 = V_{IH} or CE1 = V_{IL}).
For I_{DDs2} and I_{DDf2} with CE1 ≥ V_{DD} - 0.2V (CE2 ≤ 0.2V), the specified limits are guaranteed under the condition CE2 ≥ V_{DD} - 0.2V or CE2 ≤ 0.2V.
(CE1 ≥ V_{DD} - 0.2V or CE1 ≤ 0.2V).

Capacitance* (V_{DD} = 5V, Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{I1}	Input Capacitance (A0 ~ A16)	—	5	pF
C _{I2}	Input Capacitance (CE1, CE2, OE, R/W, RFSH)	—	7	
C _{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

TC518128BPL/BSPL/BFL/BFWL/BFTL-70/80/10
TC518128BPL/BSPL/BFL/BFWL/BFTL-70L/80L/10L Static RAM

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	UNIT	-70		-80		-10		UNIT	NOTES
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	μs	115	—	130	—	160	—	ns	
t _{RMW}	Read Modify Write Cycle Time	μs	160	—	180	—	220	—	ns	
t _{CE}	CE Pulse Width	μs	70	10,000	80	10,000	100	10,000	ns	13
t _P	CE Precharge Time	μs	35	—	40	—	50	—	ns	
t _{CEA}	CE Access Time	μs	—	70	—	80	—	100	ns	
t _{OEa}	OE Access Time	μs	—	25	—	30	—	40	ns	
t _{CLZ}	CE to Output in Low -Z	μs	20	—	20	—	20	—	ns	
t _{OLZ}	OE to Output in Low -Z	μs	0	—	0	—	0	—	ns	
t _{WLZ}	Output Active from End of Write	μs	0	—	0	—	0	—	ns	
t _{CHZ}	Chip Disable to Output in High-Z	μs	0	20	0	20	0	25	ns	9
t _{OHZ}	OE Disable to Output in High-Z	μs	0	20	0	20	0	25	ns	9
t _{WHZ}	Write Enable to Output in High-Z	μs	0	25	0	25	0	30	ns	9
t _{ODS}	OE Output Disable Setup Time	μs	0	—	0	—	0	—	ns	
t _{ODH}	OE Output Disable Hold Time	μs	10	—	10	—	10	—	ns	
t _{RCS}	Read Command Setup Time	μs	0	—	0	—	0	—	ns	
t _{RCH}	Read Command Hold Time	μs	0	—	0	—	0	—	ns	
t _{WP}	Write Pulse Width	μs	20	—	25	—	30	—	ns	
t _{WCH}	Write Command Hold Time	μs	35	10,000	40	10,000	50	10,000	ns	
t _{CWL}	Write Command to CE Lead Time	μs	20	10,000	25	10,000	30	10,000	ns	
t _{DSW}	Data Setup Time from R/W	μs	15	—	20	—	25	—	ns	10
t _{DSC}	Data Setup Time from CE	μs	15	—	20	—	25	—	ns	10
t _{DHW}	Data Hold Time from R/W	μs	0	—	0	—	0	—	ns	10
t _{DHC}	Data Hold Time from CE	μs	0	—	0	—	0	—	ns	10
t _{ASC}	Address Setup Time	μs	0	—	0	—	0	—	ns	11
t _{AHC}	Address Hold Time	μs	20	—	25	—	30	—	ns	11
t _{RHC}	RFSH Command Hold Time	μs	15	—	15	—	15	—	ns	
t _{FC}	Auto Refresh Cycle Time	μs	115	—	130	—	160	—	ns	
t _{RFD}	RFSH Delay Time from CE	μs	35	—	40	—	50	—	ns	
t _{FAP}	RFSH Pulse Width (Auto Refresh)	μs	30	8,000	30	8,000	30	8,000	ns	12
t _{FP}	RFSH Precharge Time	μs	30	—	30	—	30	—	ns	12
t _{FAS}	RFSH Pulse Width (Self Refresh)	μs	8,000	—	8,000	—	8,000	—	ns	12
t _{FRS}	CE Delay Time from RFSH (Self Refresh)	μs	160	—	160	—	190	—	ns	12
t _{REF}	Refresh Period (512 cycles, A0 ~ A8)	μs	—	8	—	8	—	8	ms	
t _T	Transition Time (Rise and Fall)	ns	3	50	3	50	3	50	ns	
t _{CES}	CE2 Low Setup Time	μs	5	—	5	—	5	—	ns	14
t _{CEH}	CE2 Low Hold Time	μs	5	—	5	—	5	—	ns	14

Notes:

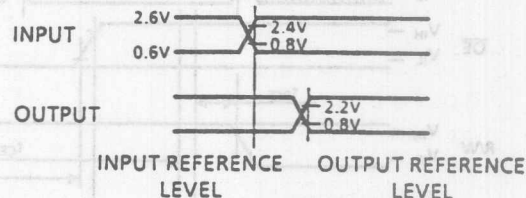
- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DDO} and I_{DDF4} depend on the cycle time.
- 4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high $\overline{CE1}$ or low CE2 is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

7) Timing reference levels

Input Levels : $V_{IH} = 2.6V$
 : $V_{IL} = 0.6V$

Input Reference Levels : $V_{IH} = 2.4V$
 : $V_{IL} = 0.8V$

Output Reference Levels : $V_{OH} = 2.2V$
 : $V_{OL} = 0.8V$

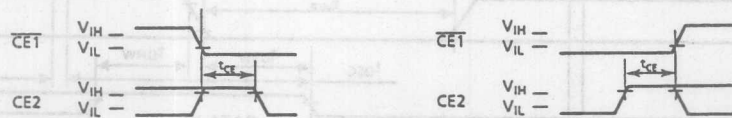


- 8) Measured with a load equivalent to 1 TTL load and 100pF.
- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) For write cycles, the input data is latched at the earlier of \overline{RW} or $\overline{CE1}$ rising edge (CE2 falling edge). Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 11) All address inputs are latched at the falling edge of $\overline{CE1}$ (rising edge of CE2). Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
- 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$.
 - Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 - Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

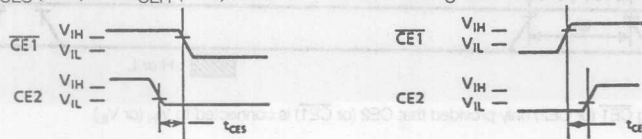
The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

- after self refresh
- if $\overline{RFSH} = "L"$ after power-up

- 13) The timings, t_{CE} (min.) and t_{CE} (max.) must be met for proper device operation.

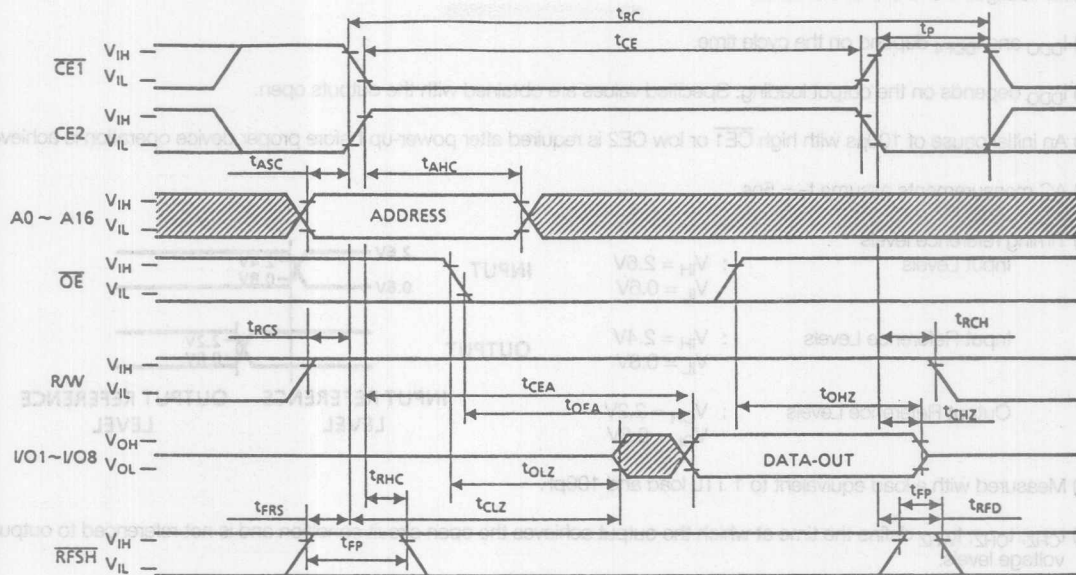


- 14) The timings, t_{CES} (min.) and t_{CEH} (min.) must be met when using $\overline{CE1}$ and CE2 as shown below.

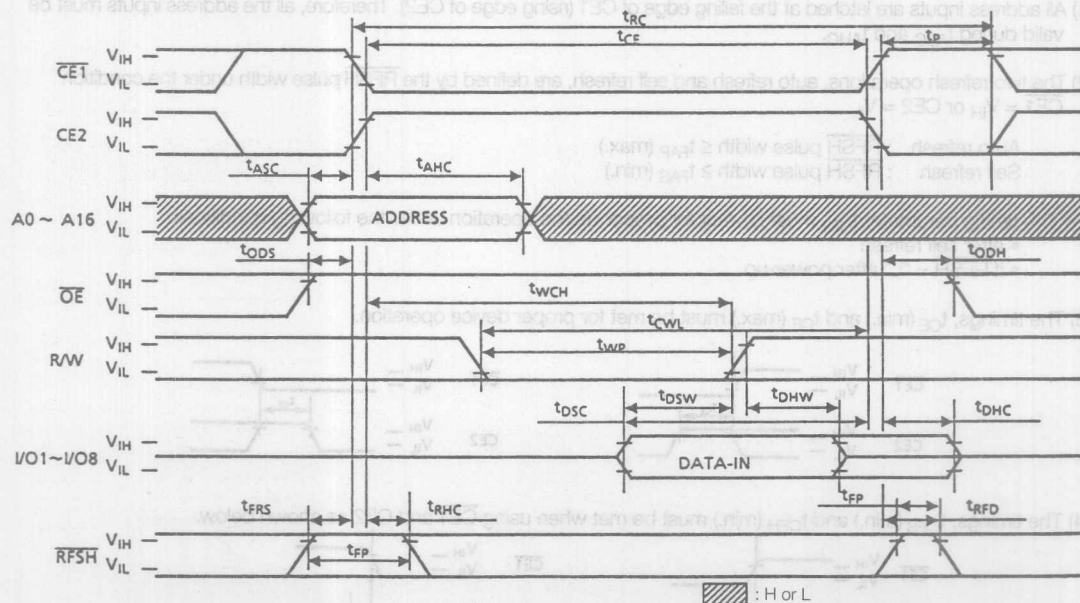


Timing Waveforms

Read Cycle

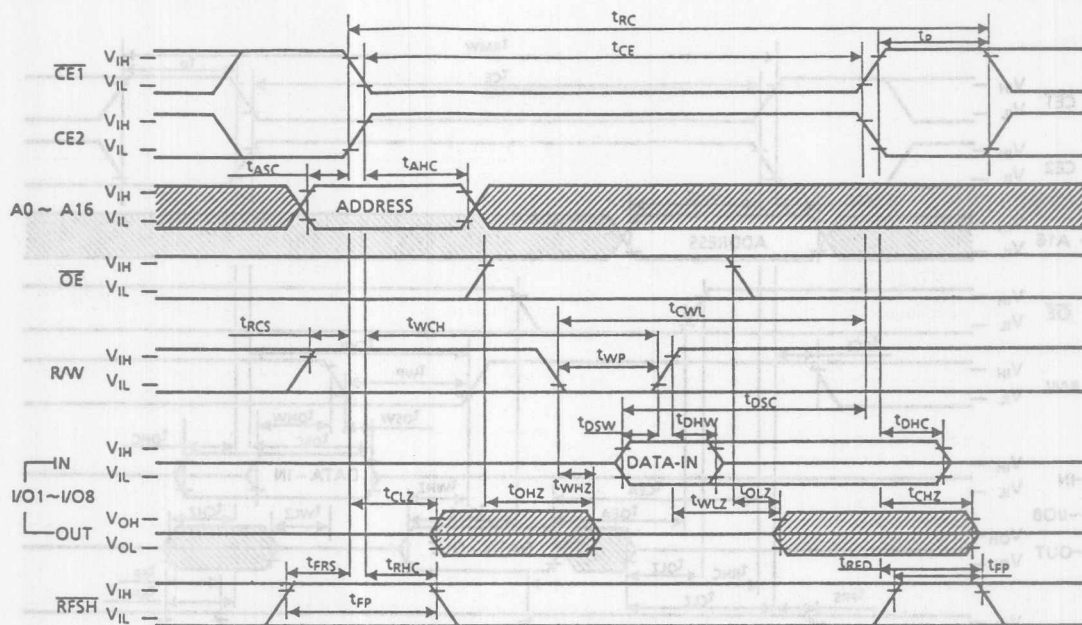


Write Cycle 1 (\overline{OE} Fixed High)

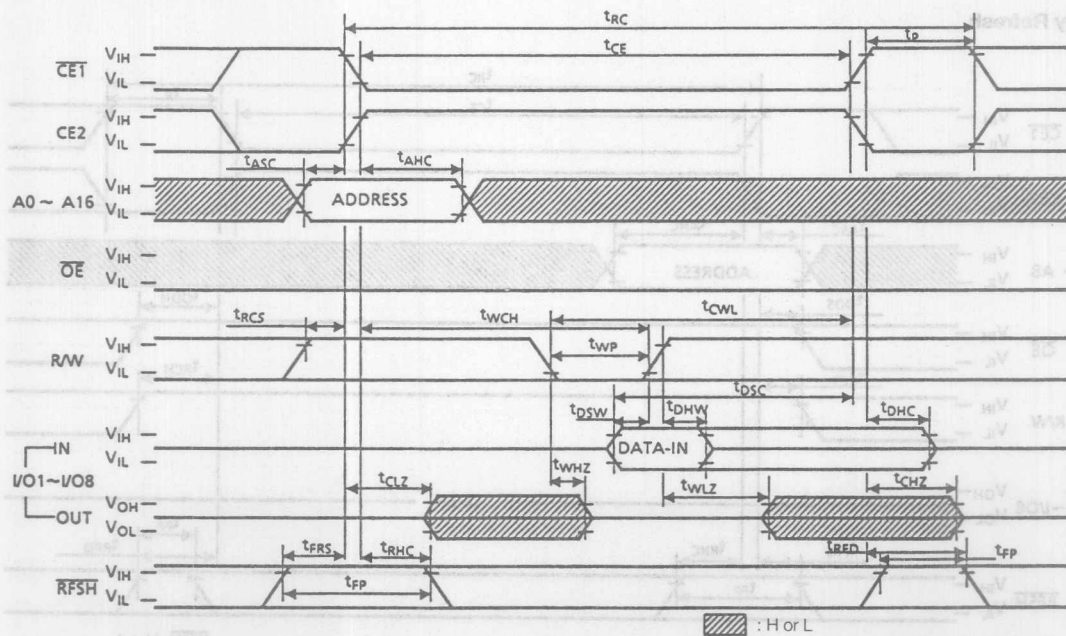


Note: The device can be operated by cycling $\overline{CE1}$ (or $\overline{CE2}$) only provided that $\overline{CE2}$ (or $\overline{CE1}$) is connected to V_{IH} (or V_{IL}).

Write Cycle 2 ($\overline{\text{OE}}$ Clocked)

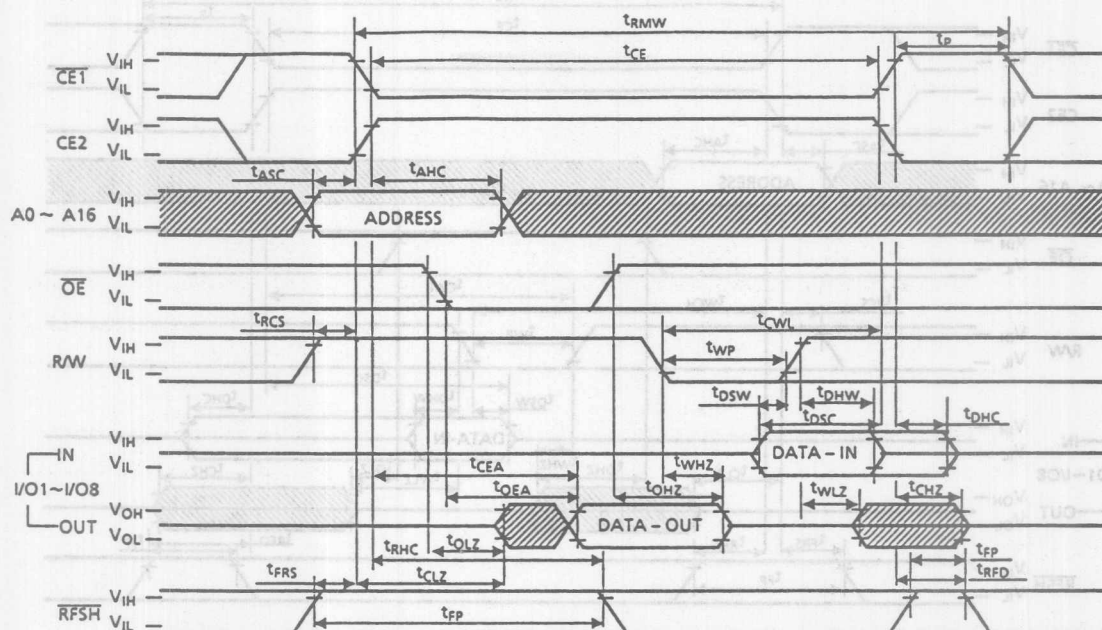


Write Cycle 3 ($\overline{\text{OE}}$ Fixed Low)

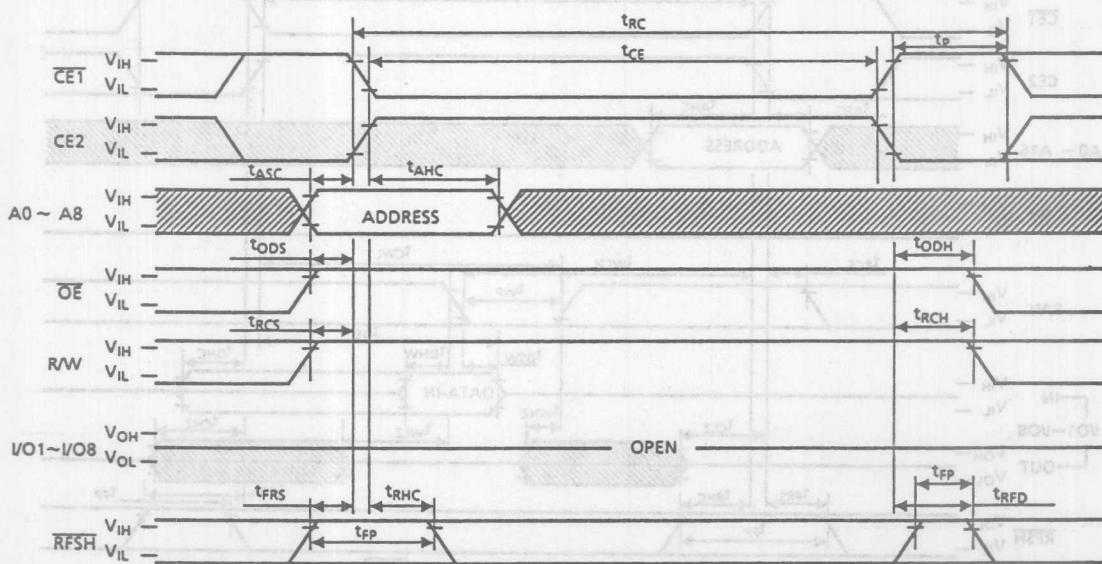


Note: The device can be operated by cycling $\overline{\text{CE1}}$ (or CE2) only provided that CE2 (or $\overline{\text{CE1}}$) is connected to V_{IH} (or V_{IL}).

Read Modify Write Cycle



CE Only Refresh

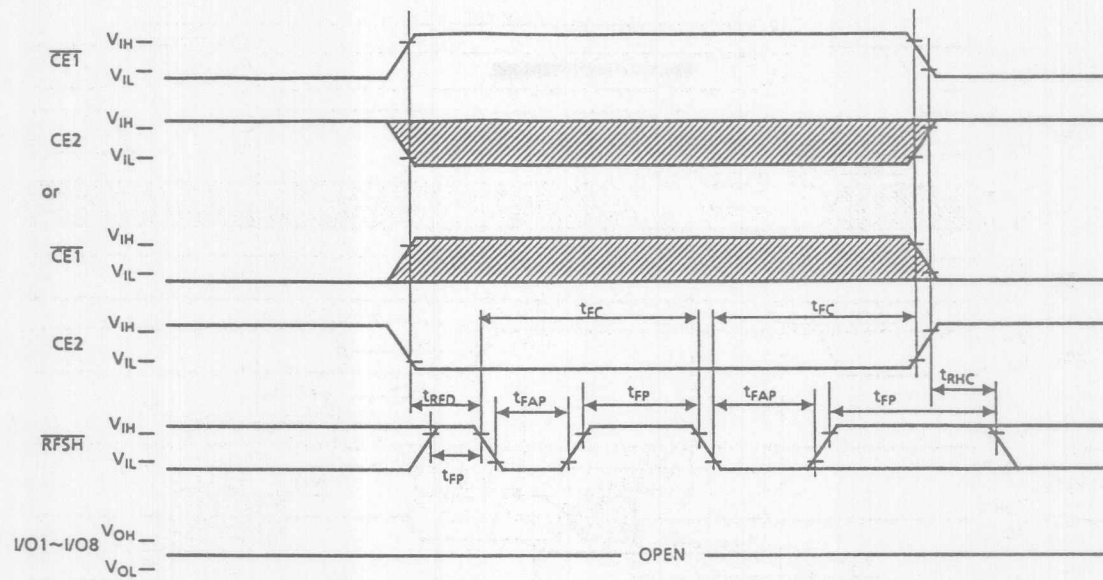


Note : A9 ~ A16 = V_{IH} or V_{IL}

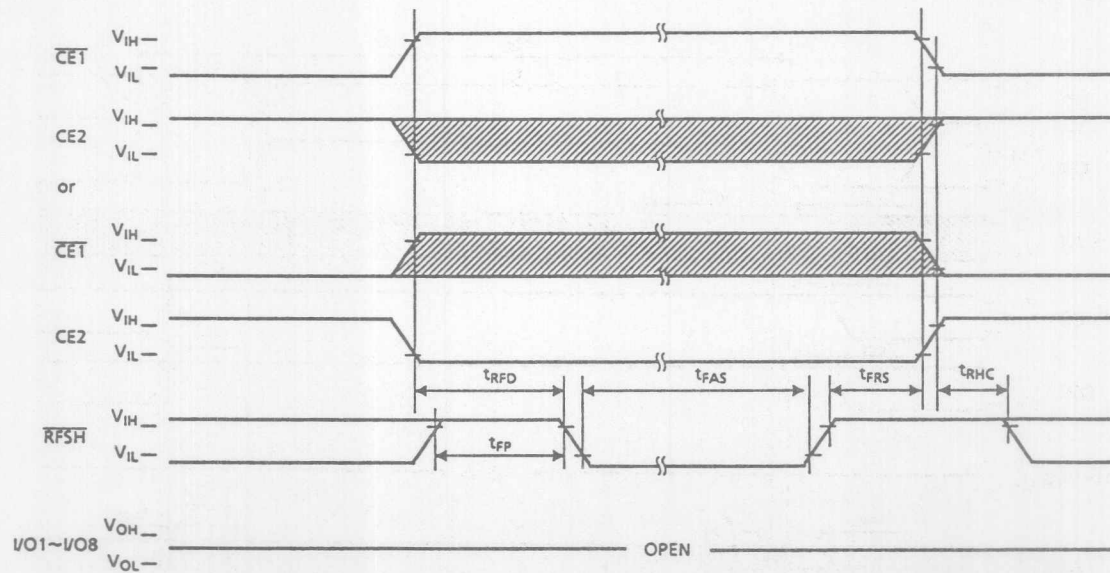
▨ : H or L

Note: The device can be operated by cycling $\overline{CE1}$ (or $\overline{CE2}$) only provided that $\overline{CE2}$ (or $\overline{CE1}$) is connected to V_{IH} (or V_{IL}).

Auto Refresh



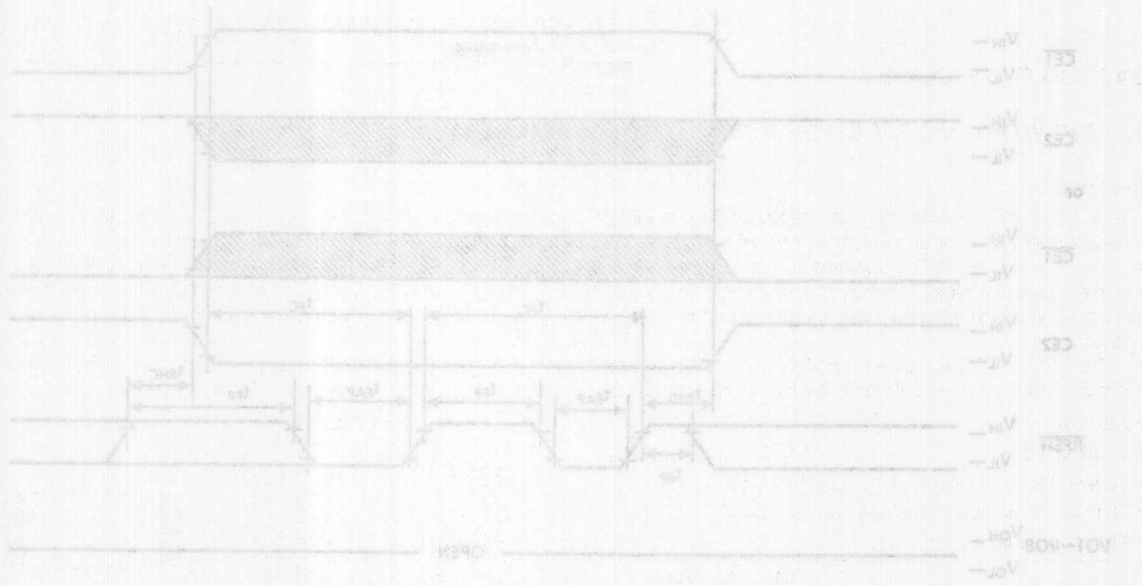
Self Refresh



Static RAM

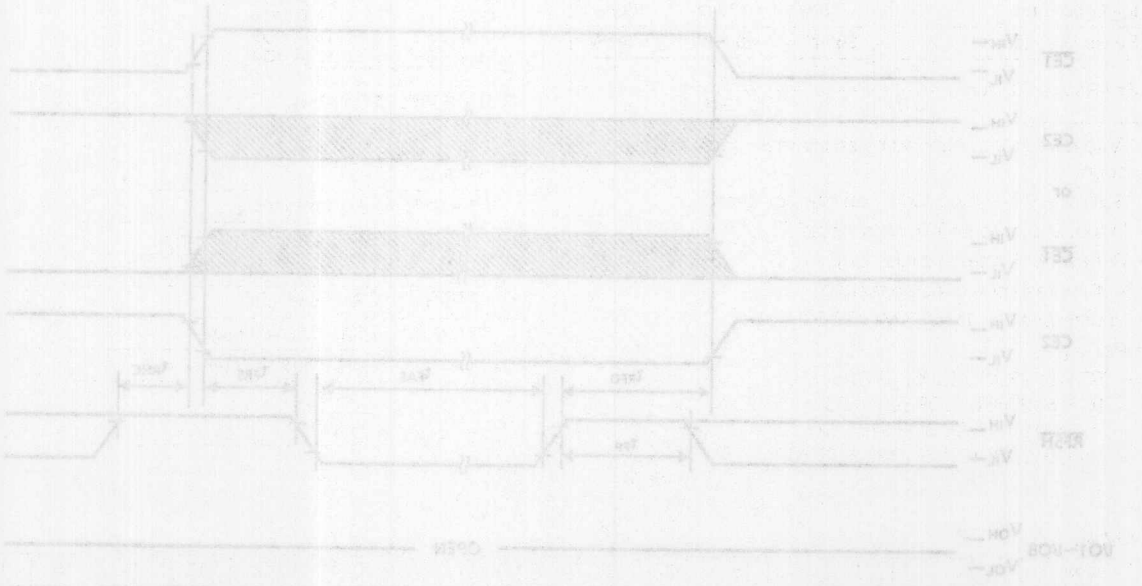
Notes

Auto Refresh



Note: $V_{DD} = V_{ih} = V_{oh}$ or $V_{il} = V_{ol}$

Self Refresh



Note: $V_{DD} = V_{ih} = V_{oh}$ or $V_{il} = V_{ol}$

TC518128BPL/BFL/BFWL/BFTL-70V/80V/10V

SILICON GATE CMOS

131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518128B-V is a 1M bit high speed CMOS pseudo static RAM organized as 131,072 words by 8 bits. The TC518128B-V utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518128B-V operates from a single power supply of 2.7 ~ 5.5V. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC518128B-V features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

The TC518128B-V is pin-compatible with the 1M bit CMOS static RAM JEDEC standard and is available in a 32-pin, 0.6 inch width plastic DIP, a small outline plastic flat package, and a 32-pin thin small outline plastic package (forward type).

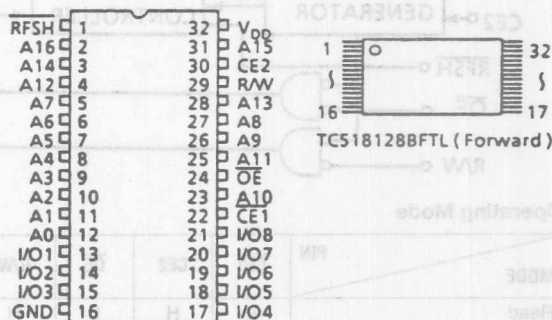
Features

- Organization: 131,072 words x 8 bits
- Low voltage operation: 2.7V ~ 5.5V
- Data retention supply voltage: 2.7V ~ 5.5V
- Fast access time

		TC518128B-V Family		
		-70	-80	-10
t _{CEA} CE Access Time		70ns	80ns	100ns
t _{OEA} OE Access Time		25ns	30ns	40ns
t _{RC} Cycle Time		115ns	130ns	160ns
Power Dissipation		385mW	330mW	275mW
Self Refresh Current	5.5V	50µA		
	3.0V	25µA		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 512 refresh cycles/8ms
- Auto refresh power down feature
- Pin compatible: 1M SRAM (JEDEC)
- Package
 - TC518128BPL: DIP32-P-600
 - TC518128BFL: SOP32-P-450
 - TC518128BFWL: SOP32-P-525
 - TC518128BFTL: TSOP32-P-0820

Pin Connection (Top View)



TC518128BPL / BFL / BFWL

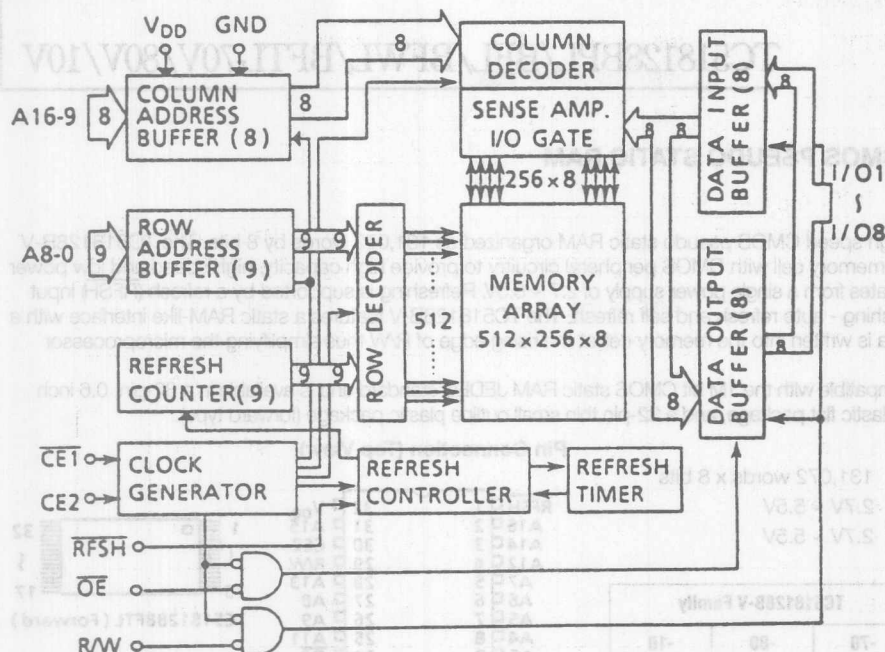
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
OE	Output Enable Input
RFSH	Refresh Input
CE1, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
V _{DD}	Power
GND	Ground

(TSOP)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CE2	A ₁₅	V _{DD}	RFSH	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	CE1	A ₁₀	OE

Block Diagram



Operating Mode

MODE	PIN	CE1	CE2	OE	R/W	RFSH	A0 ~ A16	I/O1 ~ 8
Read		L	H	L	H	*	V*	OUT
Write		L	H	*	L	*	V*	IN
CE only Refresh		L	H	H	H	*	V*	HZ
Auto/Self Refresh		H	*	*	*	L	*	HZ
Auto/Self Refresh		*	L	*	*	L	*	HZ
Standby		H	*	*	*	H	*	HZ
Standby		*	L	*	*	H	*	HZ

H = High level input (V_{IH})L = Low level input (V_{IL})* = V_{IH} or V_{IL} V* = At the falling edge of $\overline{CE1}$ ($CE2 = H$) or the rising edge of $CE2$ ($\overline{CE1} = L$), all address inputs are latched. At all other times, the address inputs are "**".

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	1
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1.0$	V	2
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) CE1, CE2, Address cycling: $t_{RC} = t_{RC \text{ min.}}$	70ns version	—	50	70	mA 3,4
		80ns version	—	40	60	
		100ns version	—	35	50	
I_{DDs1}	Standby Current CE1 = V_{IH} or CE2 = V_{IL} , RFSH = V_{IH}	—	—	1	mA	
I_{DDs2}	Standby Current CE1 = $V_{DD} - 0.2V$ or CE2 = $0.2V$, RFSH = $V_{DD} - 0.2V$	—	35	50	μA	
I_{DDF1}	Self Refresh Current (Average) CE1 = V_{IH} or CE2 = V_{IL} , RFSH = V_{IL}	—	—	1	mA	
I_{DDF2}	Self Refresh Current (Average) CE1 = $V_{DD} - 0.2V$ or CE2 = $0.2V$, RFSH = $0.2V$	—	35	50	μA	
I_{DDF3}	Auto Refresh Current (Average) RFSH cycling: $t_{FC} = t_{FC \text{ min}}$	—	—	2	mA	
I_{DDF4}	CE only Refresh Current (Average) CE1, CE2, Address cycling: $t_{RC} = t_{RC \text{ min.}}$	70ns version	—	50	70	mA 3
		80ns version	—	40	60	
		100ns version	—	35	50	
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = $0V$	—	—	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disabled (CE1 = V_{IH} or CE2 = V_{IL} or $\overline{OE} = V_{IH}$ or $R/W = V_{IL}$), $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level $I_{OH} = -1.0 \text{ mA}$	2.4	—	—	V	
V_{OL}	Output Low Level $I_{OL} = 2.1 \text{ mA}$	—	—	0.4	V	

Note: For I_{DDs1} and I_{DDF1} with CE1 = V_{IH} (CE2 = V_{IL}), the specified limits are guaranteed under the condition CE2 = V_{IH} or CE2 = V_{IL} (CE1 = V_{IH} or CE1 = V_{IL}).
For I_{DDs2} and I_{DDF2} with CE1 $\geq V_{DD} - 0.2V$ (CE2 $\leq 0.2V$), the specified limits are guaranteed under the condition CE2 $\geq V_{DD} - 0.2V$ or CE2 $\leq 0.2V$ (CE1 $\geq V_{DD} - 0.2V$ or CE1 $\leq 0.2V$).

Capacitance* ($V_{DD} = 5V$, $T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	—	5	pF
C_{I2}	Input Capacitance (CE1, CE2, \overline{OE} , R/W, RFSH)	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	115	—	130	—	160	—		
t_{RMW}	Read Modify Write Cycle Time	160	—	180	—	220	—		
t_{CE}	CE Pulse Width	70	10,000	80	10,000	100	10,000		13
t_P	CE Precharge Time	35	—	40	—	50	—		
t_{CEA}	CE Access Time	—	70	—	80	—	100		
t_{OEA}	\overline{OE} Access Time	—	25	—	30	—	40		
t_{CLZ}	CE to Output in Low -Z	20	—	20	—	20	—		
t_{OLZ}	\overline{OE} to Output in Low -Z	0	—	0	—	0	—		
t_{WLZ}	Output Active from End of Write	0	—	0	—	0	—		
t_{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	0	25		9
t_{OHZ}	\overline{OE} Disable to Output in High-Z	0	20	0	20	0	25		9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	25	0	30		9
t_{ODS}	\overline{OE} Output Disable Setup Time	0	—	0	—	0	—		
t_{ODH}	\overline{OE} Output Disable Hold Time	10	—	10	—	10	—		
t_{RCS}	Read Command Setup Time	0	—	0	—	0	—		
t_{RCH}	Read Command Hold Time	0	—	0	—	0	—		
t_{WP}	Write Pulse Width	20	—	25	—	30	—	ns	
t_{WCH}	Write Command Hold Time	35	10,000	40	10,000	50	10,000		
t_{CWL}	Write Command to CE Lead Time	20	10,000	25	10,000	30	10,000		
t_{DSW}	Data Setup Time from R/W	15	—	20	—	25	—		10
t_{DSC}	Data Setup Time from CE	15	—	20	—	25	—		10
t_{DHW}	Data Hold Time from R/W	0	—	0	—	0	—		10
t_{DHC}	Data Hold Time from CE	0	—	0	—	0	—		10
t_{ASC}	Address Setup Time	0	—	0	—	0	—		11
t_{AHC}	Address Hold Time	20	—	25	—	30	—		11
t_{RHC}	RFSH Command Hold Time	15	—	15	—	15	—		
t_{FC}	Auto Refresh Cycle Time	115	—	130	—	160	—		
t_{RFD}	RFSH Delay Time from CE	35	—	40	—	50	—		
t_{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000		12
t_{FP}	RFSH Precharge Time	30	—	30	—	30	—		12
t_{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—		12
t_{FRS}	CE Delay Time from RFSH (Self Refresh)	160	—	160	—	190	—		12
t_{REF}	Refresh Period (512 cycles, A0 ~ A8)	—	8	—	8	—	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50		
t_{CES}	CE2 Low Setup Time	5	—	5	—	5	—	ns	14
t_{CEH}	CE2 Low Hold Time	5	—	5	—	5	—		14

3.0V Operation

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	2.7	3.0	3.3	V	2
V_{IH}	Input High Voltage	$V_{DD} - 0.2V$	—	$V_{DD} + 1.0V$	V	
V_{IL}	Input Low Voltage	-0.5	—	0.2	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 3.0V \pm 0.3V$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) CE1, CE2, Address cycling: $t_{RC} = t_{RC} \text{ min.}$	—	15	20	mA	3,4
I_{DDS2}	Standby Current	—	15	25	μA	
I_{DDF2}	Self Refresh Current (Average)	—	15	25	μA	
I_{DDF3}	Auto Refresh Current (Average) RFSH cycling: $t_{FC} = t_{FC} \text{ min.}$	—	—	2	mA	
I_{DDF4}	CE only Refresh Current (Average) CE1, CE2, Address cycling: $t_{RC} = t_{RC} \text{ min.}$	—	15	20	mA	3
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = $0V$	—	—	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable, $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level	$I_{OH} = -1\text{mA}$ $I_{OH} = -100\mu\text{A}$	2.4 $V_{DD} - 0.2V$	— —	V	
V_{OL}	Output Low Level	$I_{OL} = 2.1\text{mA}$ $I_{OL} = 100\mu\text{A}$	— —	0.4 0.2	V	

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 3.0V±0.3V) (Notes: 5, 6, 8)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t _{RC}	Random Read, Write Cycle Time	240	—		
t _{RMW}	Read Modify Write Cycle Time	320	—		
t _{CE}	CE Pulse Width	150	10,000		13
t _P	CE Precharge Time	80	—		
t _{CEA}	CE Access Time	—	150		
t _{OEa}	\overline{OE} Access Time	—	80		
t _{CLZ}	CE to Output in Low -Z	20	—		
t _{OLZ}	\overline{OE} to Output in Low -Z	5	—		
t _{WLZ}	Output Active from End of Write	5	—		
t _{CHZ}	Chip Disable to Output in High-Z	0	30		9
t _{OHZ}	\overline{OE} Disable to Output in High-Z	0	30		9
t _{WHZ}	Write Enable to Output in High-Z	0	40		9
t _{ODS}	\overline{OE} Output Disable Setup Time	0	—		
t _{ODH}	\overline{OE} Output Disable Hold Time	10	—		
t _{RCS}	Read Command Setup Time	0	—		
t _{RCH}	Read Command Hold Time	0	—	ns	
t _{WP}	Write Pulse Width	35	—		
t _{WCH}	Write Command Hold Time	70	10,000		
t _{CWL}	Write Command to CE Lead Time	35	10,000		
t _{DSW}	Data Setup Time from R/W	30	—		10
t _{DSC}	Data Setup Time from CE	30	—		10
t _{DHW}	Data Hold Time from R/W	0	—		10
t _{DHC}	Data Hold Time from CE	0	—		10
t _{ASC}	Address Setup Time	0	—		11
t _{AHC}	Address Hold Time	35	—		11
t _{RHC}	\overline{RFSH} Command Hold Time	15	—		
t _{FC}	Auto Refresh Cycle Time	240	—		
t _{RFD}	\overline{RFSH} Delay Time from CE	80	—		
t _{FAP}	\overline{RFSH} Pulse Width (Auto Refresh)	50	8,000		12
t _{FP}	\overline{RFSH} Precharge Time	50	—		12
t _{FAS}	\overline{RFSH} Pulse Width (Self Refresh)	8,000	—		12
t _{FRS}	CE Delay Time from \overline{RFSH} (Self Refresh)	300	—		12
t _{REF}	Refresh Period (512 cycles, A0 ~ A8)	—	8	ms	
t _T	Transition Time (Rise and Fall)	3	50		
t _{CES}	CE2 Low Setup Time	10	—	ns	14
t _{CEH}	CE2 Low Hold Time	10	—		14

Timing Reference Levels:

Input Reference Levels: 1.5V/1.5V

Output Reference Levels: 1.5V/1.5V

Notes:

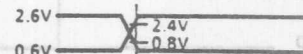
- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DDO} and I_{DDF4} depend on the cycle time.
- 4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high $\overline{CE1}$ or low CE2 is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_f = 5$ ns.

7) Timing reference levels

Input Levels

$$\begin{aligned} &: V_{IH} = 2.6V \\ &V_{IL} = 0.6V \end{aligned}$$

INPUT



Input Reference Levels

$$\begin{aligned} &: V_{IH} = 2.4V \\ &V_{IL} = 0.8V \end{aligned}$$

OUTPUT

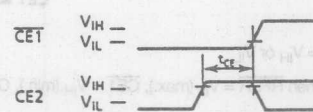
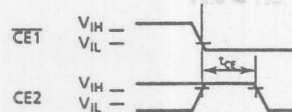


Output Reference Levels

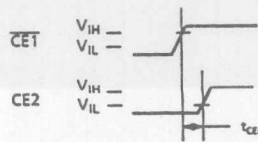
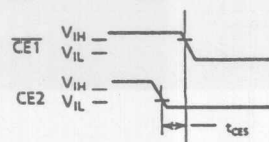
$$\begin{aligned} &: V_{OH} = 2.2V \\ &V_{OL} = 0.8V \end{aligned}$$

INPUT REFERENCE
LEVELOUTPUT REFERENCE
LEVEL

- 8) Measured with a load equivalent to 1 TTL load and 100pF.
 - 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 - 10) For write cycles, the input data is latched at the earlier of R/W or $\overline{CE1}$ rising edge (CE2 falling edge). Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
 - 11) All address inputs are latched at the falling edge of $\overline{CE1}$ (rising edge of CE2). Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
 - 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$.
 - Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 - Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)
- The timing parameter t_{FRS} must be met for proper device operation under the following conditions:
- after self refresh
 - if $\overline{RFSH} = "L"$ after power-up
- 13) The timings, t_{CE} (min.) and t_{CE} (max.) must be met for proper device operation.

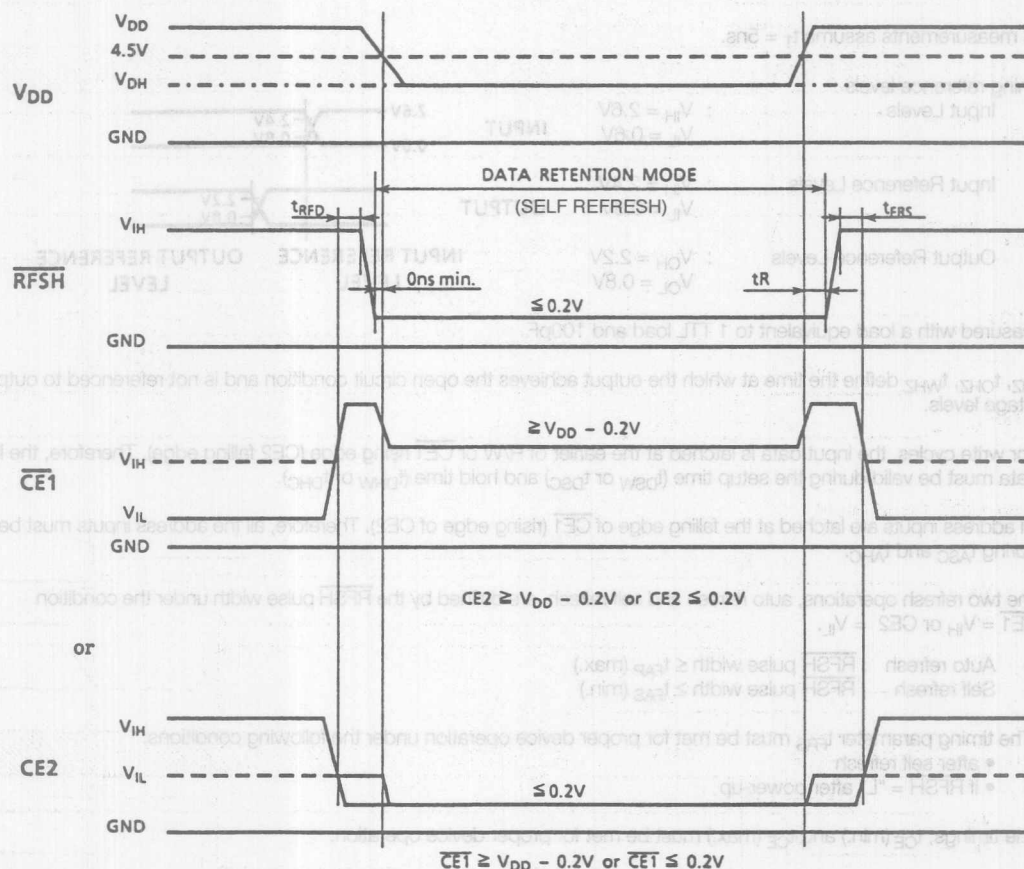


- 14) The timings, t_{CES} (min.) and t_{CEH} (min.) must be met when using $\overline{CE1}$ and CE2 as shown below.



Data Retention Characteristics ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.7	—	5.5	V
I_{DDF2}	Self Refresh Current	$V_{DH} = 3.0\text{V}$	15	25	μA
		$V_{DH} = 5.5\text{V}$	35	50	
t_R	Recovery Time	5	—	—	ms

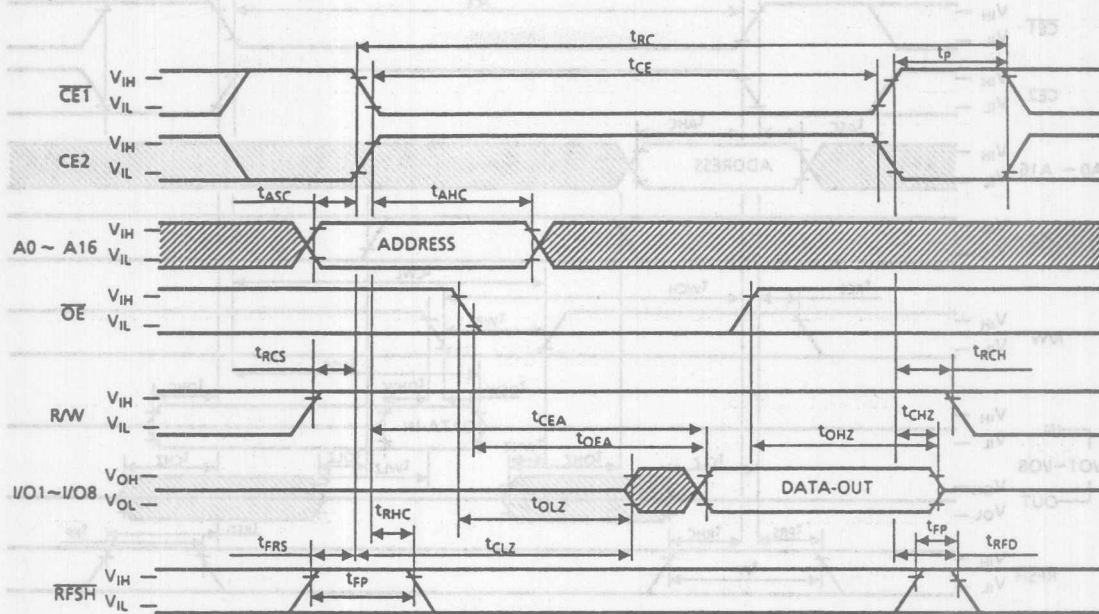
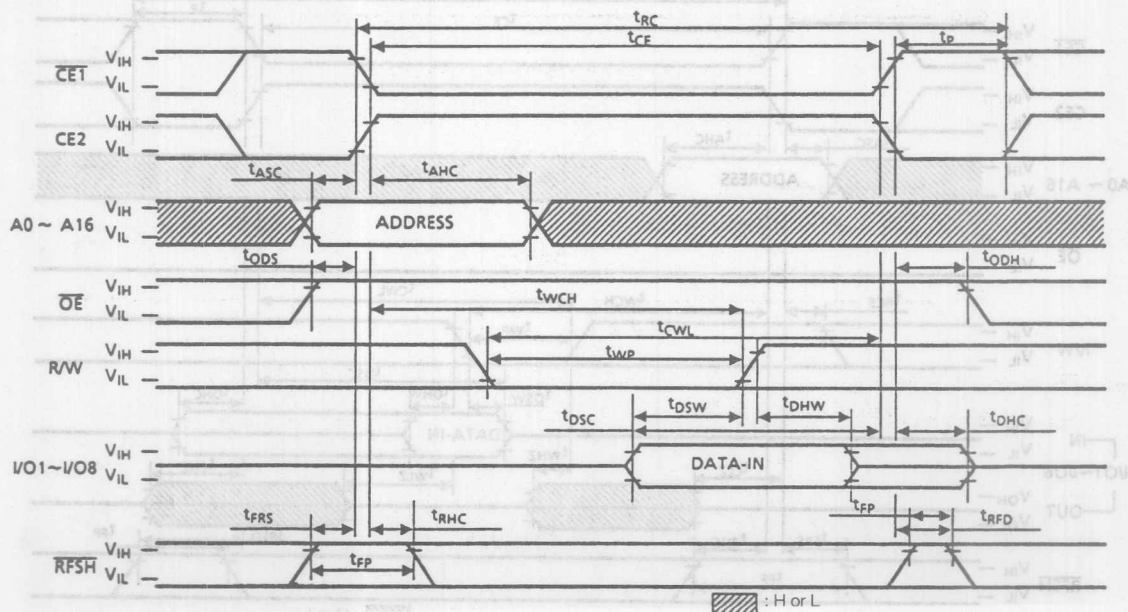


Notes: \overline{OE} , R/W , $A0 \sim A16 = V_{IH}$ or V_{IL} .

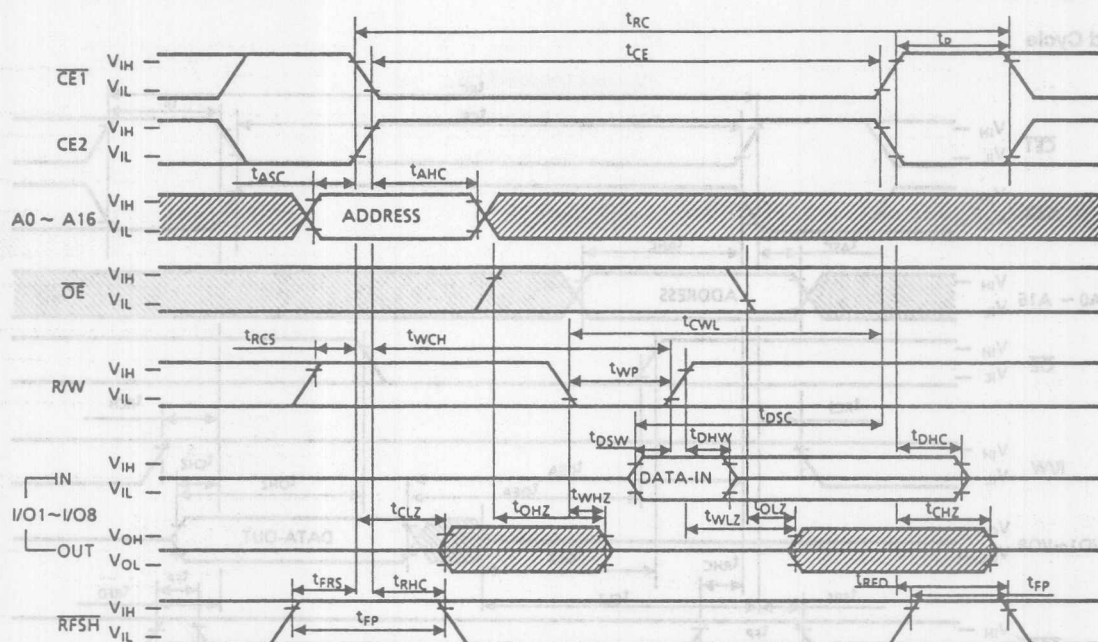
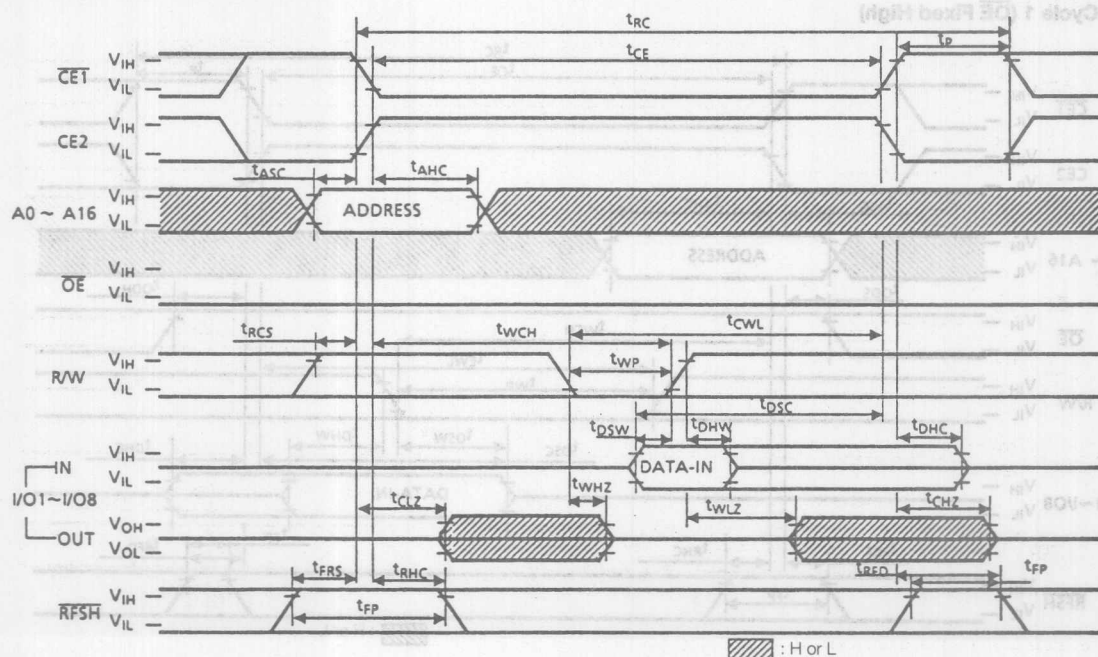
I_{DDF1} is applicable when $RFSH = V_{IL}$ (max.), $CE1 = V_{IH}$ (min.), $CE2 = V_{IL}$ (max.).

Timing Waveforms

Read Cycle

Write Cycle 1 (\overline{OE} Fixed High)

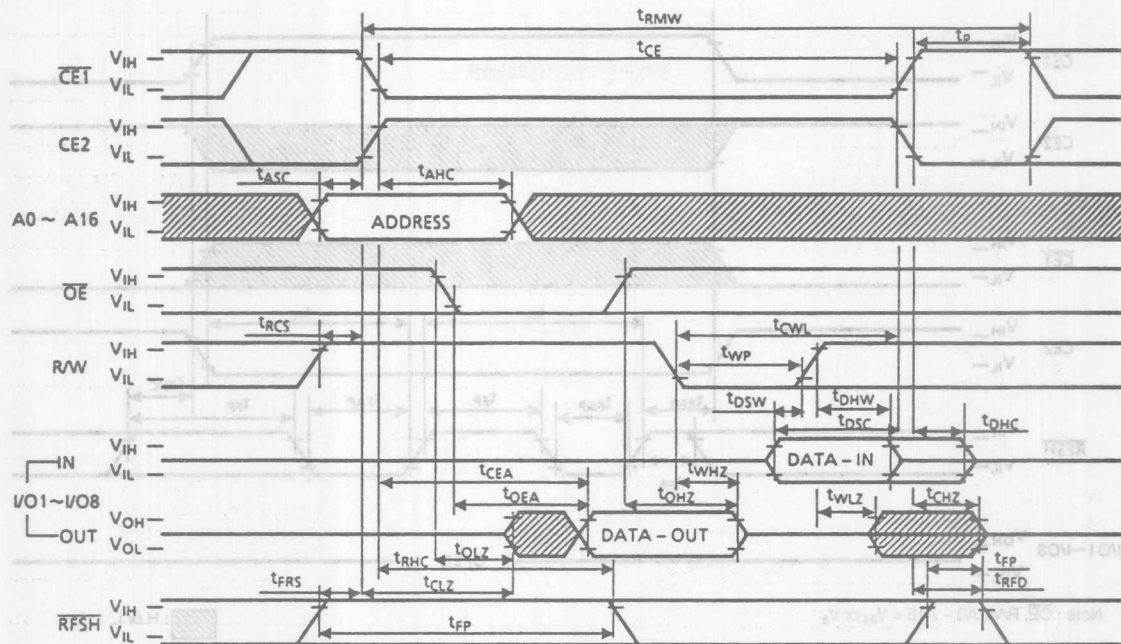
Note: The device can be operated by cycling $\overline{CE1}$ (or $\overline{CE2}$) only provided that $\overline{CE2}$ (or $\overline{CE1}$) is connected to V_{IH} (or V_{IL}).

Write Cycle 2 (\overline{OE} Clocked)Write Cycle 3 (\overline{OE} Fixed Low)

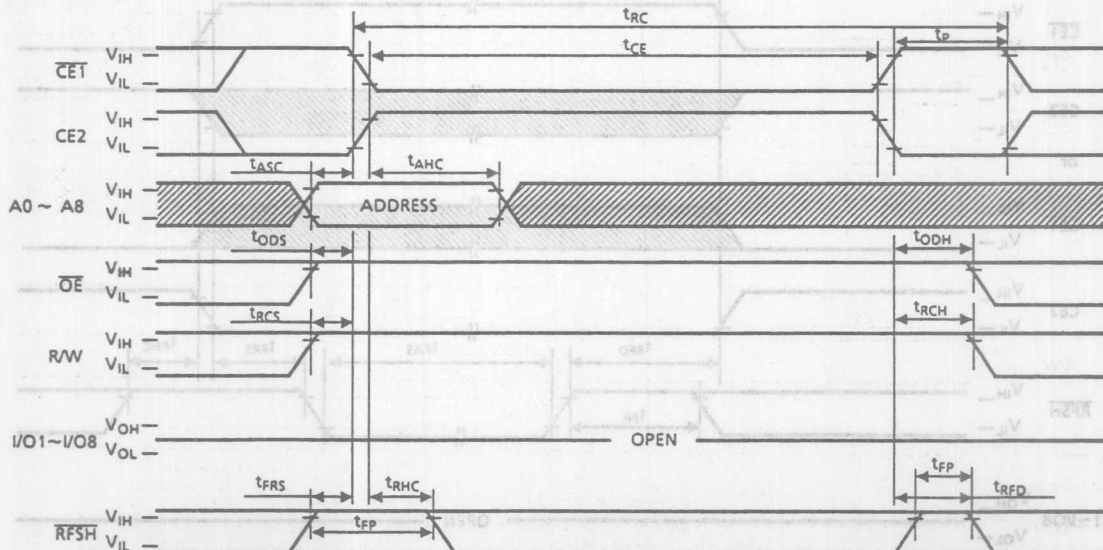
: H or L

Note: The device can be operated by cycling CE1 (or CE2) only provided that CE2 (or CE1) is connected to V_{IH} (or V_{IL}).

Read Modify Write Cycle



CE Only Refresh

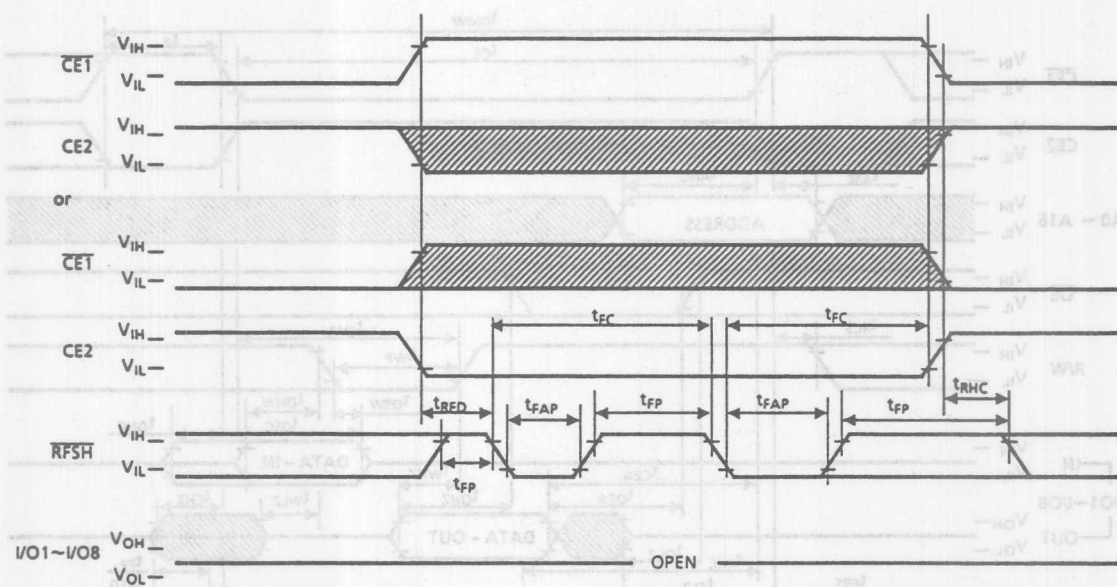


Note: A9 ~ A16 = V_{IH} or V_{IL}

▨: H or L

Note: The device can be operated by cycling $\overline{CE1}$ (or $\overline{CE2}$) only provided that $\overline{CE2}$ (or $\overline{CE1}$) is connected to V_{IH} (or V_{IL}).

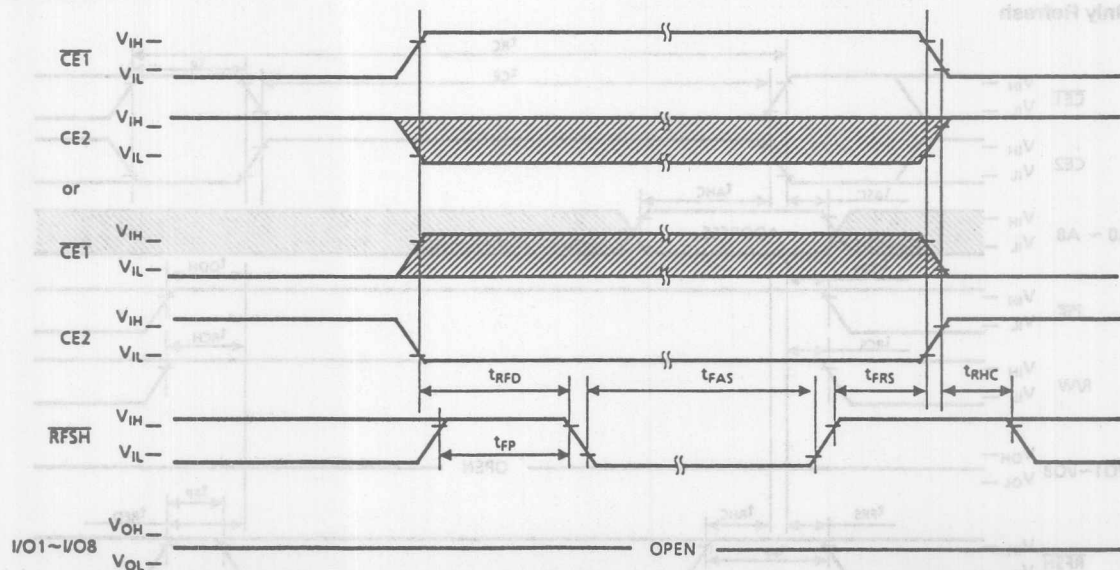
Auto Refresh



Note : \overline{OE} , \overline{RW} , $A0 \sim A16 = V_{IH}$ or V_{IL}

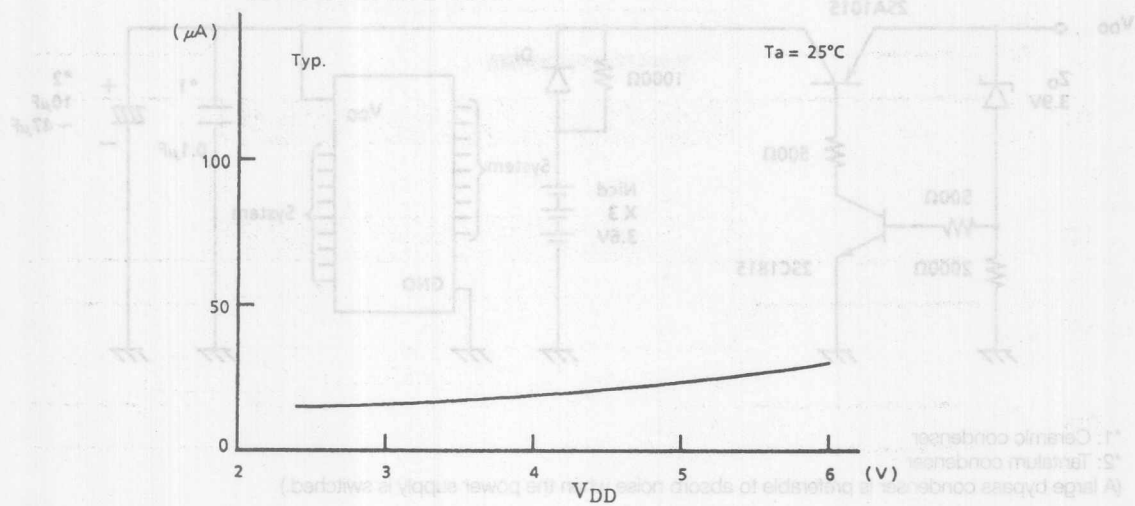
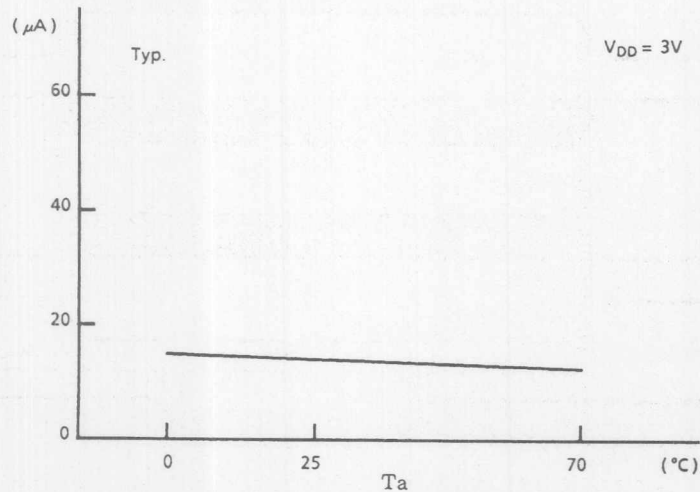
▨ : H or L

Self Refresh

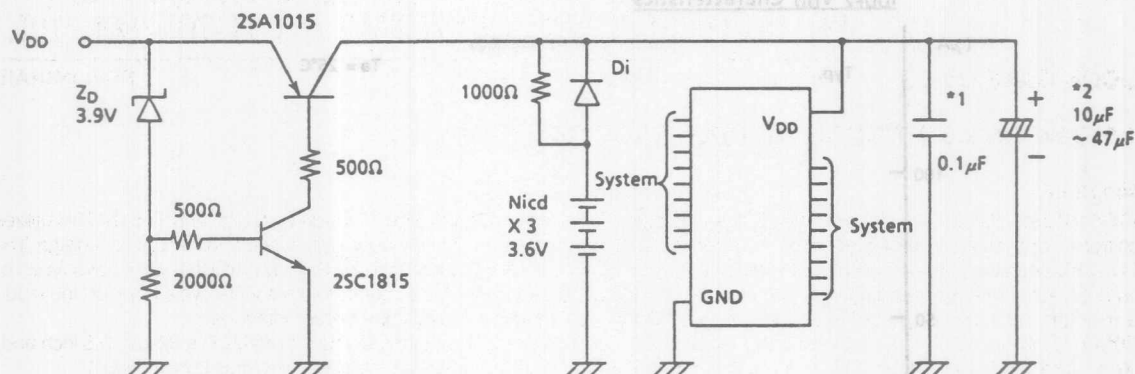


Note : \overline{OE} , \overline{RW} , $A0 \sim A16 = V_{IH}$ or V_{IL}

▨ : H or L

I_{DDF2} V_{DD} Characteristics I_{DDF2} Temp. Characteristics

Battery Backup Application Example

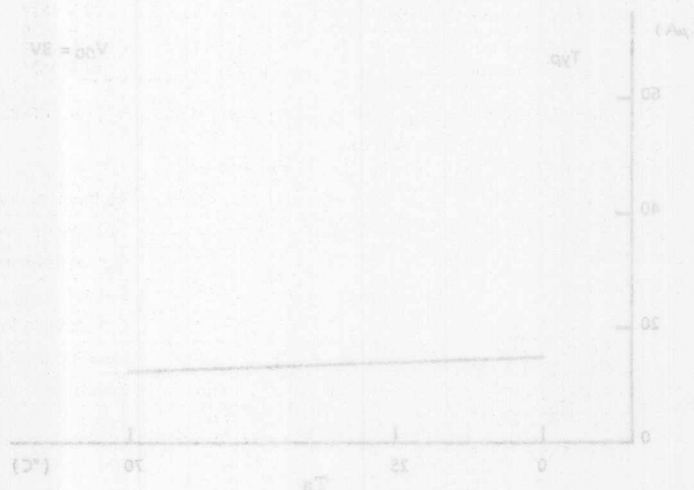


*1: Ceramic condenser

*2: Tantalum condenser

(A large bypass condenser is preferable to absorb noise when the power supply is switched.)

This circuit does not have memory protection. Therefore, rapid turnoff of the power supply must be avoided. Enter the Self Refresh mode before changing to the battery backup power supply.



TC518128CPL/CSPL/CFL/CFWL/CFTL-70/80/10 TC518128CPL/CSPL/CFL/CFWL/CFTL-70L/80L/10L

SILICON GATE CMOS

PRELIMINARY

131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518128C is a 1M bit high speed CMOS pseudo static RAM organized as 131,072 words by 8 bits. The TC518128C utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518128C operates from a single 5V power supply. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC518128C features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

The TC518128C is pin-compatible with the 1M bit CMOS static RAM JEDEC standard and is available in a 32-pin, 0.6 inch and 0.3 inch width plastic DIP, a small outline plastic flat package, and a 32-pin thin small outline plastic package (forward type).

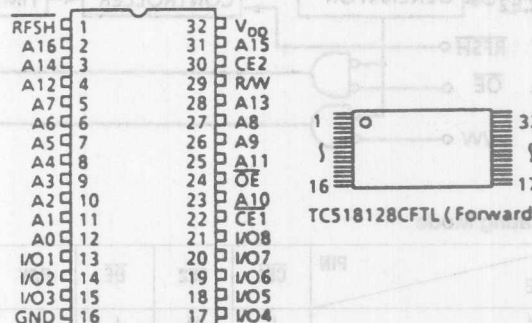
Features

- Organization: 131,072 words x 8 bits
- Single 5V power supply
- Fast access time

	TC518128C Family		
	-70	-80	-10
t _{CEA} CE Access Time	70ns	80ns	100ns
t _{OE} OE Access Time	25ns	30ns	40ns
t _{RC} Cycle Time	115ns	130ns	160ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	100μA (L version) 50μA (LL version)		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 512 refresh cycles/8ms
- Auto refresh power down feature
- Pin compatible: 1M SRAM (JEDEC)
- Package
 - TC518128CPL : DIP32-P-600
 - TC518128CFL : SOP32-P-450
 - TC518128CSPL : DIP32-P-300
 - TC518128CFWL : SOP32-P-525
 - TC518128CFTL : TSOP32-P-0820

Pin Connection (Top View)



TC518128CPL/CFL/CSPL/CFWL

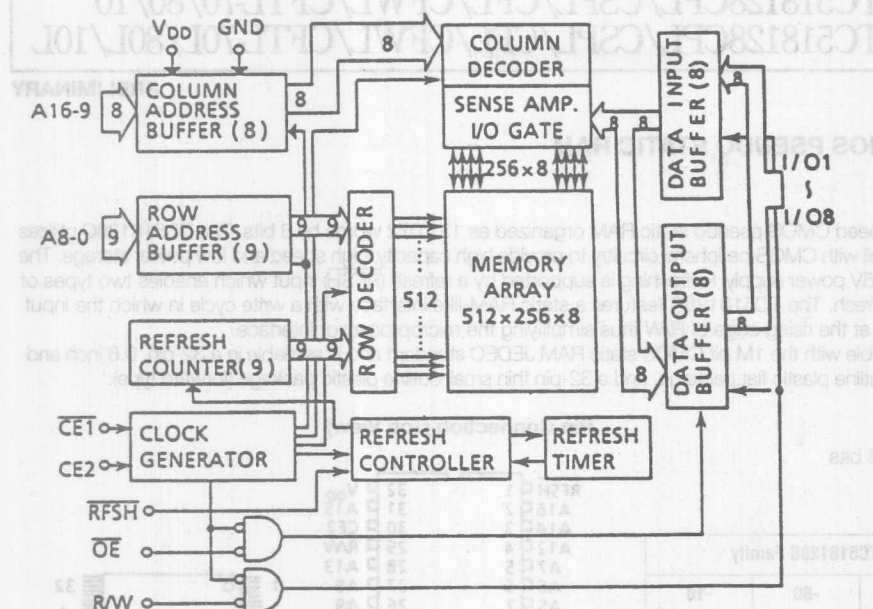
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
OE	Output Enable Input
RFSH	Refresh Input
CE1, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
V _{DD}	Power
GND	Ground

(TSOP)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CE2	A ₁₅	V _{DD}	RFSH	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	CE1	A ₁₀	OE

Block Diagram



Operating Mode

MODE	PIN	CE1	CE2	OE	R/W	RFSH	AO ~ A16	I/O1 ~ 8
Read		L	H	L	H	*	V*	OUT
Write		L	H	*	L	*	V*	IN
CE only Refresh		L	H	H	H	*	V*	HZ
Auto/Self Refresh		H	*	*	*	L	*	HZ
Auto/Self Refresh		*	L	*	*	L	*	HZ
Standby		H	*	*	*	H	*	HZ
Standby		*	L	*	*	H	*	HZ

H = High level input (V_{IH})

L = Low level input (V_{IL})

* = V_{IH} or V_{IL}

V* = At the falling edge of CE1 (CE2 = H) or the rising edge of CE2 (CE1 = L), all address inputs are latched. At all other times, the address inputs are ***.

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V	
V _{IH}	Input High Voltage	2.4	—	V _{DD} + 1.0	V	2
V _{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I _{DDO}	Operating Current (Average) CE1, CE2, Address cycling: t _{RC} = t _{RC} min.	70ns version	—	50	70	mA 3,4
		80ns version	—	40	60	
		100ns version	—	35	50	
I _{DDs1}	Standby Current CE1 = V _{IH} or CE2 = V _{IL} , RFSH = V _{IH}	—	—	1	mA	
I _{DDs2}	Standby Current CE1 = V _{DD} - 0.2V or CE2 = 0.2V, RFSH = V _{DD} - 0.2V	L version	—	50	100	μA
		LL version	—	35	50	μA
I _{DDF1}	Self Refresh Current (Average) CE1 = V _{IH} or CE2 = V _{IL} , RFSH = V _{IL}	—	—	1	mA	
I _{DDF2}	Self Refresh Current (Average) CE1 = V _{DD} - 0.2V or CE2 = 0.2V, RFSH = 0.2V	L version	—	50	100	μA
		LL version	—	35	50	μA
I _{DDF3}	Auto Refresh Current (Average) RFSH cycling: t _{FC} = t _{FC} min	—	—	2	mA	
I _{DDF4}	CE only Refresh Current (Average) CE1, CE2, Address cycling: t _{RC} = t _{RC} min.	70ns version	—	50	70	mA 3
		80ns version	—	40	60	
		100ns version	—	35	50	
I _{I(L)}	Input Leakage Current 0V ≤ V _{IN} ≤ V _{DD} , All other Inputs not under test = 0V	—	—	±10	μA	
I _{O(L)}	Output Leakage Current Output Disabled (CE1 = V _{IH} or CE2 = V _{IL} or OE = V _{IH} or R/W = V _{IL}), 0V ≤ V _{OUT} ≤ V _{DD}	—	—	±10	μA	
V _{OH}	Output High Level I _{OH} = -1mA	2.4	—	—	V	
V _{OL}	Output Low Level I _{OL} = 2.1mA	—	—	0.4	V	

Note: For I_{DDs1} and I_{DDF1} with CE1 = V_{IH} (CE2 = V_{IL}), the specified limits are guaranteed under the condition CE2 = V_{IH} or CE2 = V_{IL} (CE1 = V_{IH} or CE1 = V_{IL}).
For I_{DDs2} and I_{DDF2} with CE1 ≥ V_{DD} - 0.2V (CE2 ≤ 0.2V), the specified limits are guaranteed under the condition CE2 ≥ V_{DD} - 0.2V or CE2 ≤ 0.2V (CE1 ≥ V_{DD} - 0.2V or CE1 ≤ 0.2V).

Capacitance* (V_{DD} = 5V, Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{I1}	Input Capacitance (A0 ~ A16)	—	5	pF
C _{I2}	Input Capacitance (CE1, CE2, OE, R/W, RFSH)	—	7	
C _{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

TC518128CPL/CSPL/CFL/CFWL/CFTL-70/80/10
TC518128CPL/CSPL/CFL/CFWL/CFTL-70L/80L/10L Static RAM

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	115	—	130	—	160	—		
t _{RMW}	Read Modify Write Cycle Time	160	—	180	—	220	—		
t _{CE}	CE Pulse Width	70	10,000	80	10,000	100	10,000		13
t _p	CE Precharge Time	35	—	40	—	50	—		
t _{CEA}	CE Access Time	—	70	—	80	—	100		
t _{OEA}	\overline{OE} Access Time	—	25	—	30	—	40		
t _{CLZ}	CE to Output in Low -Z	20	—	20	—	20	—		
t _{OLZ}	\overline{OE} to Output in Low -Z	0	—	0	—	0	—		
t _{WLZ}	Output Active from End of Write	0	—	0	—	0	—		
t _{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	0	25		9
t _{OHZ}	\overline{OE} Disable to Output in High-Z	0	20	0	20	0	25		9
t _{WHZ}	Write Enable to Output in High-Z	0	25	0	25	0	30		9
t _{ODS}	\overline{OE} Output Disable Setup Time	0	—	0	—	0	—		
t _{ODH}	\overline{OE} Output Disable Hold Time	10	—	10	—	10	—		
t _{RCS}	Read Command Setup Time	0	—	0	—	0	—		
t _{RCH}	Read Command Hold Time	0	—	0	—	0	—		
t _{WP}	Write Pulse Width	20	—	25	—	30	—	ns	
t _{WCH}	Write Command Hold Time	35	10,000	40	10,000	50	10,000		
t _{CWL}	Write Command to CE Lead Time	20	10,000	25	10,000	30	10,000		
t _{DSW}	Data Setup Time from R/W	15	—	20	—	25	—		10
t _{DSC}	Data Setup Time from CE	15	—	20	—	25	—		10
t _{DHW}	Data Hold Time from R/W	0	—	0	—	0	—		10
t _{DHC}	Data Hold Time from CE	0	—	0	—	0	—		10
t _{ASC}	Address Setup Time	0	—	0	—	0	—		11
t _{AHC}	Address Hold Time	20	—	25	—	30	—		11
t _{RHC}	RFSH Command Hold Time	15	—	15	—	15	—		
t _{FC}	Auto Refresh Cycle Time	115	—	130	—	160	—		
t _{RFD}	RFSH Delay Time from CE	35	—	40	—	50	—		
t _{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000		12
t _{FP}	RFSH Precharge Time	30	—	30	—	30	—		12
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—		12
t _{FRS}	CE Delay Time from RFSH (Self Refresh)	160	—	160	—	190	—		12
t _{REF}	Refresh Period (512 cycles, A0 ~ A8)	—	8	—	8	—	8	ms	
t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	
t _{CES}	CE2 Low Setup Time	5	—	5	—	5	—	ns	14
t _{CEH}	CE2 Low Hold Time	5	—	5	—	5	—	ns	14

Notes:

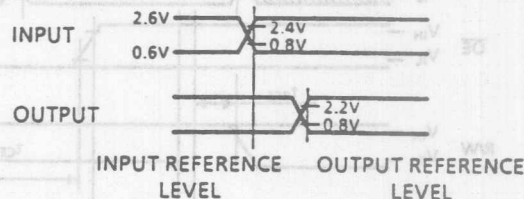
- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DDO} and I_{DDF4} depend on the cycle time.
- 4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high $\overline{CE1}$ or low CE2 is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

7) Timing reference levels

Input Levels : $V_{IH} = 2.6V$
 : $V_{IL} = 0.6V$

Input Reference Levels : $V_{IH} = 2.4V$
 : $V_{IL} = 0.8V$

Output Reference Levels : $V_{OH} = 2.2V$
 : $V_{OL} = 0.8V$



- 8) Measured with a load equivalent to 1 TTL load and 100pF.

- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

- 10) For write cycles, the input data is latched at the earlier of R/W or $\overline{CE1}$ rising edge (CE2 falling edge). Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).

- 11) All address inputs are latched at the falling edge of $\overline{CE1}$ (rising edge of CE2). Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .

- 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$.

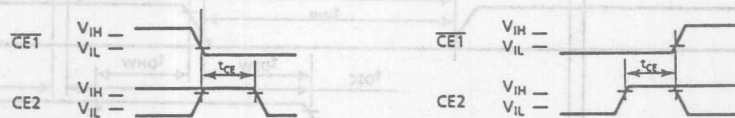
Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)

Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

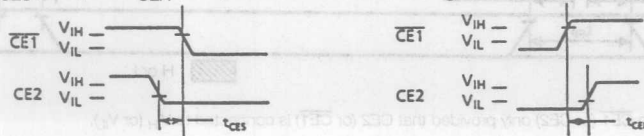
The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

- after self refresh
- if $\overline{RFSH} = "L"$ after power-up

- 13) The timings, t_{CE} (min.) and t_{CEH} (min.) must be met for proper device operation.

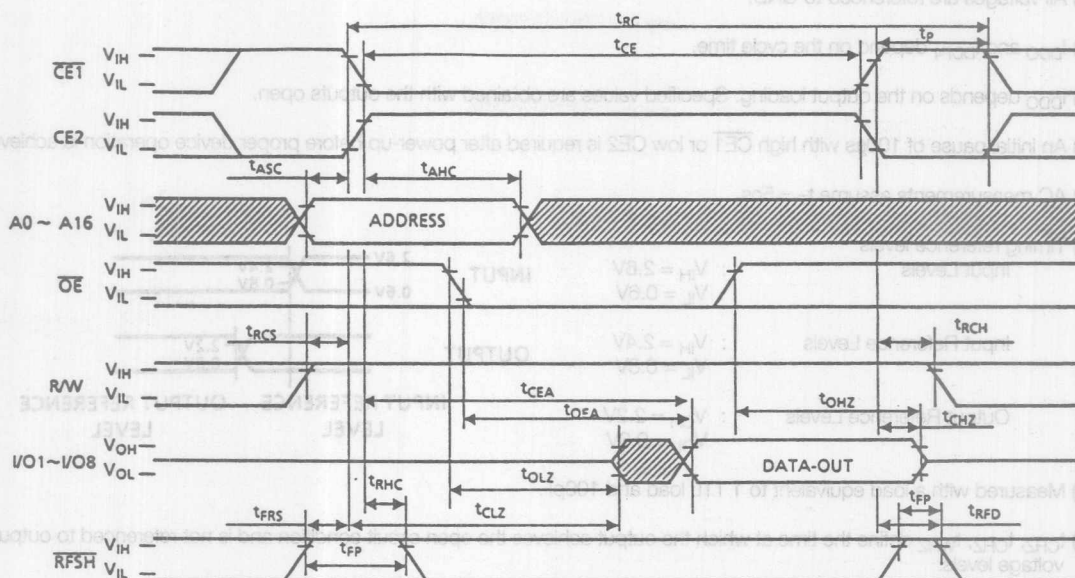


- 14) The timings, t_{CES} (min.) and t_{CEH} (min.) must be met when using $\overline{CE1}$ and CE2 as shown below.

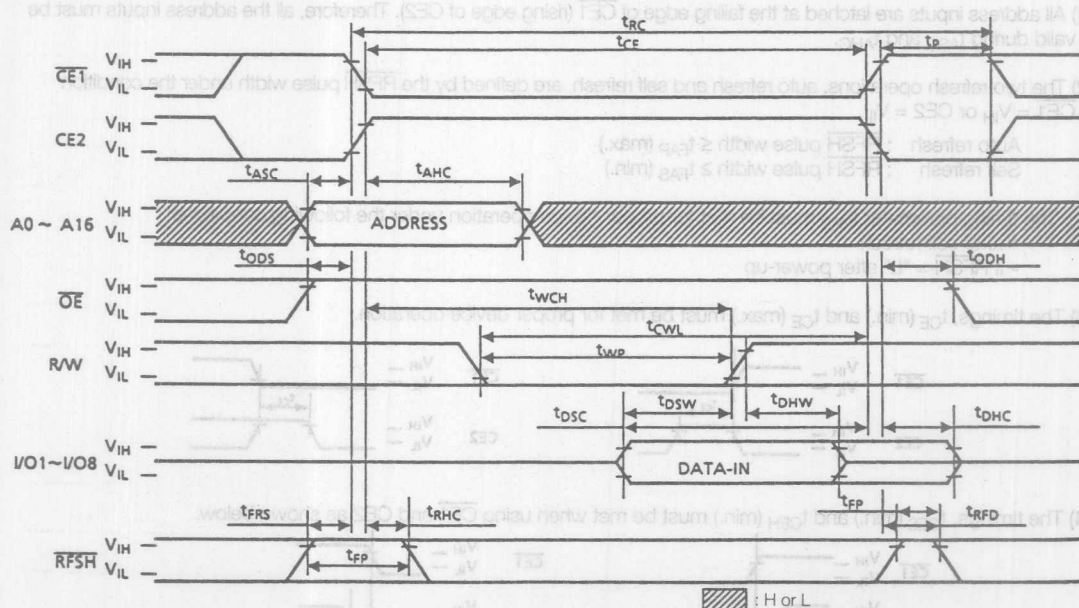


Timing Waveforms

Read Cycle

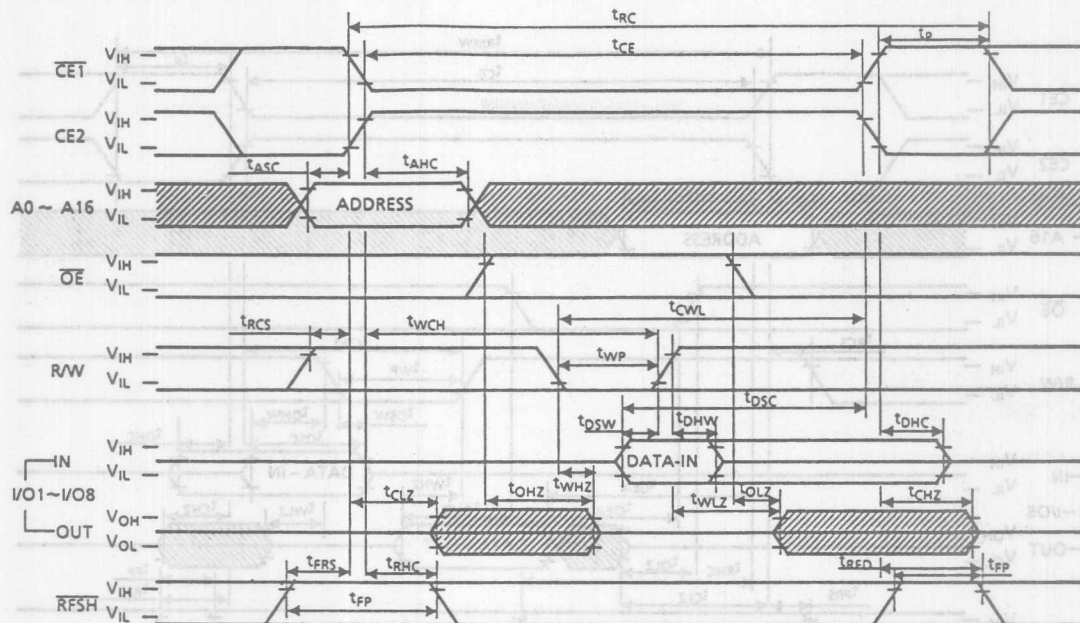


Write Cycle 1 (\overline{OE} Fixed High)

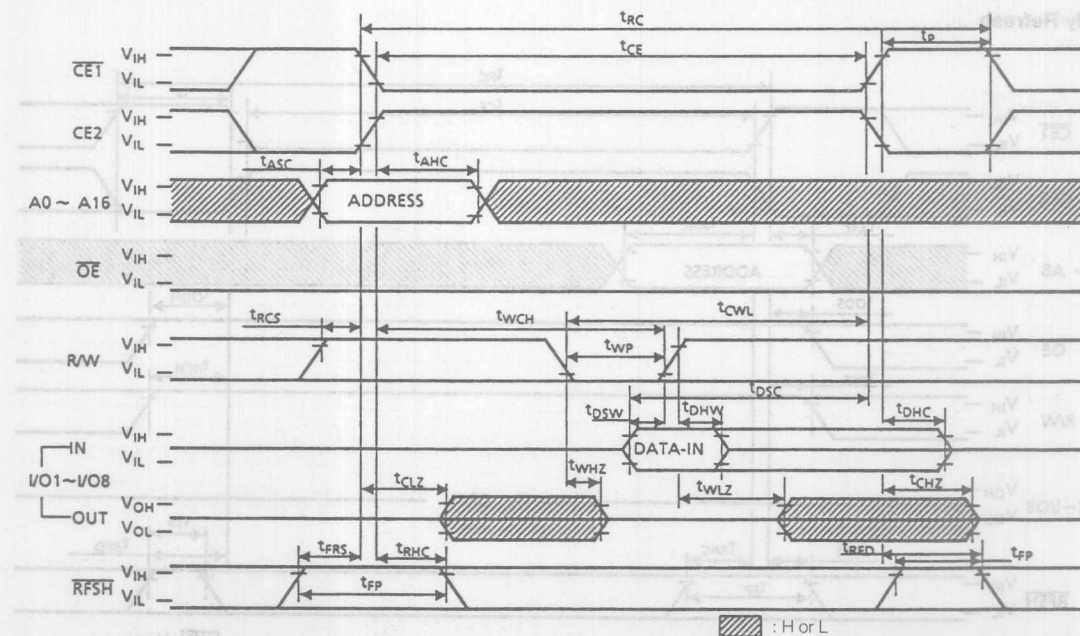


Note: The device can be operated by cycling $\overline{CE1}$ (or $\overline{CE2}$) only provided that $\overline{CE2}$ (or $\overline{CE1}$) is connected to V_{IH} (or V_{IL}).

Write Cycle 2 ($\overline{\text{OE}}$ Clocked)

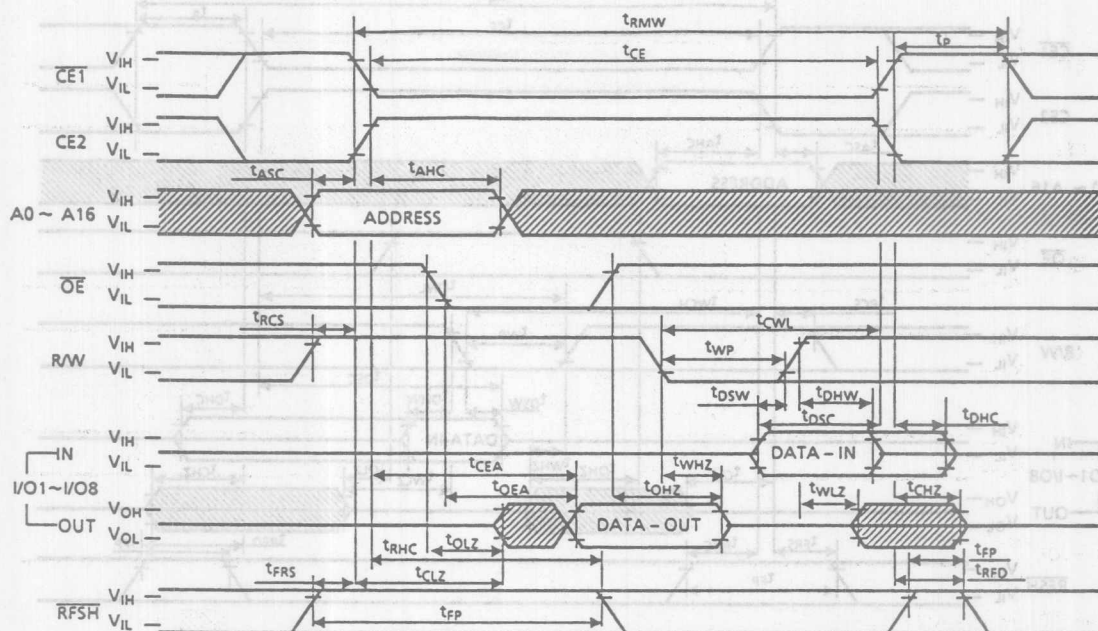


Write Cycle 3 ($\overline{\text{OE}}$ Fixed Low)

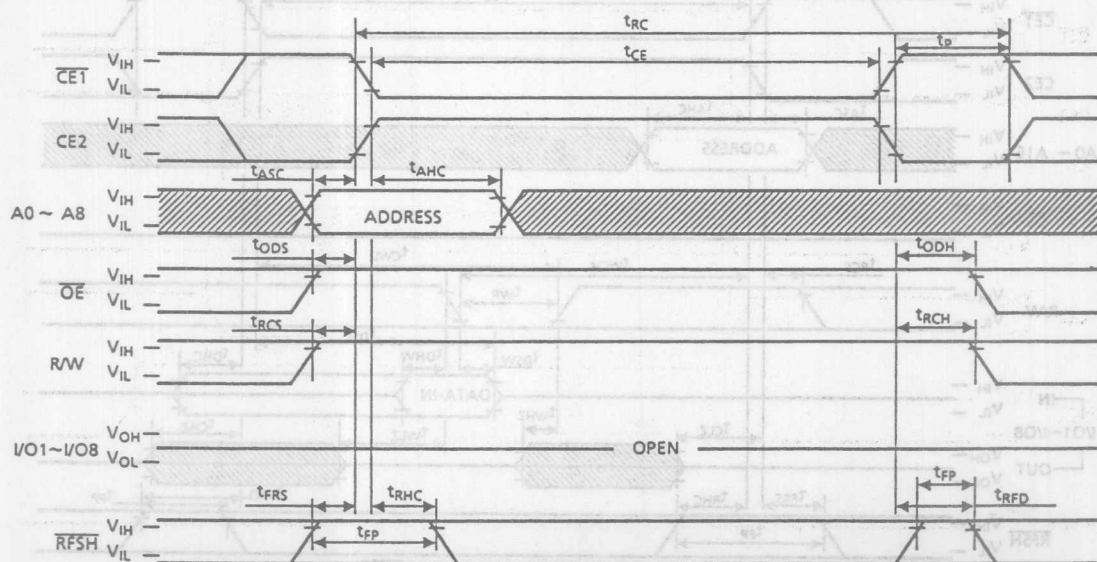


Note: The device can be operated by cycling $\overline{\text{CE1}}$ (or $\overline{\text{CE2}}$) only provided that $\overline{\text{CE2}}$ (or $\overline{\text{CE1}}$) is connected to V_{IH} (or V_{IL}).

Read Modify Write Cycle



CE Only Refresh

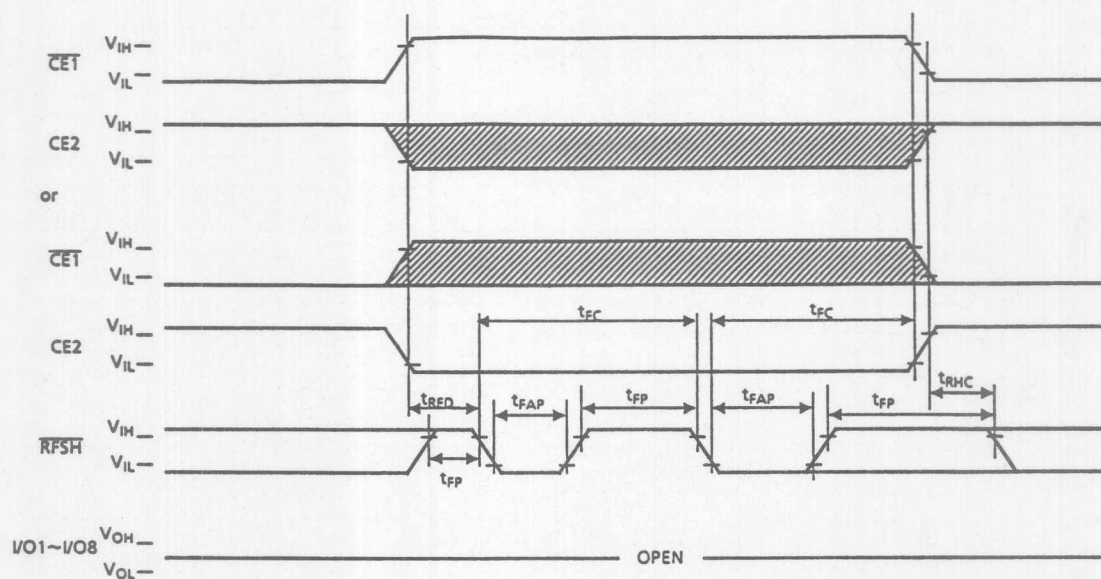


Note : A9 ~ A16 = V_{IH} or V_{IL}

▨ : H or L

Note: The device can be operated by cycling $\overline{CE1}$ (or $\overline{CE2}$) only provided that $\overline{CE2}$ (or $\overline{CE1}$) is connected to V_{IH} (or V_{IL}).

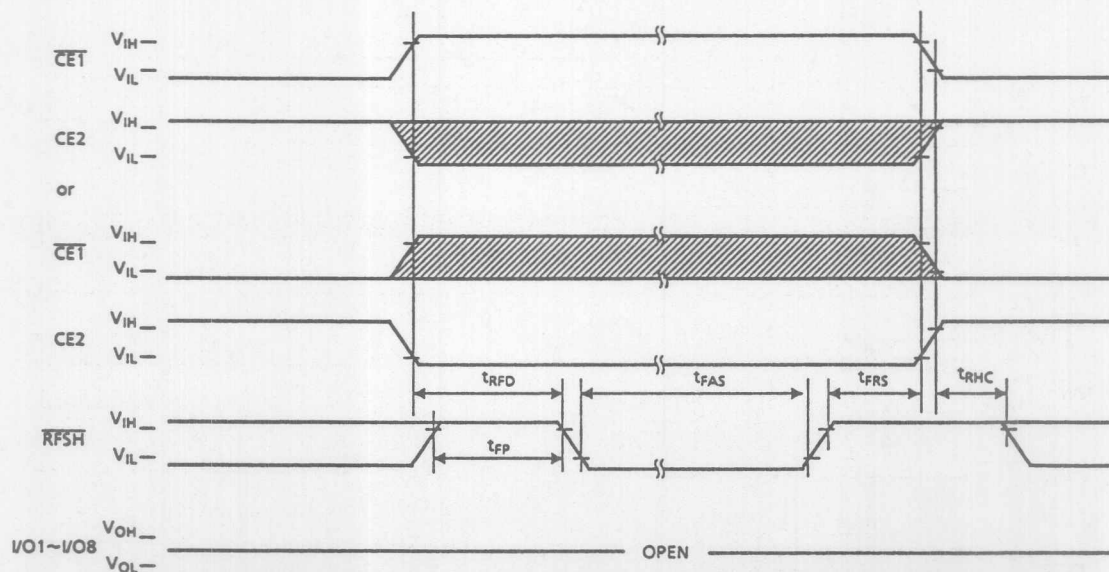
Auto Refresh



Note : \overline{OE} , R/W, A0 ~ A16 = V_{IH} or V_{IL}

■ : H or L

Self Refresh



Note : \overline{OE} , R/W, A0 ~ A16 = V_{IH} or V_{IL}

■ : H or L

TC518129AP/ASP/AF/AFW-80/10/12 TC518129APL/ASPL/AFL/AFWL-80/10/12 TC518129AFTL-80/10/12

SILICON GATE CMOS

131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518129A is a 1M bit high speed CMOS pseudo static RAM organized as 131,072 words by 8 bits. The TC518129A utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518129A operates from a single 5V power supply. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC518129A features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

A CS standby mode interface is incorporated in the TC518129A family, with the CE2 pin in the TC518128A family changed to a CS pin. The TC518129A is available in a 32-pin, 0.6 inch and 0.3 inch width plastic DIP, a small outline plastic flat package, and a 32-pin thin small outline plastic package (forward type).

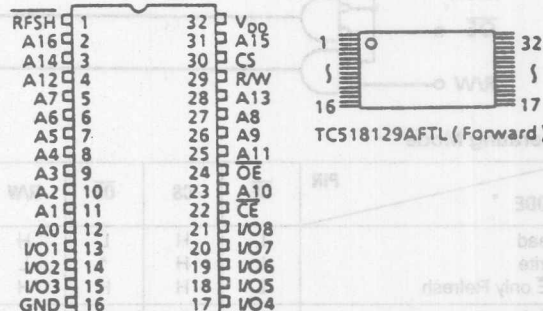
Features

- Organization: 131,072 words x 8 bits
- Single 5V power supply
- Fast access time

	TC518129A Family		
	-80	-10	-12
t _{CEA} \overline{CE} Access Time	80ns	100ns	120ns
t _{OE} \overline{OE} Access Time	35ns	40ns	50ns
t _{RC} Cycle Time	130ns	160ns	190ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	1mA/200 μ A (L version)		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 512 refresh cycles/8ms
- Auto refresh power down feature
- Package
 - TC518129AP/APL : DIP32-P-600
 - TC518129AF/AFL : SOP32-P-450
 - TC518129ASP/ASPL : DIP32-P-300
 - TC518129AFW/AFWL : SOP32-P-525
 - TC518129AFTL : TSOP32-P-0820

Pin Connection (Top View)



TC518129APL / AFL / ASPL / AFWL

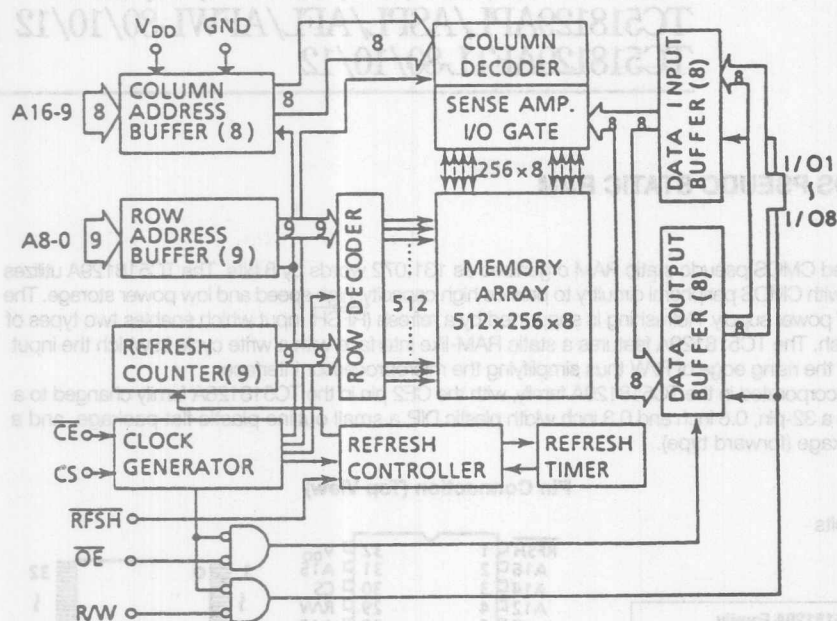
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
RFSH	Refresh Input
\overline{CE}	Chip Enable Input
CS	Chip Select Input
I/O1 ~ I/O8	Data Inputs/Outputs
V _{DD}	Power
GND	Ground

(TSOP)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CS	A ₁₅	V _{DD}	RFSH	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀	\overline{OE}

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	CS	\overline{OE}	R/W	RFSH	A0 ~ A16	I/O1 ~ 8
Read		L	H	L	H	*	V*	OUT
Write		L	H	L	L	*	V*	IN
\overline{CE} only Refresh		L	H	H	H	*	V*	HZ
CS Standby		L	L	*	*	*	*	HZ
Auto/Self Refresh		H	*	*	*	L	*	HZ
Standby		H	*	*	*	H	*	HZ

H = High level input (V_{IH})

L = Low level input (V_{IL})

* = V_{IH} or V_{IL}

V* = At the falling edge of \overline{CE} , all address inputs are latched. At all other times, the address inputs are ***.

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V	
V _{IH}	Input High Voltage	2.4	—	V _{DD} + 1.0	V	2
V _{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I _{DDO}	Operating Current (Average) CE, Address cycling: t _{RC} = t _{RC} min.	80ns version	—	50	70	mA 3,4
		100ns version	—	40	60	
		120ns version	—	35	50	
I _{DDs1}	Standby Current CE = V _{IH} , RFSH = V _{IH}	Normal version	—	—	2	mA
		L version	—	—	1	
I _{DDs2}	Standby Current CE = V _{DD} - 0.2V, RFSH = V _{DD} - 0.2V	Normal version	—	—	1	mA
		L version	—	100	200	
I _{DDF1}	Self Refresh Current (Average) CE = V _{IH} , RFSH = V _{IL}	Normal version	—	—	2	mA
		L version	—	—	1	
I _{DDF2}	Self Refresh Current (Average) CE = V _{DD} - 0.2V, RFSH = 0.2V	Normal version	—	—	1	mA
		L version	—	100	200	
I _{DDF3}	Auto Refresh Current (Average) RFSH cycling: t _{FC} = t _{FC} min	—	—	—	2	mA
I _{DDF4}	CE only Refresh Current (Average) CE, Address cycling: t _{RC} = t _{RC} min.	80ns version	—	50	70	mA 3
		100ns version	—	40	60	
		120ns version	—	35	50	
I _{I(L)}	Input Leakage Current 0V ≤ V _{IN} ≤ V _{DD} , All other Inputs not under test = 0V	—	—	—	±10	μA
I _{O(L)}	Output Leakage Current Output Disabled (CE = V _{IH} or OE = V _{IH} or R/W = V _{IL}), 0V ≤ V _{OUT} ≤ V _{DD}	—	—	—	±10	μA
V _{OH}	Output High Level I _{OH} = -5mA	2.4	—	—	—	V
V _{OL}	Output Low Level I _{OL} = 4.2mA	—	—	—	0.4	V

Capacitance* (V_{DD} = 5V, Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{I1}	Input Capacitance (A0 ~ A16)	—	5	pF
C _{I2}	Input Capacitance (CE, CS, OE, R/W, RFSH)	—	7	
C _{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	130	—	160	—	190	—		
t_{RMW}	Read Modify Write Cycle Time	195	—	235	—	280	—		
t_{CE}	\overline{CE} Pulse Width	80	10,000	100	10,000	120	10,000		
t_P	\overline{CE} Precharge Time	40	—	50	—	60	—		
t_{CEA}	\overline{CE} Access Time	—	80	—	100	—	120		
t_{OEA}	\overline{OE} Access Time	—	35	—	40	—	50		
t_{CLZ}	\overline{CE} to Output in Low -Z	30	—	30	—	30	—		
t_{OLZ}	\overline{OE} to Output in Low -Z	0	—	0	—	0	—		
t_{WLZ}	Output Active from End of Write	0	—	0	—	0	—		
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35	9	
t_{OHZ}	\overline{OE} Disable to Output in High-Z	0	25	0	30	0	35	9	
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35	9	
t_{ODS}	\overline{OE} Output Disable Setup Time	0	—	0	—	0	—		
t_{ODH}	\overline{OE} Output Disable Hold Time	10	—	10	—	10	—		
t_{RCS}	Read Command Setup Time	0	—	0	—	0	—		
t_{RCH}	Read Command Hold Time	0	—	0	—	0	—		
t_{CSS}	Chip Select Setup Time	0	—	0	—	0	—		
t_{CSH}	Chip Select Hold Time	20	—	25	—	30	—	ns	
t_{WP}	Write Pulse Width	60	—	70	—	85	—		
t_{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000		
t_{CWL}	Write Command to \overline{CE} Lead Time	60	10,000	70	10,000	85	10,000		
t_{DSW}	Data Setup Time from R/W	30	—	35	—	45	—	10	
t_{DSC}	Data Setup Time from \overline{CE}	30	—	35	—	45	—	10	
t_{DHW}	Data Hold Time from R/W	0	—	0	—	0	—	10	
t_{DHC}	Data Hold Time from \overline{CE}	0	—	0	—	0	—	10	
t_{ASC}	Address Setup Time	0	—	0	—	0	—	11	
t_{AHC}	Address Hold Time	20	—	25	—	30	—	11	
t_{RHC}	RFSH Command Hold Time	15	—	15	—	15	—		
t_{FC}	Auto Refresh Cycle Time	130	—	160	—	190	—		
t_{RFD}	RFSH Delay Time from \overline{CE}	40	—	50	—	60	—		
t_{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	12	
t_{FP}	RFSH Precharge Time	30	—	30	—	30	—	12	
t_{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—	12	
t_{FRS}	\overline{CE} Delay Time from RFSH (Self Refresh)	160	—	190	—	225	—	12	
t_{REF}	Refresh Period (512 cycles, A0 ~ A8)	—	8	—	8	—	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

Notes:

- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DD0} and I_{DDF4} depend on the cycle time.
- 4) I_{DD0} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

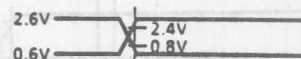
7) Timing reference levels

Input Levels

$$: V_{IH} = 2.6V$$

$$V_{IL} = 0.6V$$

INPUT

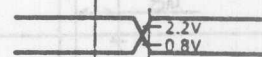


Input Reference Levels

$$: V_{IH} = 2.4V$$

$$V_{IL} = 0.8V$$

OUTPUT



Output Reference Levels

$$: V_{OH} = 2.2V$$

$$V_{OL} = 0.8V$$

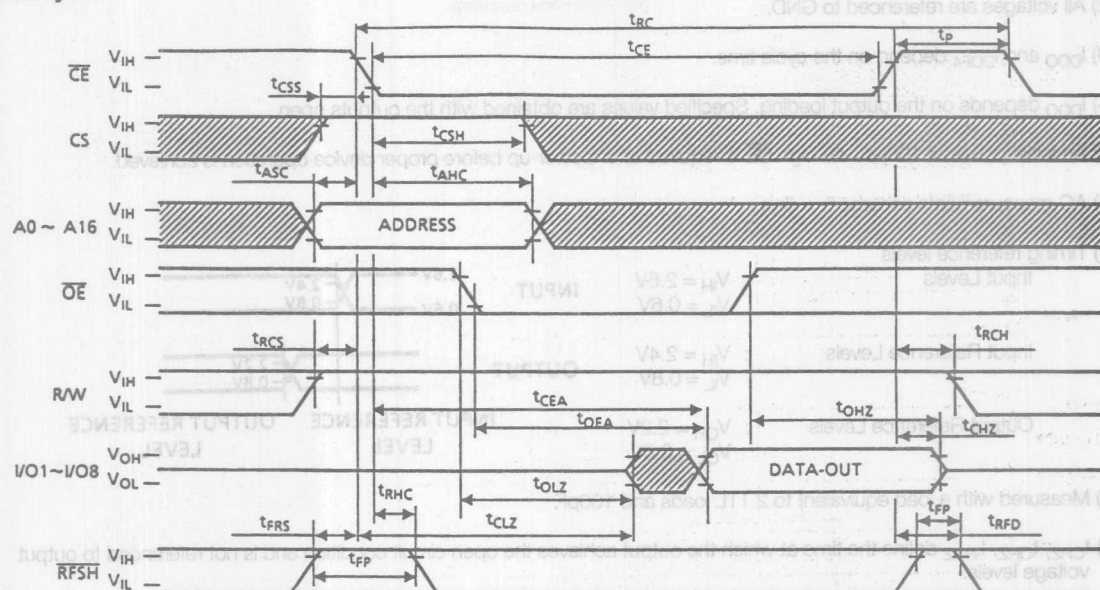
INPUT REFERENCE
LEVELOUTPUT REFERENCE
LEVEL

- 8) Measured with a load equivalent to 2 TTL loads and 100pF.
- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) For write cycles, the input data is latched at the earlier of R/W or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
- 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.
Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

- after self refresh
- if $\overline{RFSH} = "L"$ after power-up

Read Cycle

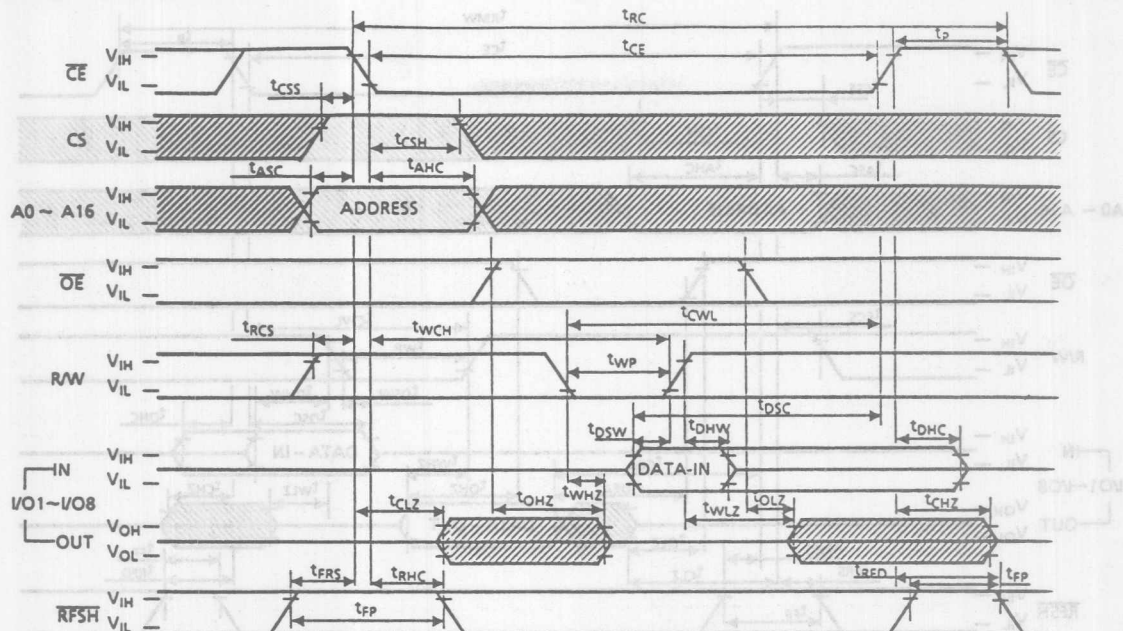


The timing diagram illustrates the relationship between several signals and their timing parameters:

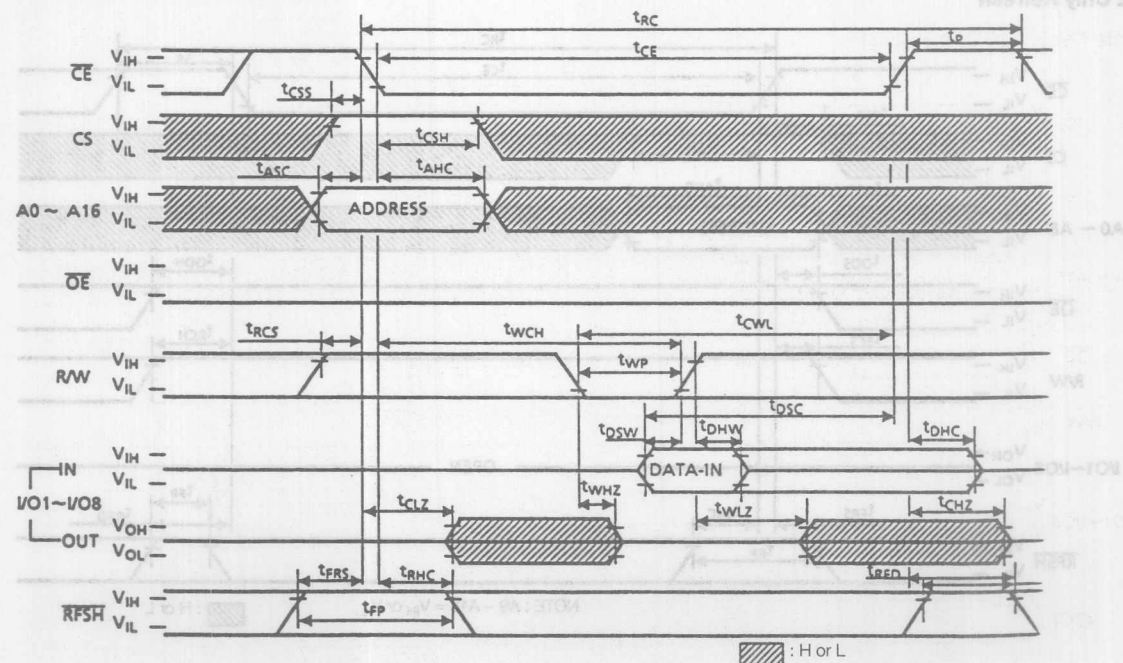
- CE (Chip Enable):** Shows setup time t_{CSS} before the clock edge and hold time t_{CH} after the clock edge. The total delay from clock to output is t_{CF} .
- CS (Chip Select):** Shows setup time t_{SCS} before the clock edge and hold time t_{SCH} after the clock edge.
- A0 ~ A16 (Address):** Shows setup time t_{ASC} before the clock edge and hold time t_{AHC} after the clock edge.
- OE (Output Enable):** Shows setup time t_{OS} before the clock edge and hold time t_{OH} after the clock edge.
- RW (Read/Write):** Shows setup time t_{WCH} before the clock edge and hold time t_{WH} after the clock edge.
- VO1 ~ VO8 (Data-In):** Shows setup time t_{DSC} before the clock edge, data setup time t_{DSW} , data hold time t_{DHW} , and output hold time t_{OHC} .
- RFSH (Refresh):** Shows refresh setup time t_{FRS} before the clock edge and refresh hold time t_{RHC} after the clock edge.

Legend: H or L (High or Low)

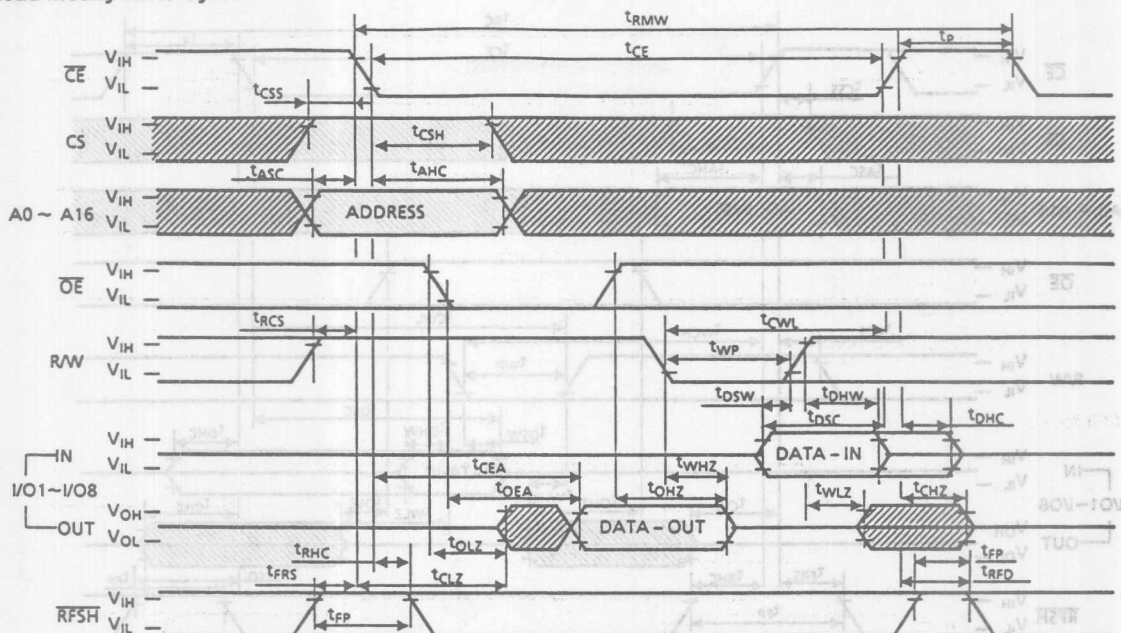
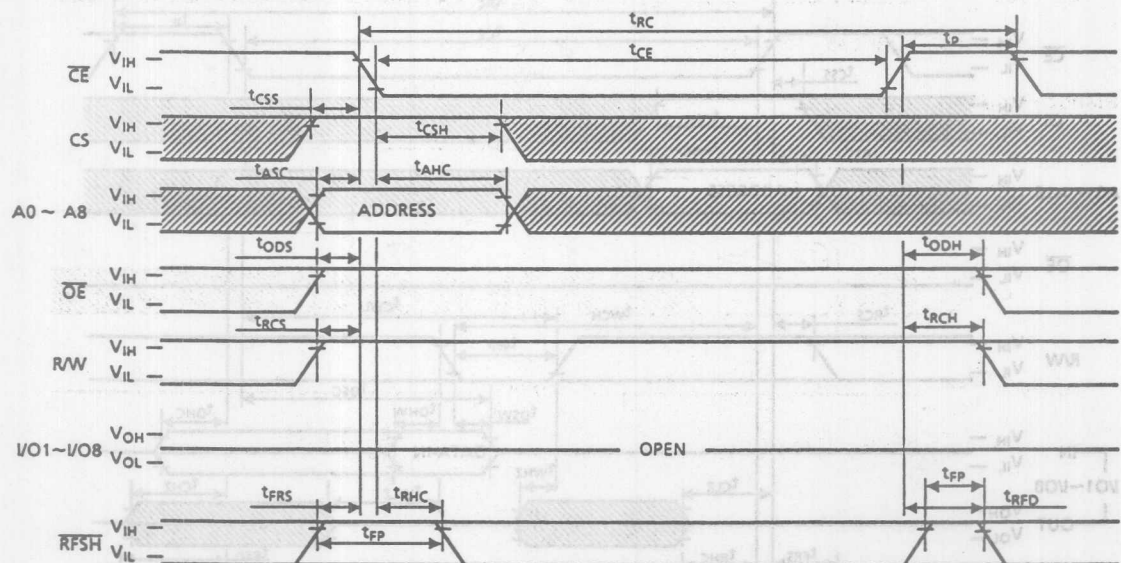
Write Cycle 2 (\overline{OE} Clocked)



Write Cycle 3 (\overline{OE} Fixed Low)

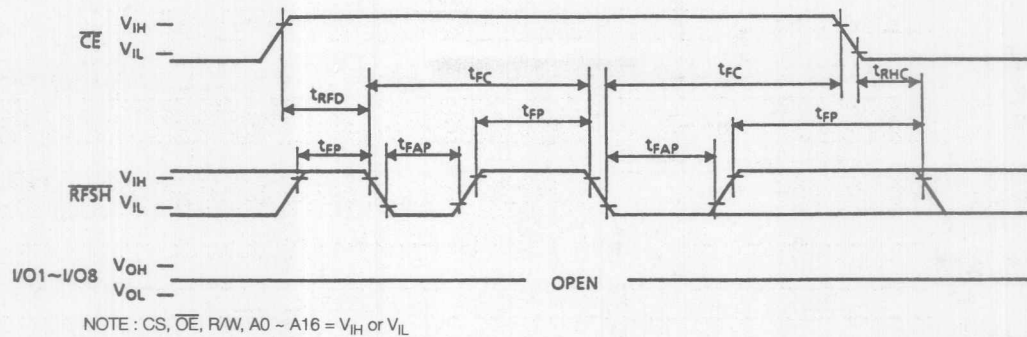


Read Modify Write Cycle

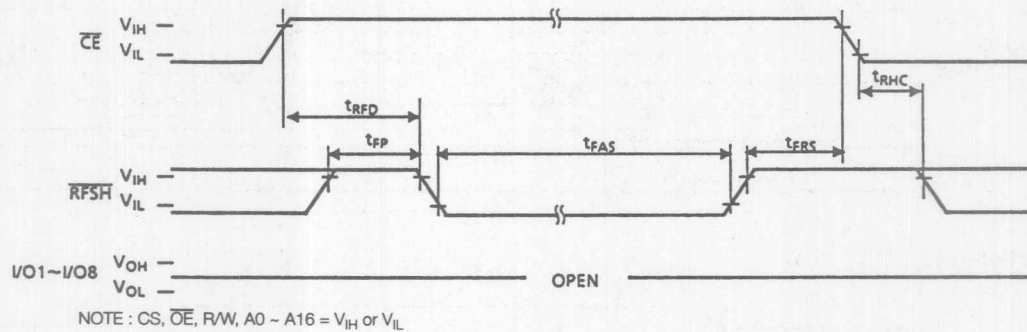
 \overline{CE} Only RefreshNOTE : A9 ~ A16 = V_{IH} or V_{IL}

: H or L

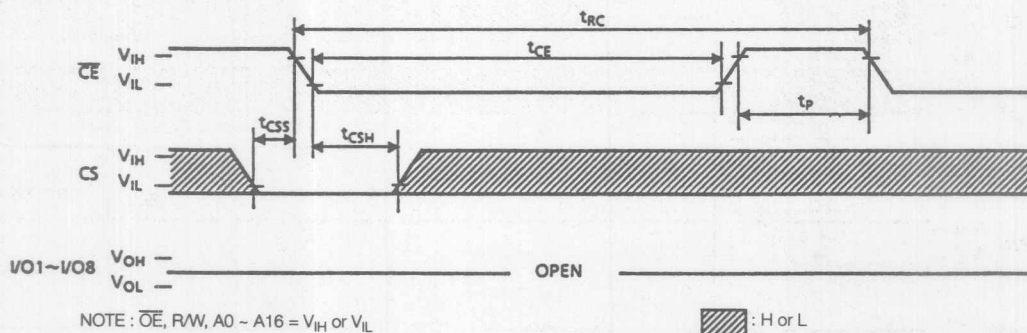
Auto Refresh



Self Refresh



CS Standby Mode



Notes

TC518129APL/AFL/AFWL-80LV/10LV/12LV TC518129AFTL-80LV/10LV/12LV

SILICON GATE CMOS

131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518129A-LV is a 1M bit high speed CMOS pseudo static RAM organized as 131,072 words by 8 bits. The TC518129A-LV utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518129A-LV operates from a single power supply of 3.135V ~ 5.5V. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC518129A-LV features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

A CS standby mode interface is incorporated in the TC518129A-LV family, with the CE2 pin in the TC518128A-LV family changed to a CS pin. The TC518129A-LV is available in a 32-pin, 0.6 inch width plastic DIP, a small outline plastic flat package, and a 32-pin thin small outline plastic package (forward type).

Features

- Organization: 131,072 words x 8 bits
- Low voltage operation: 3.135V ~ 5.5V
- Data retention supply voltage: 3.0V ~ 5.5V
- Fast access time

	TC518129A-LV Family		
	-80	-10	-12
t _{CEA} \overline{CE} Access Time	80ns	100ns	120ns
t _{OEa} \overline{OE} Access Time	35ns	40ns	50ns
t _{RC} Cycle Time	130ns	160ns	190ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	5.5V	200μA	
	3.0V	100μA	

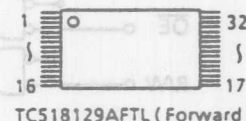
- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 512 refresh cycles/8ms
- Auto refresh power down feature
- Package
 - TC518129APL: DIP32-P-600
 - TC518129AFL: SOP32-P-450
 - TC518129AFWL: SOP32-P-525
 - TC518129AFTL: TSOP32-P-0820

(TSOP)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CS	A ₁₅	V _{DD}	RFSH	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀	\overline{OE}

Pin Connection (Top View)

RFSH	1	32	V _{DD}
A16	2	31	A15
A14	3	30	CS
A12	4	29	R/W
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	\overline{OE}
A2	10	23	A10
A1	11	22	\overline{CE}
A0	12	21	I/O8
I/O1	13	20	I/O7
I/O2	14	19	I/O6
I/O3	15	18	I/O5
GND	16	17	I/O4



TC518129APL/AFL/AFWL

Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
RFSH	Refresh Input
\overline{CE}	Chip Enable Input
CS	Chip Select Input
I/O1 ~ I/O8	Data Inputs/Outputs
V _{DD}	Power
GND	Ground

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1.0$	V	
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC \min}$.	80ns version	—	50	70	3, 4
		100ns version	—	40	60	
		120ns version	—	35	50	
I_{DDs1}	Standby Current $\overline{CE} = V_{IH}$, $RFSH = V_{IH}$	—	—	1	—	mA
I_{DDs2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$, $RFSH = V_{DD} - 0.2V$	—	100	200	—	μA
I_{DDF1}	Self Refresh Current (Average) $\overline{CE} = V_{IH}$, $RFSH = V_{IL}$	—	—	1	—	mA
I_{DDF2}	Self Refresh Current (Average) $\overline{CE} = V_{DD} - 0.2V$, $RFSH = 0.2V$	—	100	200	—	μA
I_{DDF3}	Auto Refresh Current (Average) $RFSH$ cycling: $t_{FC} = t_{FC \min}$	—	—	2	—	mA
I_{DDF4}	\overline{CE} only Refresh Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC \min}$.	80ns version	—	50	70	3
		100ns version	—	40	60	
		120ns version	—	35	50	
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other inputs not under test = $0V$	—	—	± 10	—	μA
$I_{O(L)}$	Output Leakage Current Output Disabled ($\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $R/W = V_{IL}$), $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	—	μA
V_{OH}	Output High Level $I_{OH} = -5mA$	2.4	—	—	—	V
V_{OL}	Output Low Level $I_{OL} = 4.2mA$	—	—	0.4	—	V

Capacitance* ($V_{DD} = 5V$, $T_a = 25^\circ\text{C}$, $f = 1MHz$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	—	5	pF
C_{I2}	Input Capacitance (\overline{CE} , CS, \overline{OE} , R/W, $RFSH$)	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	130	—	160	—	190	—		
t _{RMW}	Read Modify Write Cycle Time	195	—	235	—	280	—		
t _{CE}	\overline{CE} Pulse Width	80	10,000	100	10,000	120	10,000		
t _p	\overline{CE} Precharge Time	40	—	50	—	60	—		
t _{CEA}	\overline{CE} Access Time	—	80	—	100	—	120		
t _{OEa}	\overline{OE} Access Time	—	35	—	40	—	50		
t _{CLZ}	\overline{CE} to Output in Low -Z	30	—	30	—	30	—		
t _{OLZ}	\overline{OE} to Output in Low -Z	0	—	0	—	0	—		
t _{WLZ}	Output Active from End of Write	0	—	0	—	0	—		
t _{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35	9	
t _{OHZ}	\overline{OE} Disable to Output in High-Z	0	25	0	30	0	35	9	
t _{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35	9	
t _{ODS}	\overline{OE} Output Disable Setup Time	0	—	0	—	0	—		
t _{ODH}	\overline{OE} Output Disable Hold Time	10	—	10	—	10	—		
t _{RCS}	Read Command Setup Time	0	—	0	—	0	—		
t _{RCH}	Read Command Hold Time	0	—	0	—	0	—		
t _{CSS}	Chip Select Setup Time	0	—	0	—	0	—	ns	
t _{CSH}	Chip Select Hold Time	20	—	25	—	30	—		
t _{WP}	Write Pulse Width	60	—	70	—	85	—		
t _{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000		
t _{CWL}	Write Command to \overline{CE} Lead Time	60	10,000	70	10,000	85	10,000		
t _{DSW}	Data Setup Time from R/W	30	—	35	—	45	—	10	
t _{DSC}	Data Setup Time from \overline{CE}	30	—	35	—	45	—	10	
t _{DHW}	Data Hold Time from R/W	0	—	0	—	0	—	10	
t _{DHC}	Data Hold Time from \overline{CE}	0	—	0	—	0	—	10	
t _{ASC}	Address Setup Time	0	—	0	—	0	—	11	
t _{AHC}	Address Hold Time	20	—	25	—	30	—	11	
t _{RHC}	RFSH Command Hold Time	15	—	15	—	15	—		
t _{FC}	Auto Refresh Cycle Time	130	—	160	—	190	—		
t _{RFD}	RFSH Delay Time from \overline{CE}	40	—	50	—	60	—		
t _{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	12	
t _{FP}	RFSH Precharge Time	30	—	30	—	30	—	12	
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—	12	
t _{FRS}	\overline{CE} Delay Time from RFSH (Self Refresh)	160	—	190	—	225	—	12	
t _{REF}	Refresh Period (512 cycles, A0 ~ A8)	—	8	—	8	—	8	ms	
t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

3.3V Operation

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	3.135	3.3	3.465	V	2
V_{IH}	Input High Voltage	$V_{DD} - 0.2V$	—	$V_{DD} + 1.0V$	V	
V_{IL}	Input Low Voltage	-0.5	—	0.2	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 3.3V \pm 5\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) CE, Address cycling: $t_{RC} = t_{RC \text{ min.}}$	—	15	20	mA	3,4
I_{DDS2}	Standby Current	—	50	100	μA	
I_{DDF2}	Self Refresh Current (Average)	—	50	100	μA	
I_{DDF3}	Auto Refresh Current (Average) RFSH cycling: $t_{FC} = t_{FC \text{ min}}$	—	—	2	mA	
I_{DDF4}	CE only Refresh Current (Average) CE Address cycling: $t_{RC} = t_{RC \text{ min.}}$	—	15	20	mA	3
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = $0V$	—	—	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable, $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level	$I_{OH} = -1\text{mA}$	2.4	—	—	V
		$I_{OH} = -100\mu\text{A}$	$V_{DD} - 0.2V$	—	—	
V_{OL}	Output Low Level	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
		$I_{OL} = 100\mu\text{A}$	—	—	0.2	

AC Characteristics (Ta = 0 ~ 70°C, VDD = 3.3V±5%) (Notes: 5, 6, 8)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t _{RC}	Random Read, Write Cycle Time	300	—		
t _{RMW}	Read Modify Write Cycle Time	405	—		
t _{CE}	\overline{CE} Pulse Width	200	10,000		
t _p	\overline{CE} Precharge Time	90	—		
t _{CEA}	\overline{CE} Access Time	—	200		
t _{OEa}	\overline{OE} Access Time	—	80		
t _{CLZ}	\overline{CE} to Output in Low -Z	40	—		
t _{OLZ}	\overline{OE} to Output in Low -Z	5	—		
t _{WLZ}	Output Active from End of Write	5	—		
t _{CHZ}	Chip Disable to Output in High-Z	0	50		9
t _{OHZ}	\overline{OE} Disable to Output in High-Z	0	50		9
t _{WHZ}	Write Enable to Output in High-Z	0	50		9
t _{ODS}	\overline{OE} Output Disable Setup Time	0	—		
t _{ODH}	\overline{OE} Output Disable Hold Time	10	—		
t _{RCS}	Read Command Setup Time	0	—		
t _{RCH}	Read Command Hold Time	0	—	ns	
t _{WP}	Write Pulse Width	100	—		
t _{WCH}	Write Command Hold Time	100	10,000		
t _{CWL}	Write Command to \overline{CE} Lead Time	100	10,000		
t _{DSW}	Data Setup Time from R/W	50	—		10
t _{DSC}	Data Setup Time from \overline{CE}	50	—		10
t _{DHW}	Data Hold Time from R/W	0	—		10
t _{DHC}	Data Hold Time from \overline{CE}	0	—		10
t _{ASC}	Address Setup Time	0	—		11
t _{AHC}	Address Hold Time	35	—		11
t _{RHC}	RFSH Command Hold Time	15	—		
t _{FC}	Auto Refresh Cycle Time	300	—		
t _{RFD}	RFSH Delay Time from \overline{CE}	90	—		
t _{FAP}	RFSH Pulse Width (Auto Refresh)	50	8,000		12
t _{FP}	RFSH Precharge Time	50	—		12
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—		12
t _{FRS}	\overline{CE} Delay Time from RFSH (Self Refresh)	300	—		12
t _{REF}	Refresh Period (512 cycles, A0 ~ A8)	—	8	ms	
t _T	Transition Time (Rise and Fall)	3	50	ns	

Timing Reference Levels:

Input Reference Levels: 1.5V/1.5V

Output Reference Levels: 1.5V/1.5V

Notes:

1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.

2) All voltages are referenced to GND.

3) I_{DD0} and I_{DDF4} depend on the cycle time.

4) I_{DD0} depends on the output loading. Specified values are obtained with the outputs open.

5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.

6) AC measurements assume $t_r = 5$ ns.

7) Timing reference levels

Input Levels

: $V_{IH} = 2.6V$

$V_{IL} = 0.6V$

INPUT

Input Reference Levels

: $V_{IH} = 2.4V$

$V_{IL} = 0.8V$

OUTPUT

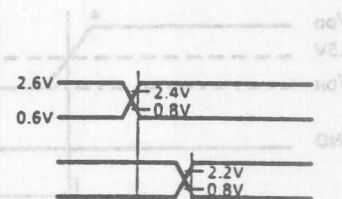
Output Reference Levels

: $V_{OH} = 2.2V$

$V_{OL} = 0.8V$

INPUT REFERENCE
LEVEL

OUTPUT REFERENCE
LEVEL



8) Measured with a load equivalent to 2 TTL loads and 100pF.

9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10) For write cycles, the input data is latched at the earlier of R/W or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).

11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .

12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.

Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)

Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

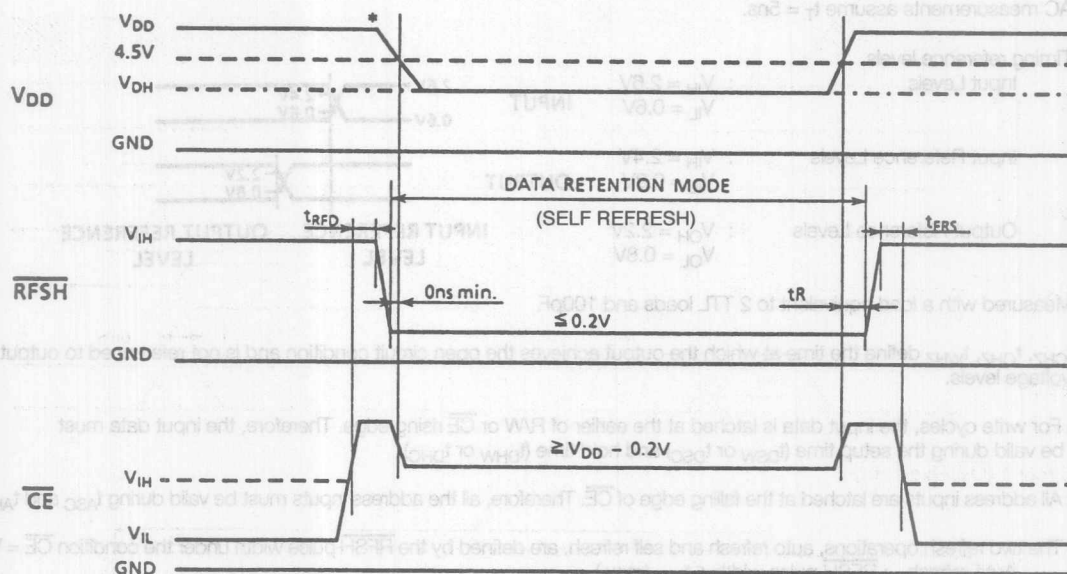
The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

- after self refresh
- if $\overline{RFSH} = "L"$ after power-up

Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	3.0	—	5.5	V
I_{DDF2}	Self Refresh Current	$V_{DH} = 3.0V$	—	40	μA
		$V_{DH} = 5.5V$	—	100	
t_R	Recovery Time	5	—	—	ms

*The falling slope of V_{DD} must be more than 50ms for proper device operation (20ms/V).

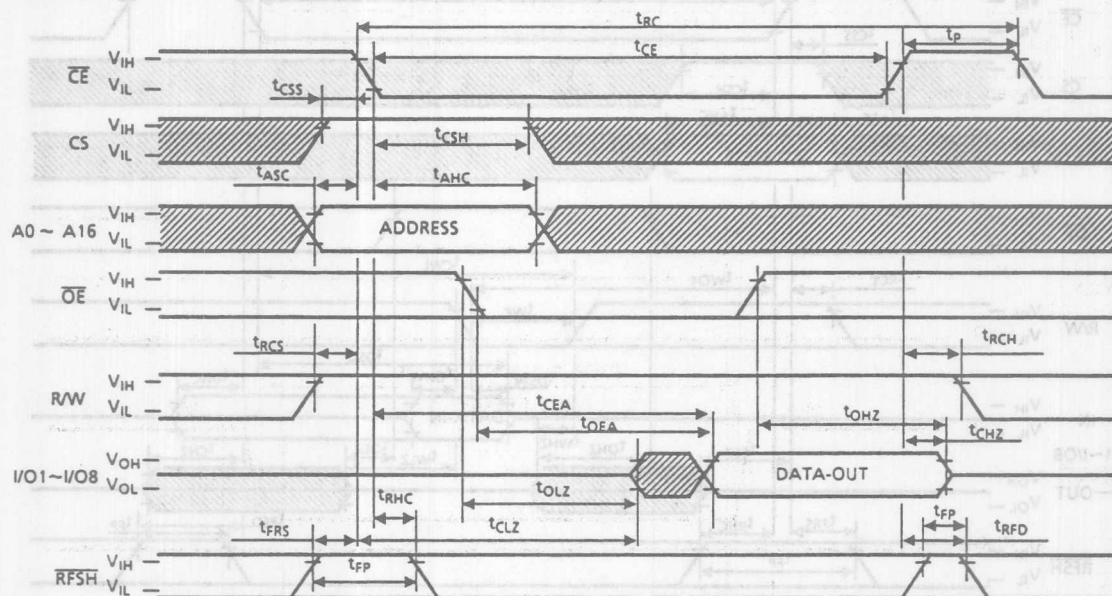


Notes: CS, OE, R/W, A0 ~ A16 = V_{IH} or V_{IL}

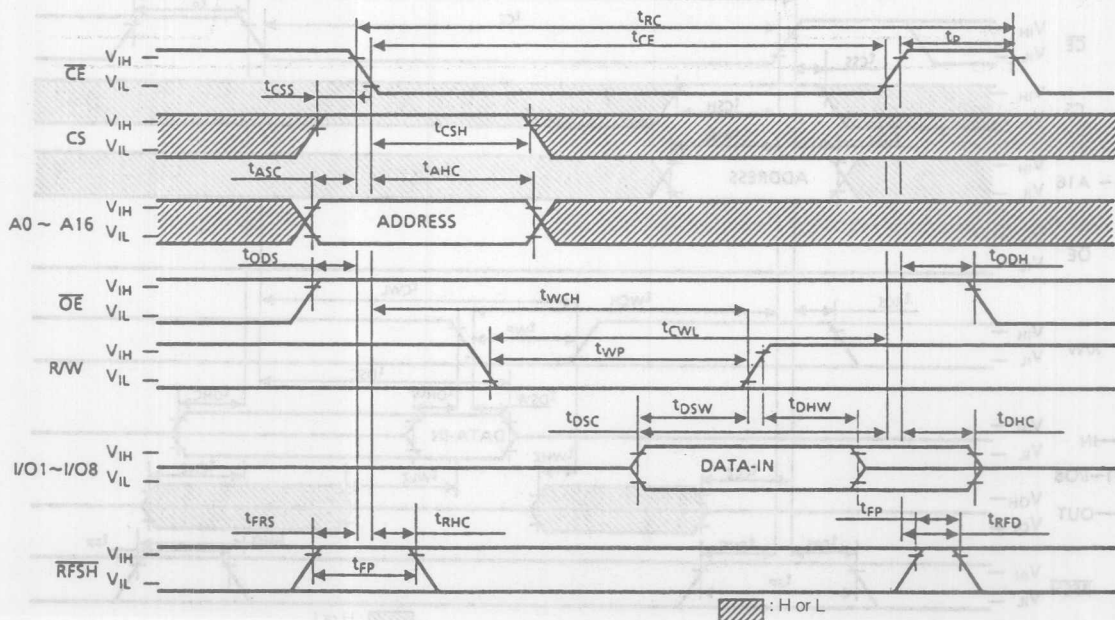
I_{DDF1} is applicable when $RFSH = V_{IL}$ (max.), $\overline{CE} = V_{IH}$ (min.).

Timing Waveforms

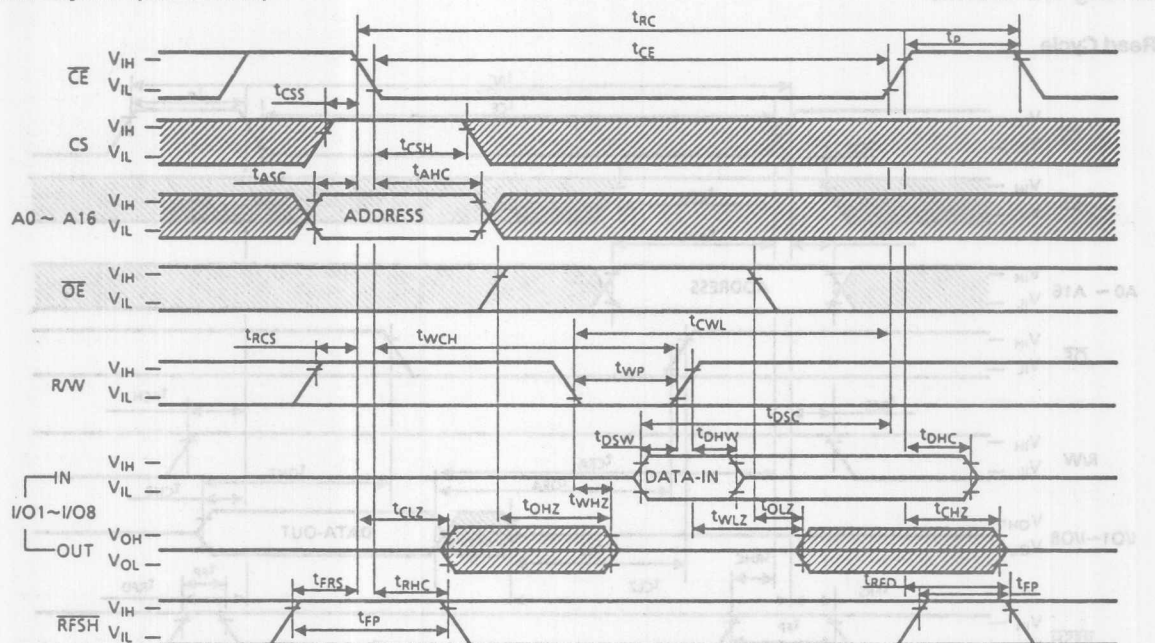
Read Cycle



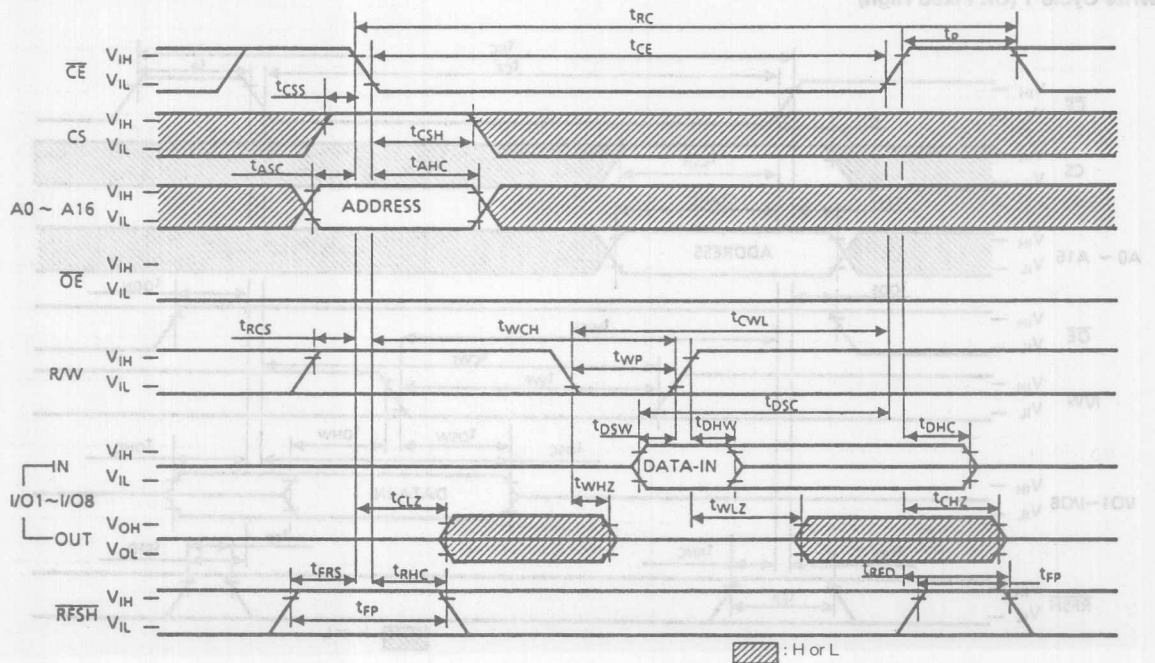
Write Cycle 1 (\overline{OE} Fixed High)



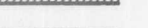
Write Cycle 2 ($\overline{\text{OE}}$ Clocked)



Write Cycle 3 ($\overline{\text{OE}}$ Fixed Low)

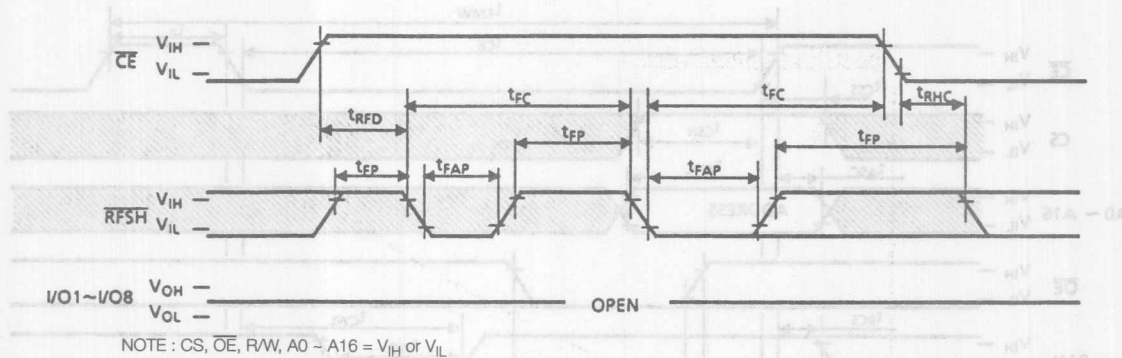


 : H or L

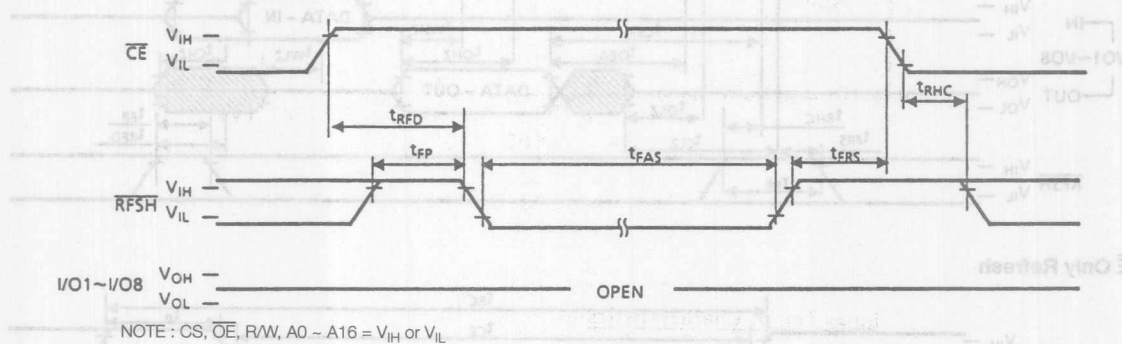


 : H or L

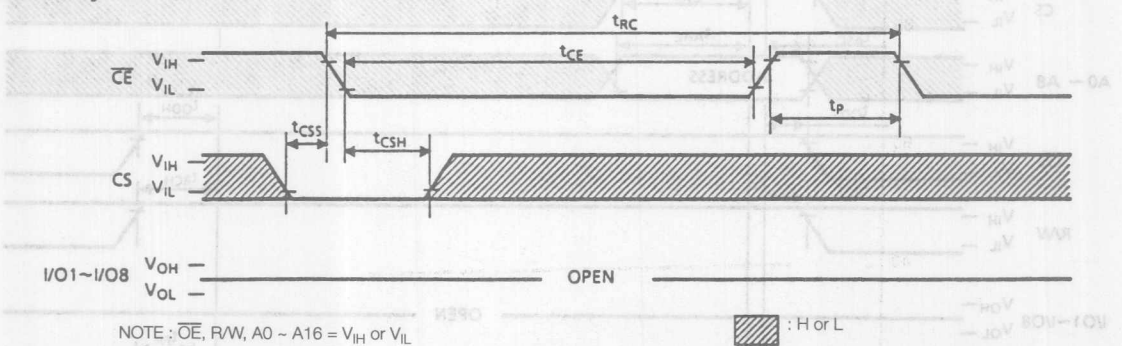
Auto Refresh



Self Refresh

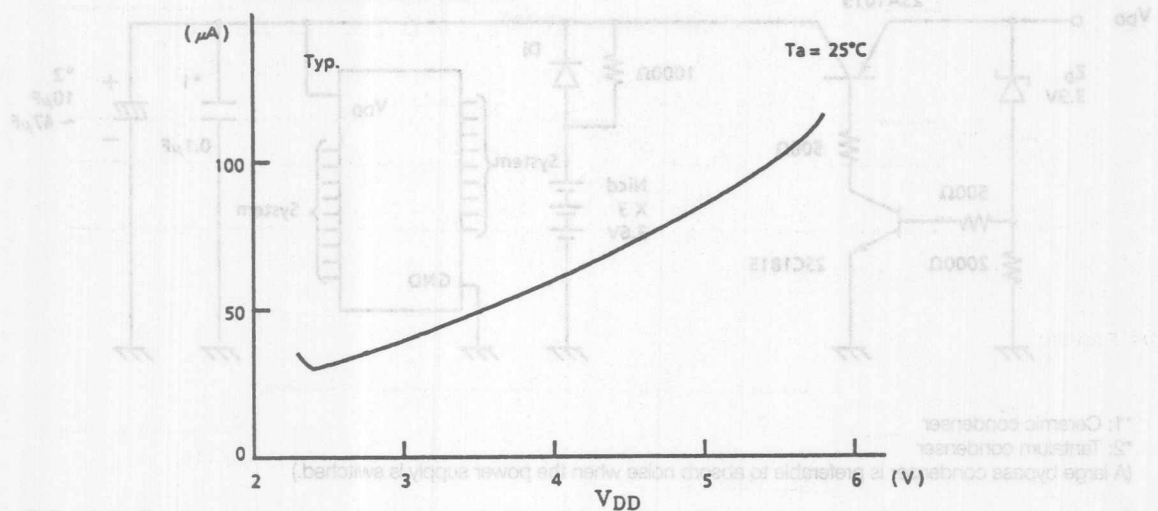


CS Standby Mode

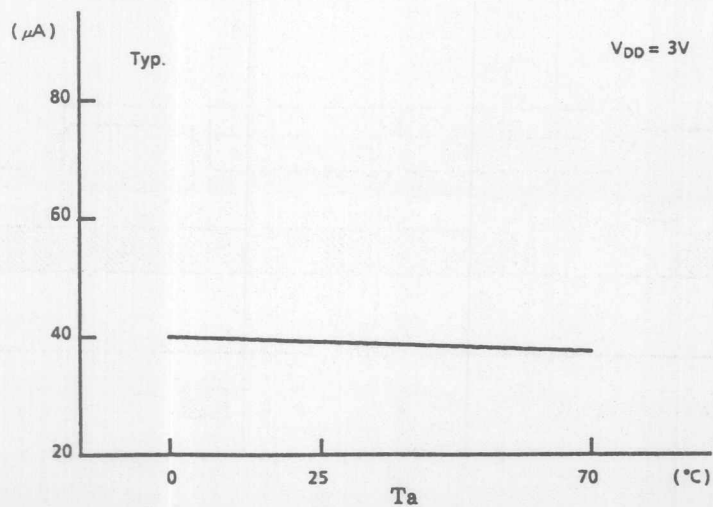


Battery Backup Application Example

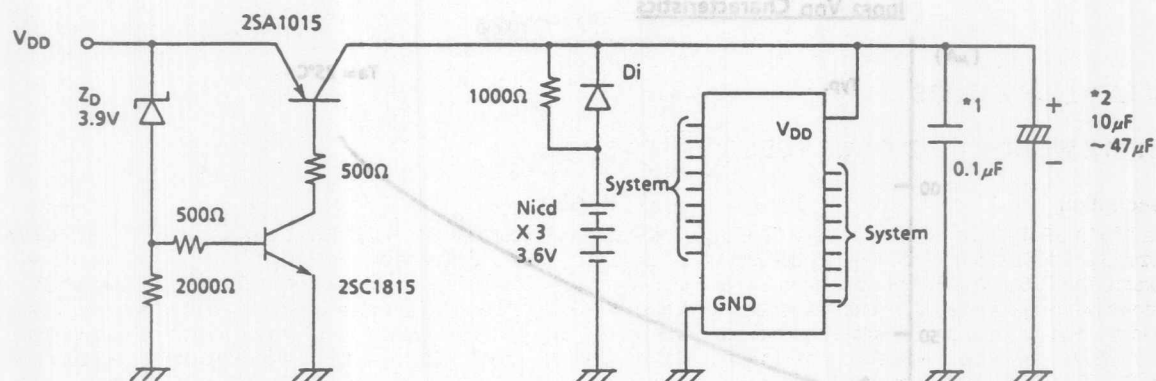
I_{DDF2} V_{DD} Characteristics



I_{DDF2} Temp. Characteristics



Battery Backup Application Example

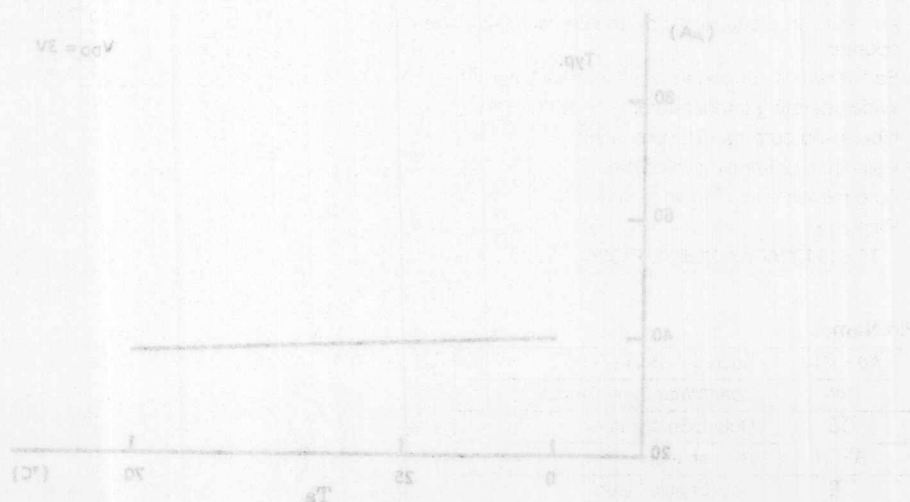


*1: Ceramic condenser

*2: Tantalum condenser

(A large bypass condenser is preferable to absorb noise when the power supply is switched.)

This circuit does not have memory protection. Therefore, rapid turnoff of the power supply must be avoided. Enter the Self Refresh mode before changing to the battery backup power supply.



SILICON GATE CMOS

131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518129AFWI is a 1M bit high speed CMOS pseudo static RAM organized as 131,072 words by 8 bits. The TC518129AFWI utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518129AFWI operates from a single 5V power supply. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC518129AFWI features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

A CS standby mode interface is incorporated in the TC518129AFWI, with the CE2 pin in the TC518128A family changed to a CS pin. The TC518129AFWI is guaranteed over an operating temperature range of -40 ~ 85°C so the TC518129AFWI is suitable for use in wide operating temperature systems. It is available in a 32-pin, 0.525 inch small outline plastic flat package.

Features

- Organization: 131,072 words x 8 bits
- Single 5V power supply
- Fast access time

t_{CEA} \overline{CE} Access Time	100ns
t_{OEA} \overline{OE} Access Time	40ns
t_{RC} Cycle Time	160ns
Power Dissipation	330mW
Self Refresh Current	200 μ A

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Wide operating temperature: -40 ~ 85°C
- Inputs and outputs TTL compatible
- Refresh: 512 refresh cycles/8ms
- Auto refresh power down feature
- Package
 - TC518129AFWI: SOP32-P-525

Pin Connection

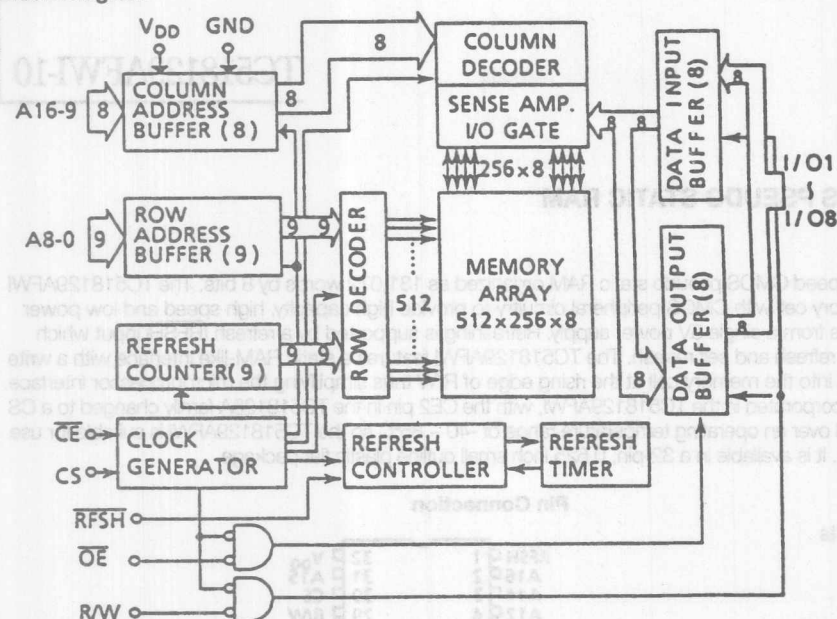
RFSH	1	32	V _{DD}
A16	2	31	A15
A14	3	30	CS
A12	4	29	R/W
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	OE
A2	10	23	A10
A1	11	22	CE
A0	12	21	I/O1
I/O1	13	20	I/O7
I/O1	14	19	I/O6
I/O3	15	18	I/O5
GND	16	17	I/O4

Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
OE	Output Enable Input
RFSH	Refresh Input
CE	Chip Enable Input
CS	Chip Select Input
I/O1 ~ I/O8	Data Inputs/Outputs
V _{DD}	Power
GND	Ground

SYMBOL	ITEM	RATING	UNIT	NOTES
V _{in}	Input Voltage	-1.0 ~ 7.0	V	
V _{out}	Output Voltage	-1.0 ~ 7.0	V	
V _{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T _{opr}	Operating Temperature	-40 ~ 85	°C	
T _{stg}	Storage Temperature	-55 ~ 150	°C	
T _{sol}	Soldering Temperature + Time	250 ~ 10	°C + sec	
P _d	Power Dissipation	300	mW	
I _{out}	Static Circuit Output Current	50	mA	

Block Diagram



Operating Mode

MODE	PIN	CE	CS	OE	R/W	RFSH	A0 ~ A16	I/O1 ~ 8
Read		L	H	L	H	*	V*	OUT
Write		L	H	*	L	*	V*	IN
CE only Refresh		L	H	H	H	*	V*	HZ
CS Standby		L	L	*	*	*	*	HZ
Auto/Self Refresh		H	*	*	*	L	*	HZ
Standby		H	*	*	*	H	*	HZ

H = High level input (V_{IH})L = Low level input (V_{IL})* = V_{IH} or V_{IL} V* = At the falling edge of \overline{CE} , all address inputs are latched. At all other times, the address inputs are ***.

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	-40 ~ 85	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1.0$	V	2
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics ($T_a = -40 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC \min}$.	—	40	60	mA	3,4
I_{DDS1}	Standby Current $\overline{CE} = V_{IH}$, $RFSH = V_{IH}$	—	—	1	mA	
I_{DDS2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$, $RFSH = V_{DD} - 0.2V$	—	100	200	μA	
I_{DDF1}	Self Refresh Current (Average) $\overline{CE} = V_{IH}$, $RFSH = V_{IL}$	—	—	1	mA	
I_{DDF2}	Self Refresh Current (Average) $\overline{CE} = V_{DD} - 0.2V$, $RFSH = 0.2V$	—	100	200	μA	
I_{DDF3}	Auto Refresh Current (Average) $RFSH$ cycling: $t_{FC} = t_{FC \min}$	—	—	2	mA	
I_{DDF4}	\overline{CE} only Refresh Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC \min}$.	—	40	60	mA	3
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = $0V$	—	—	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disabled ($\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $R/W = V_{IL}$), $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level $I_{OH} = -5mA$	2.4	—	—	V	
V_{OL}	Output Low Level $I_{OL} = 4.2mA$	—	—	0.4	V	

Capacitance* ($V_{DD} = 5V$, $T_a = 25^\circ\text{C}$, $f = 1MHz$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	—	5	pF
C_{I2}	Input Capacitance (\overline{CE} , CS, \overline{OE} , R/W, $RFSH$)	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-10		UNIT	NOTES
		MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	160	—		
t _{RMW}	Read Modify Write Cycle Time	235	—		
t _{CE}	$\overline{\text{CE}}$ Pulse Width	100	10,000		
t _p	$\overline{\text{CE}}$ Precharge Time	50	—		
t _{CEA}	$\overline{\text{CE}}$ Access Time	—	100		
t _{OEa}	$\overline{\text{OE}}$ Access Time	—	40		
t _{CLZ}	$\overline{\text{CE}}$ to Output in Low -Z	30	—		
t _{OLZ}	$\overline{\text{OE}}$ to Output in Low -Z	0	—		
t _{WLZ}	Output Active from End of Write	0	—		
t _{CHZ}	Chip Disable to Output in High-Z	0	30		9
t _{OHZ}	$\overline{\text{OE}}$ Disable to Output in High-Z	0	30		9
t _{WHZ}	Write Enable to Output in High-Z	0	30		9
t _{ODS}	$\overline{\text{OE}}$ Output Disable Setup Time	0	—		
t _{ODH}	$\overline{\text{OE}}$ Output Disable Hold Time	10	—		
t _{RCS}	Read Command Setup Time	0	—		
t _{RCH}	Read Command Hold Time	0	—		
t _{CSS}	Chip Select Setup Time	0	—		
t _{CSH}	Chip Select Hold Time	25	—	ns	
t _{WP}	Write Pulse Width	70	—		
t _{WCH}	Write Command Hold Time	70	10,000		
t _{CWL}	Write Command to $\overline{\text{CE}}$ Lead Time	70	10,000		
t _{DSW}	Data Setup Time from R/W	35	—		10
t _{DSC}	Data Setup Time from $\overline{\text{CE}}$	35	—		10
t _{DHW}	Data Hold Time from R/W	0	—		10
t _{DHC}	Data Hold Time from $\overline{\text{CE}}$	0	—		10
t _{ASC}	Address Setup Time	0	—		11
t _{AHC}	Address Hold Time	25	—		11
t _{RHC}	RFSH Command Hold Time	15	—		
t _{FC}	Auto Refresh Cycle Time	160	—		
t _{RFD}	RFSH Delay Time from $\overline{\text{CE}}$	50	—		
t _{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000		12
t _{FP}	RFSH Precharge Time	30	—		12
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—		12
t _{FRS}	$\overline{\text{CE}}$ Delay Time from RFSH (Self Refresh)	190	—		12
t _{REF}	Refresh Period (512 cycles, A0 ~ A8)	—	8	ms	
t _T	Transition Time (Rise and Fall)	3	50	ns	

Notes:

- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DDO} and I_{DDF4} depend on the cycle time.
- 4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

7) Timing reference levels

Input Levels

 $V_{IH} = 2.6V$
 $V_{IL} = 0.6V$

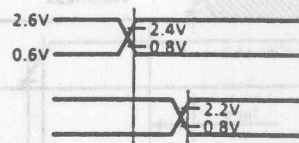
INPUT

Input Reference Levels

 $V_{IH} = 2.4V$
 $V_{IL} = 0.8V$

OUTPUT

Output Reference Levels

 $V_{OH} = 2.2V$
 $V_{OL} = 0.8V$
INPUT REFERENCE
LEVELOUTPUT REFERENCE
LEVEL

- 8) Measured with a load equivalent to 2 TTL loads and 100pF.

- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

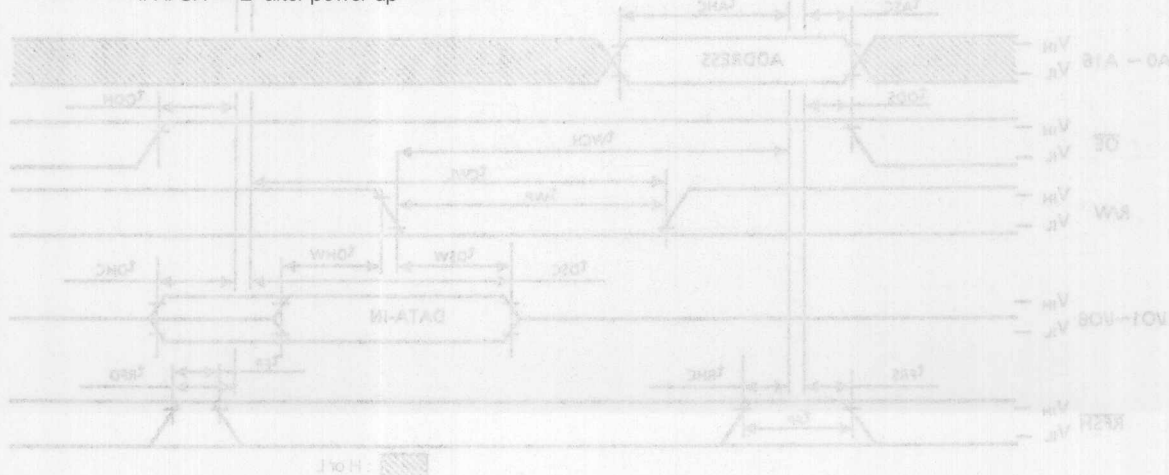
- 10) For write cycles, the input data is latched at the earlier of R/W or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).

- 11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .

- 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.

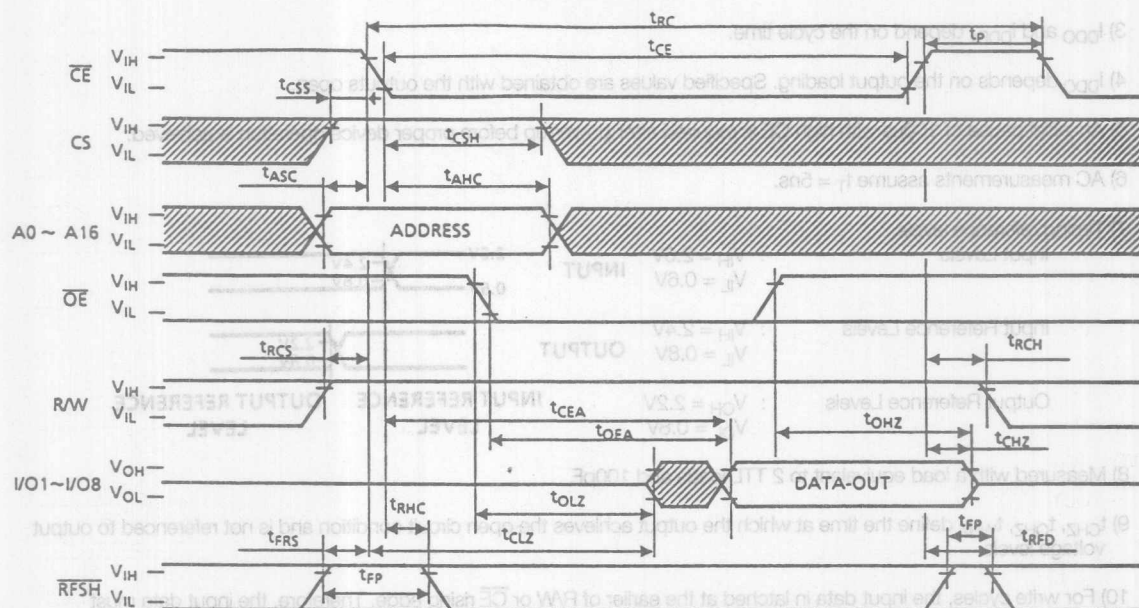
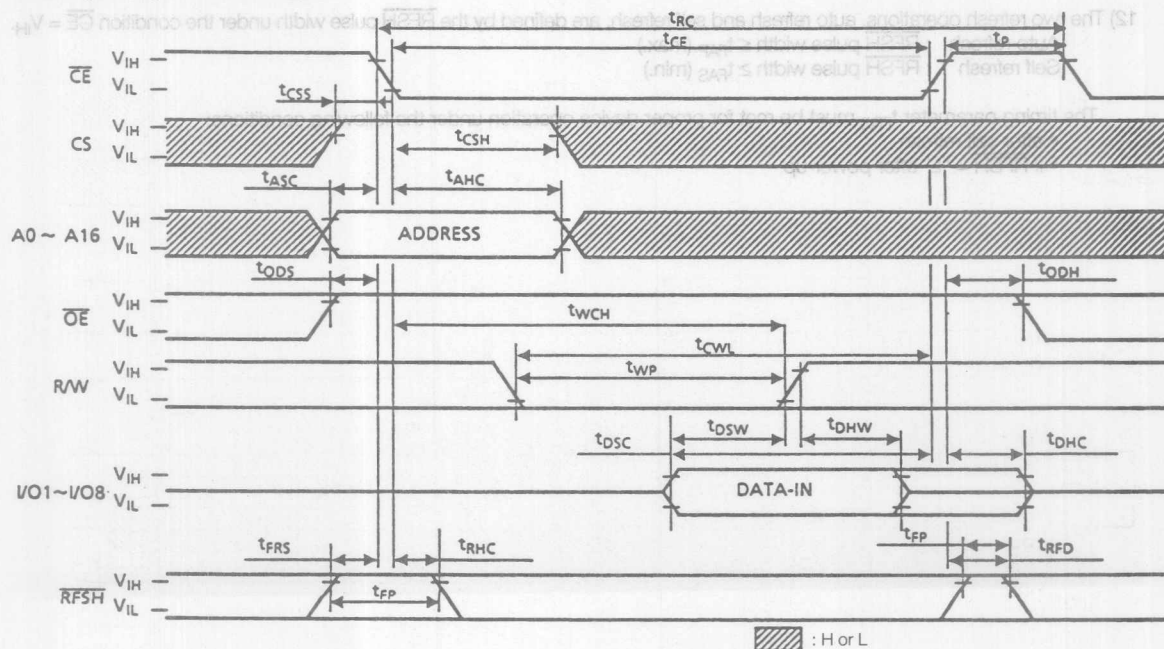
Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

- after self refresh
- if $\overline{RFSH} = "L"$ after power-up

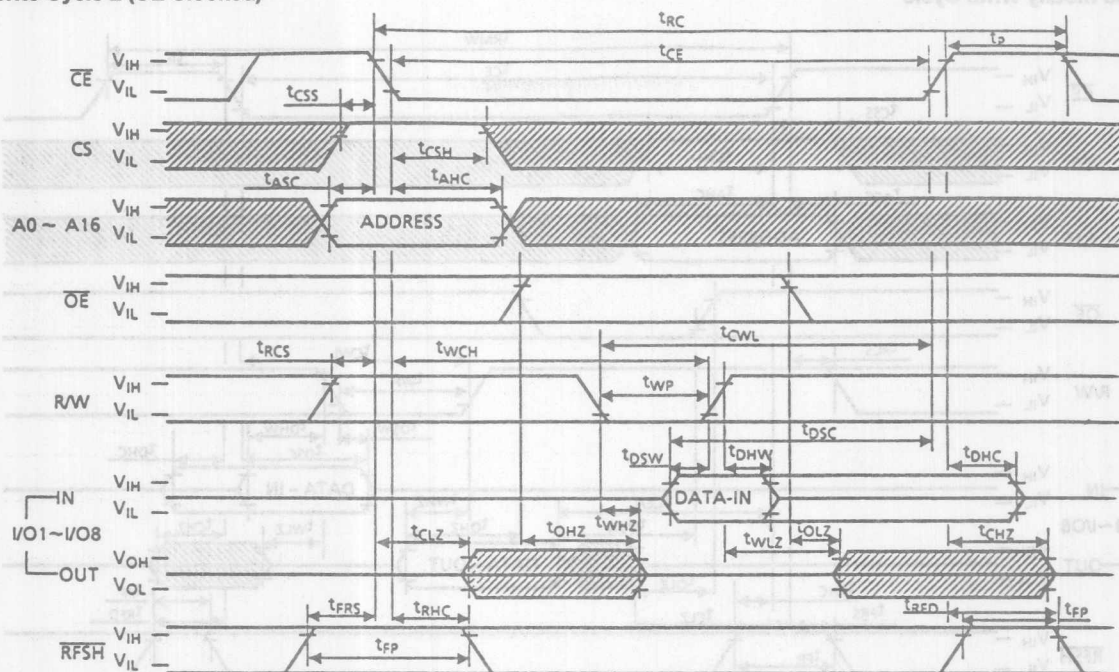
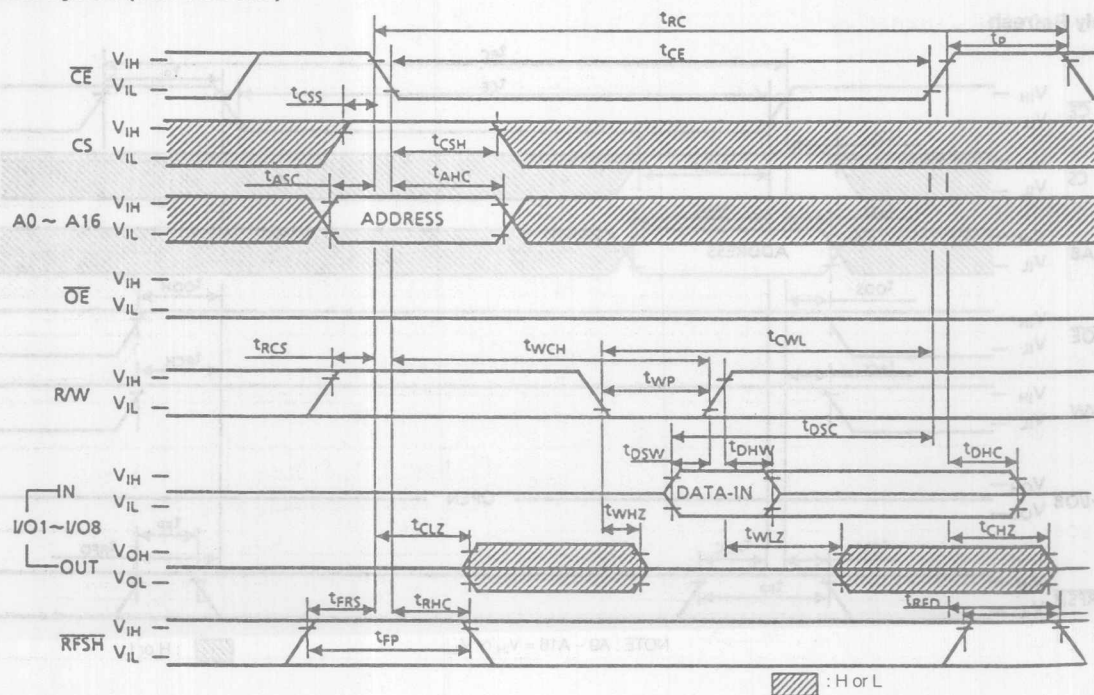


Timing Waveforms

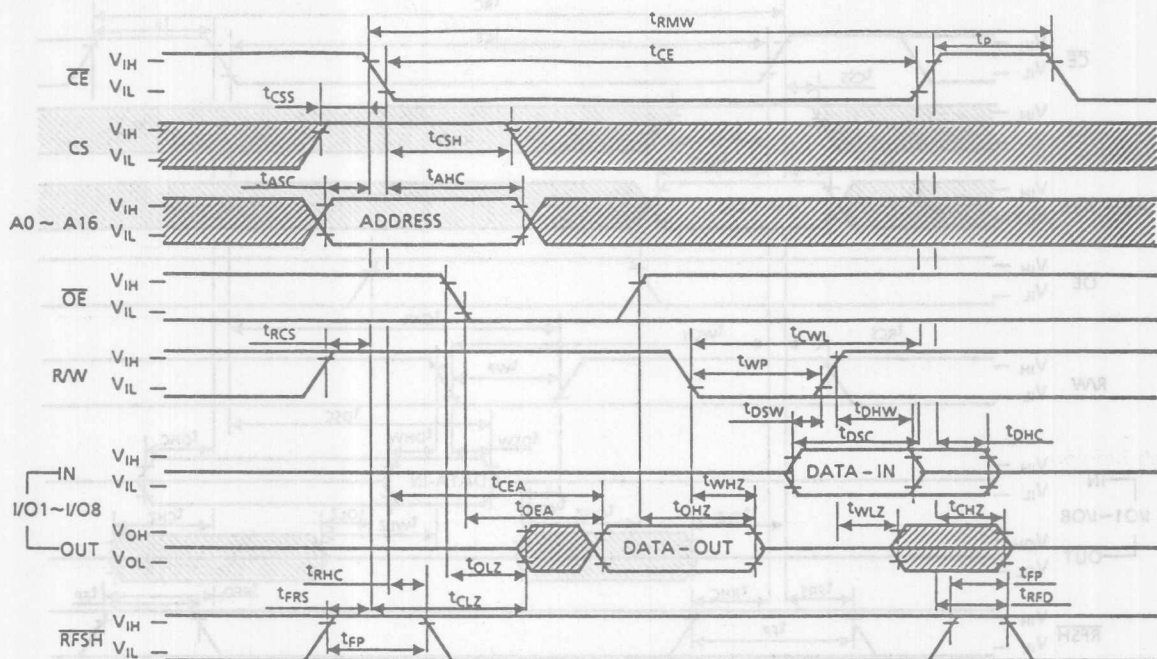
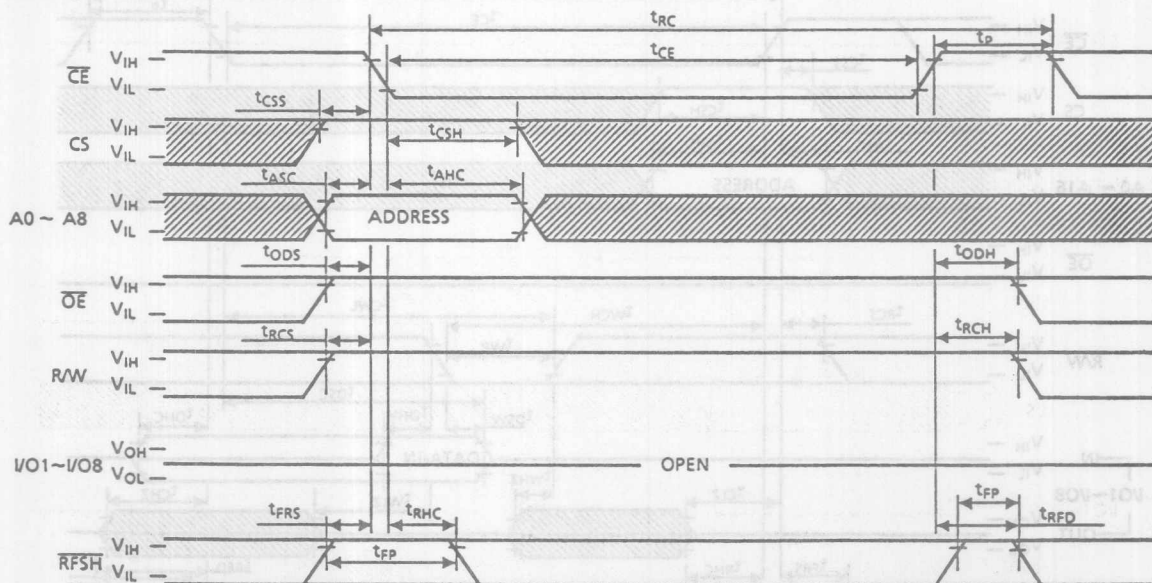
Read Cycle

Write Cycle 1 (\overline{OE} = Fixed High)

▨ : H or L

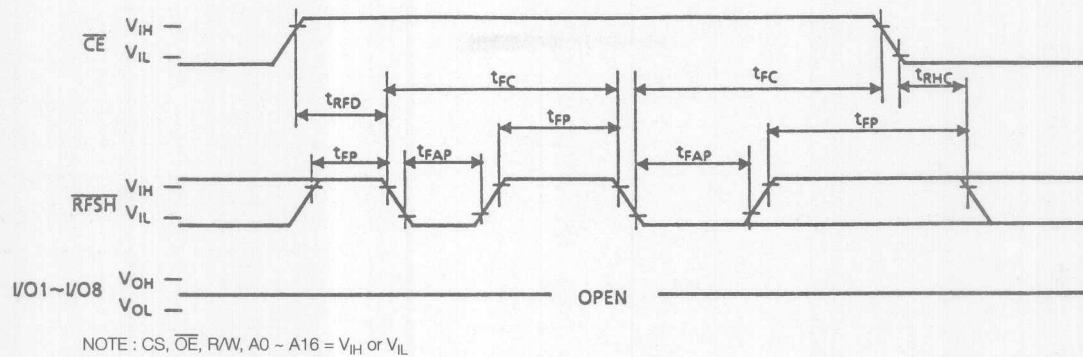
Write Cycle 2 (\overline{OE} Clocked)Write Cycle 3 (\overline{OE} Fixed Low)

Read Modify Write Cycle

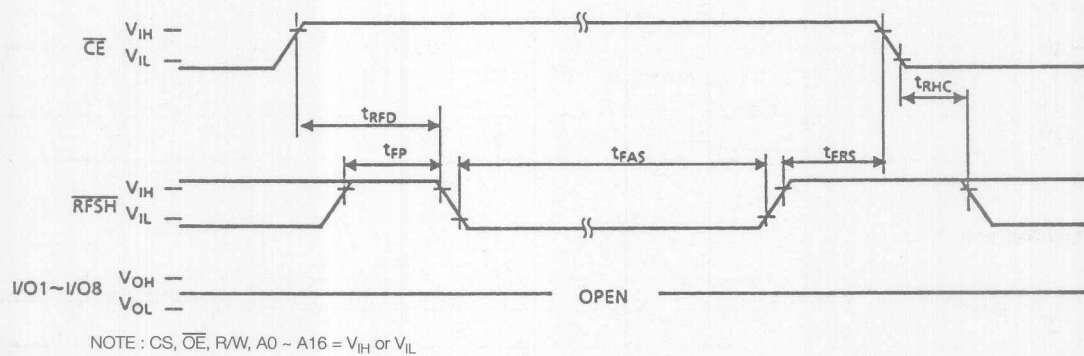
 \overline{CE} Only RefreshNOTE : A9 ~ A16 = V_{IH} or V_{IL}

: H or L

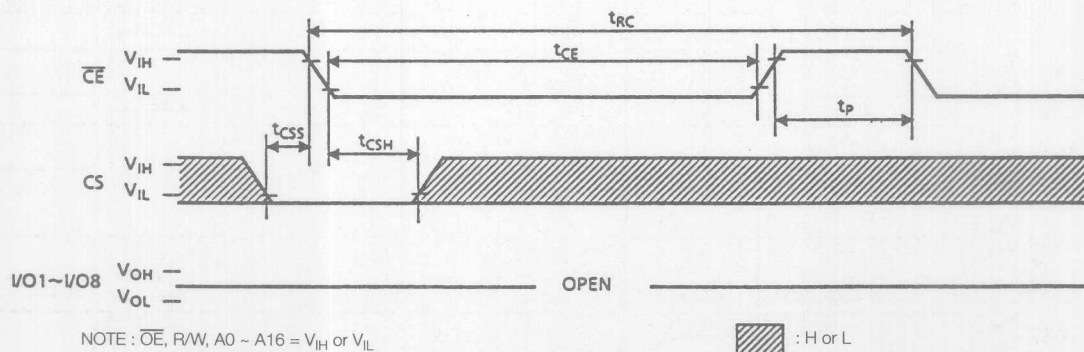
Auto Refresh



Self Refresh

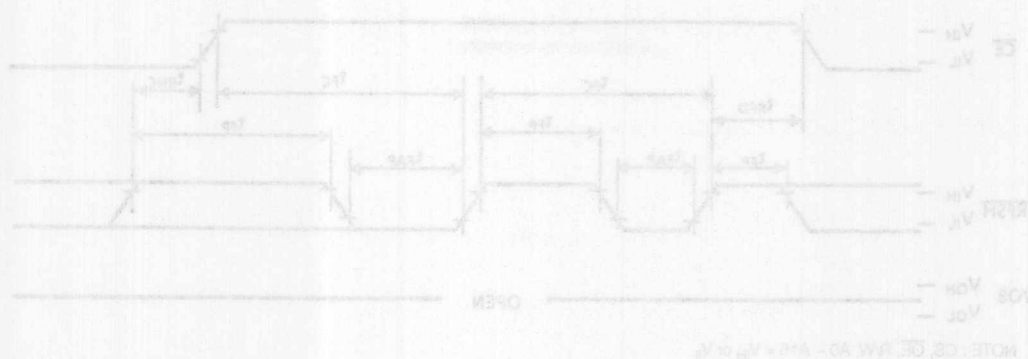


CS Standby Mode

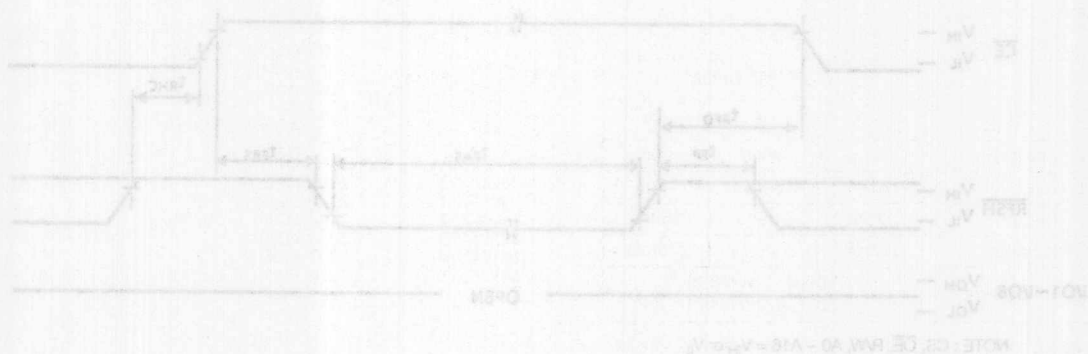


Notes

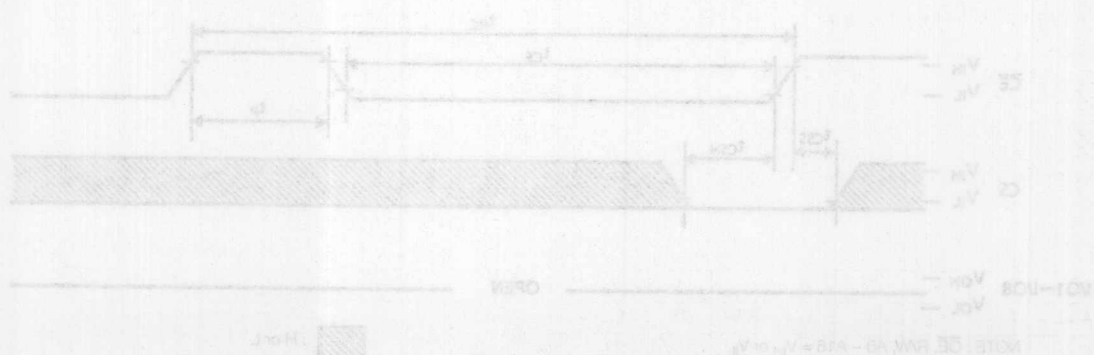
Auto Refresh



Self Refresh



CS Standby Mode



TC518129BPL/BSPL/BFL/BFWL/BFTL-70/80/10 TC518129BPL/BSPL/BFL/BFWL/BFTL-70L/80L/10L

SILICON GATE CMOS

131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518129B is a 1M bit high speed CMOS pseudo static RAM organized as 131,072 words by 8 bits. The TC518129B utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518129B operates from a single 5V power supply. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC518129B features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

A CS standby mode interface is incorporated in the TC518129B family, with the CE2 pin in the TC518128B family changed to a CS pin. The TC518129B is available in a 32-pin, 0.6 inch and 0.3 inch width plastic DIP, a small outline plastic flat package, and a 32-pin thin small outline plastic package (forward type).

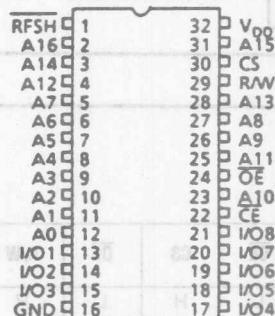
Features

- Organization: 131,072 words x 8 bits
- Single 5V power supply
- Fast access time

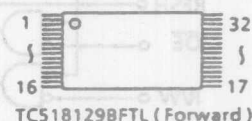
	TC518129B Family		
	-70	-80	-10
t_{CEA} \overline{CE} Access Time	70ns	80ns	100ns
t_{OEA} \overline{OE} Access Time	25ns	30ns	40ns
t_{RC} Cycle Time	115ns	130ns	160ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	200 μ A (L version) 50 μ A (LL version)		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 512 refresh cycles/8ms
- Auto refresh power down feature
- Package
 - TC518129BPL : DIP32-P-600
 - TC518129BFL : SOP32-P-450
 - TC518129BSPL : DIP32-P-300
 - TC518129BFWL : SOP32-P-525
 - TC518129BFTL : TSOP32-P-0820

Pin Connection (Top View)



TC518129BPL/8FL/BSPL/BFWL



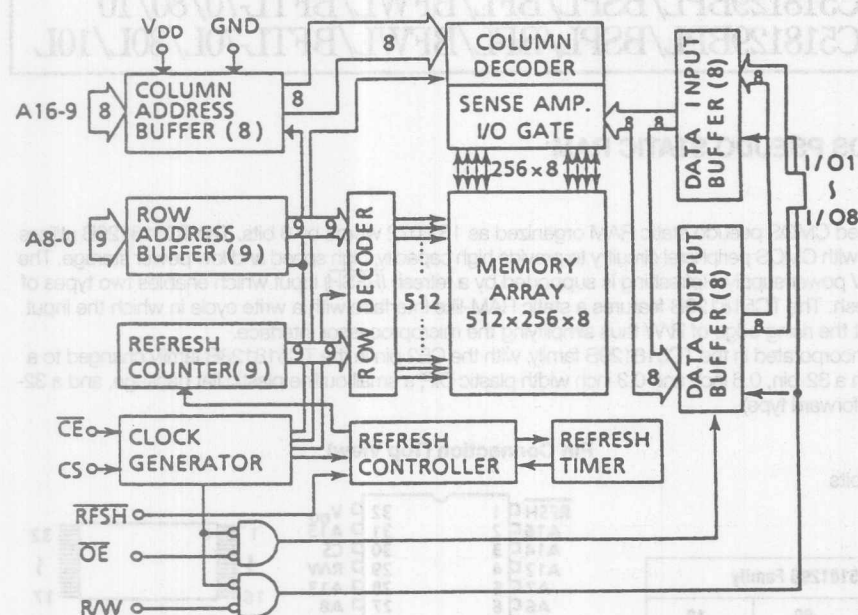
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
RFSH	Refresh Input
\overline{CE}	Chip Enable Input
CS	Chip Select Input
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

(TSOP)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CS	A ₁₅	V_{DD}	RFSH	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀	\overline{OE}

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	CS	\overline{OE}	R/W	\overline{RFSH}	A0 ~ A16	I/O1 ~ 8
Read		L	H	L	H	*	V*	OUT
Write		L	H	*	L	*	V*	IN
\overline{CE} only Refresh		L	H	H	H	*	V*	HZ
CS Standby		L	L	*	*	*	*	HZ
Auto/Self Refresh		H	*	*	*	L	*	HZ
Standby		H	*	*	*	H	*	HZ

H = High level input (V_{IH})

L = Low level input (V_{IL})

* = V_{IH} or V_{IL}

V* = At the falling edge of \overline{CE} , all address inputs are latched. At all other times, the address inputs are **.

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1.0$	V	
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC} \text{ min.}$	70ns version	—	50	70	mA 3,4
		80ns version	—	40	60	
		100ns version	—	35	50	
I_{DDs1}	Standby Current $\overline{CE} = V_{IH}$, $\overline{RFSH} = V_{IH}$	—	—	1	mA	
I_{DDs2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$, $\overline{RFSH} = V_{DD} - 0.2V$	L version	—	100	200	μA
		LL version	—	35	50	μA
I_{DDF1}	Self Refresh Current (Average) $\overline{CE} = V_{IH}$, $\overline{RFSH} = V_{IL}$	—	—	1	mA	
I_{DDF2}	Self Refresh Current (Average) $\overline{CE} = V_{DD} - 0.2V$, $\overline{RFSH} = 0.2V$	L version	—	100	200	μA
		LL version	—	35	50	μA
I_{DDF3}	Auto Refresh Current (Average) \overline{RFSH} cycling: $t_{FC} = t_{FC} \text{ min.}$	—	—	2	mA	
I_{DDF4}	\overline{CE} only Refresh Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC} \text{ min.}$	70ns version	—	50	70	mA 3
		80ns version	—	40	60	
		100ns version	—	35	50	
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = $0V$	—	—	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disabled ($\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $R/W = V_{IL}$), $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level $I_{OH} = -1mA$	2.4	—	—	V	
V_{OL}	Output Low Level $I_{OL} = 2.1mA$	—	—	0.4	V	

Capacitance* ($V_{DD} = 5V$, $T_a = 25^\circ\text{C}$, $f = 1MHz$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	—	5	pF
C_{I2}	Input Capacitance (\overline{CE} , CS, \overline{OE} , R/W, \overline{RFSH})	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

TC518129BPL/BSPL/BFL/BFWL/BFTL-70/80/10
 TC518129BPL/BSPL/BFL/BFWL/BFTL-70L/80L/10L Static RAM

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	115	—	130	—	160	—		
t_{RMW}	Read Modify Write Cycle Time	160	—	180	—	220	—		
t_{CE}	\overline{CE} Pulse Width	70	10,000	80	10,000	100	10,000		
t_p	\overline{CE} Precharge Time	35	—	40	—	50	—		
t_{CEA}	\overline{CE} Access Time	—	70	—	80	—	100		
t_{OEA}	\overline{OE} Access Time	—	25	—	30	—	40		
t_{CLZ}	\overline{CE} to Output in Low -Z	20	—	20	—	20	—		
t_{OLZ}	\overline{OE} to Output in Low -Z	0	—	0	—	0	—		
t_{WLZ}	Output Active from End of Write	0	—	0	—	0	—		
t_{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	0	25		9
t_{OHZ}	\overline{OE} Disable to Output in High-Z	0	20	0	20	0	25		9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	25	0	30		9
t_{ODS}	\overline{OE} Output Disable Setup Time	0	—	0	—	0	—		
t_{ODH}	\overline{OE} Output Disable Hold Time	10	—	10	—	10	—		
t_{RCS}	Read Command Setup Time	0	—	0	—	0	—		
t_{RCH}	Read Command Hold Time	0	—	0	—	0	—		
t_{CSS}	Chip Select Setup Time	0	—	0	—	0	—	ns	
t_{CSH}	Chip Select Hold Time	20	—	25	—	30	—		
t_{WP}	Write Pulse Width	20	—	25	—	30	—		
t_{WCH}	Write Command Hold Time	35	10,000	40	10,000	50	10,000		
t_{CWL}	Write Command to \overline{CE} Lead Time	20	10,000	25	10,000	30	10,000		
t_{DSW}	Data Setup Time from R/W	15	—	20	—	25	—		10
t_{DSC}	Data Setup Time from \overline{CE}	15	—	20	—	25	—		10
t_{DHW}	Data Hold Time from R/W	0	—	0	—	0	—		10
t_{DHC}	Data Hold Time from \overline{CE}	0	—	0	—	0	—		10
t_{ASC}	Address Setup Time	0	—	0	—	0	—		11
t_{AHC}	Address Hold Time	20	—	25	—	30	—		11
t_{RHC}	RFSH Command Hold Time	15	—	15	—	15	—		
t_{FC}	Auto Refresh Cycle Time	115	—	130	—	160	—		
t_{RFD}	RFSH Delay Time from \overline{CE}	35	—	40	—	50	—		
t_{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000		12
t_{FP}	RFSH Precharge Time	30	—	30	—	30	—		12
t_{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—		12
t_{FRS}	\overline{CE} Delay Time from RFSH (Self Refresh)	160	—	160	—	190	—		12
t_{REF}	Refresh Period (512 cycles, A0 ~ A8)	—	8	—	8	—	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

Notes:

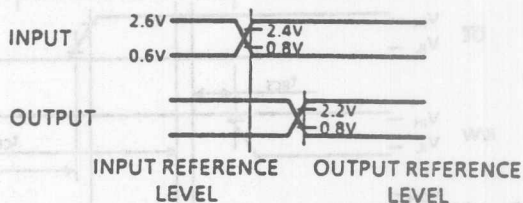
- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DDO} and I_{DDF4} depend on the cycle time.
- 4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

7) Timing reference levels

Input Levels : $V_{IH} = 2.6V$
 $V_{IL} = 0.6V$

Input Reference Levels : $V_{IH} = 2.4V$
 $V_{IL} = 0.8V$

Output Reference Levels : $V_{OH} = 2.2V$
 $V_{OL} = 0.8V$

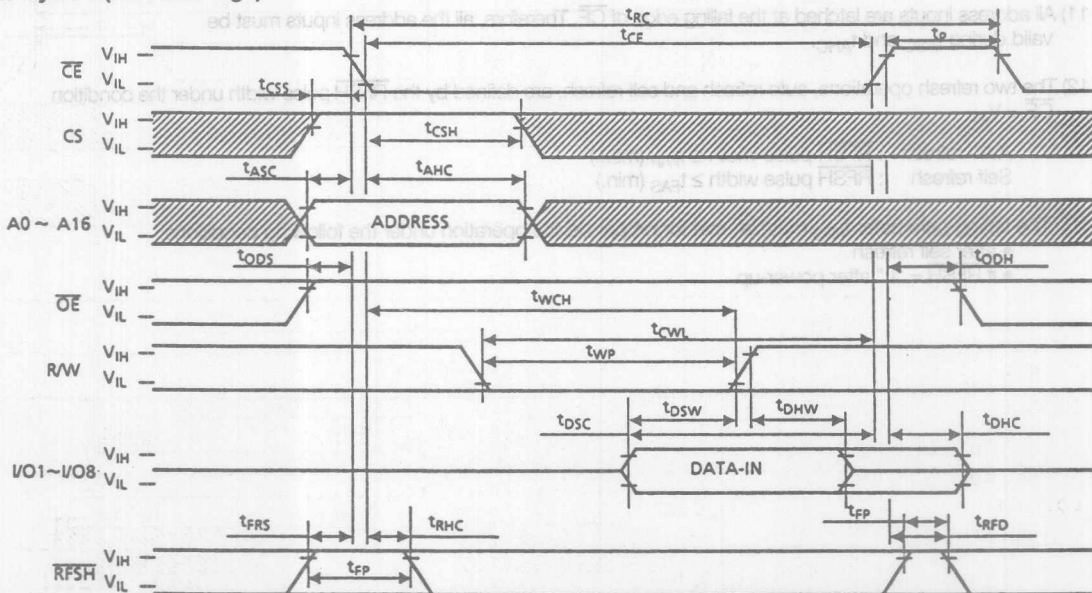
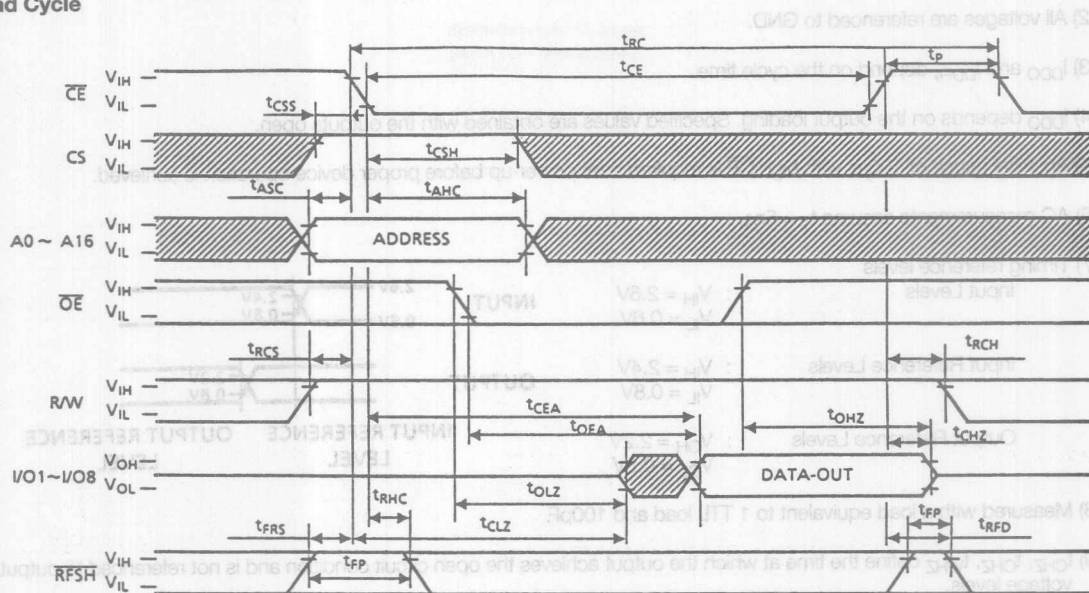


- 8) Measured with a load equivalent to 1 TTL load and 100pF.
- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) For write cycles, the input data is latched at the earlier of R/W or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
- 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.
 - Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 - Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

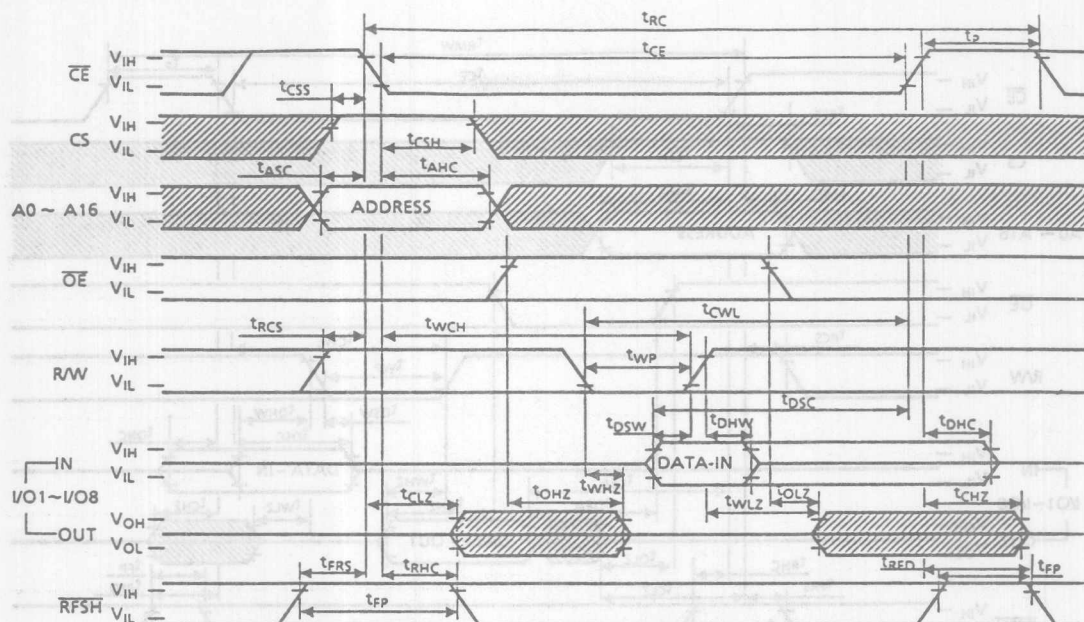
- after self refresh
- if $\overline{RFSH} = "L"$ after power-up

† Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.

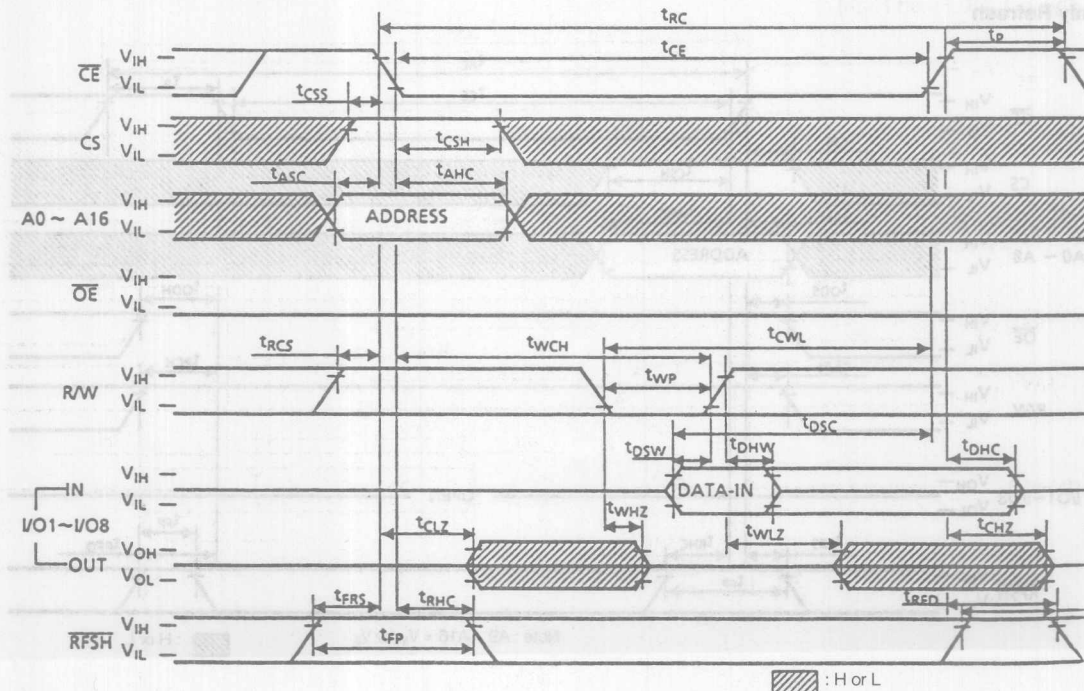


 : H or L

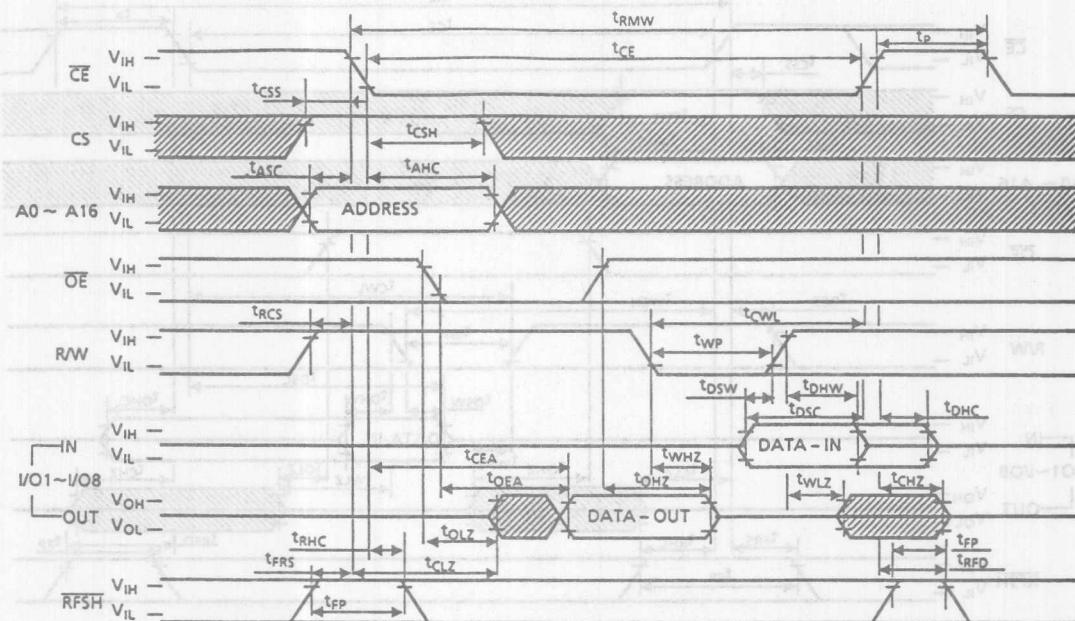
Write Cycle 2 (\overline{OE} Clocked)



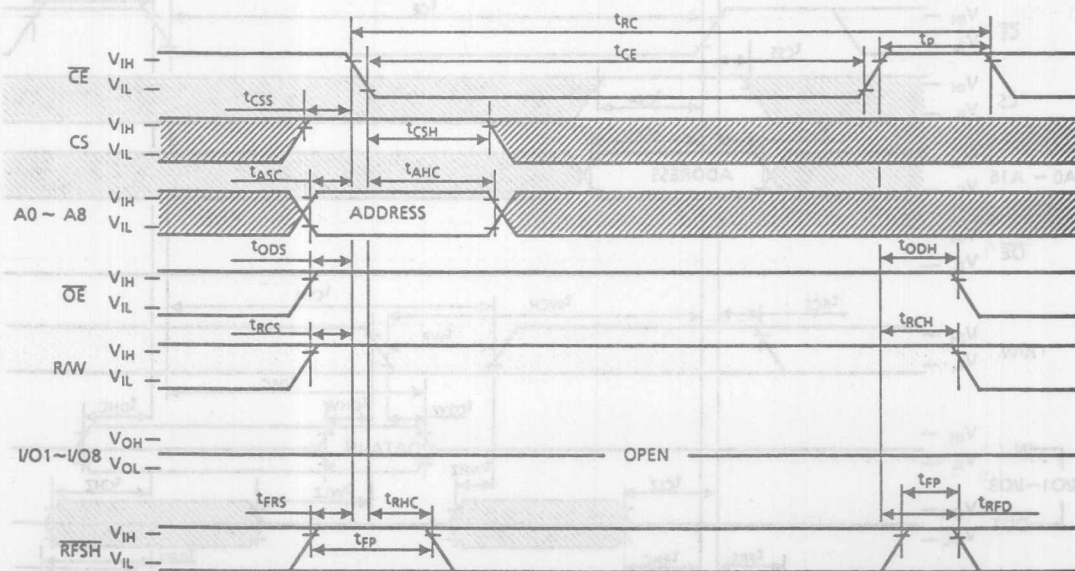
Write Cycle 3 (\overline{OE} Fixed Low)



Read Modify Write Cycle



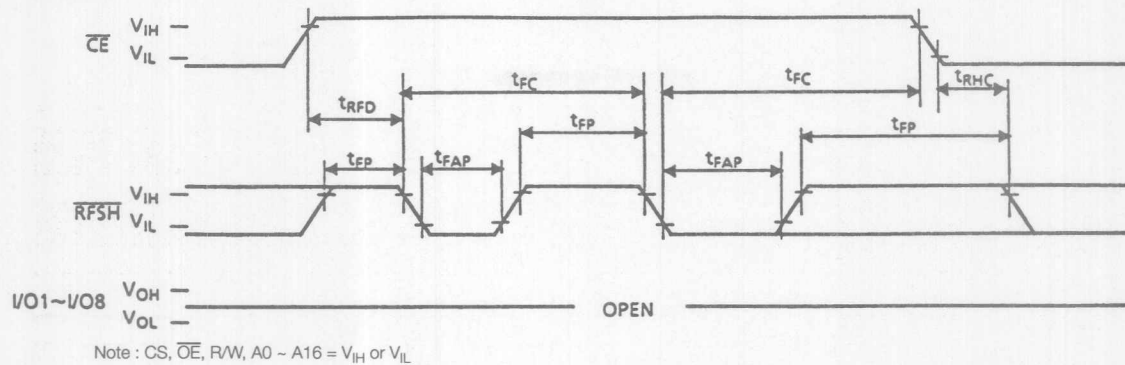
$\overline{\text{CE}}$ Only Refresh



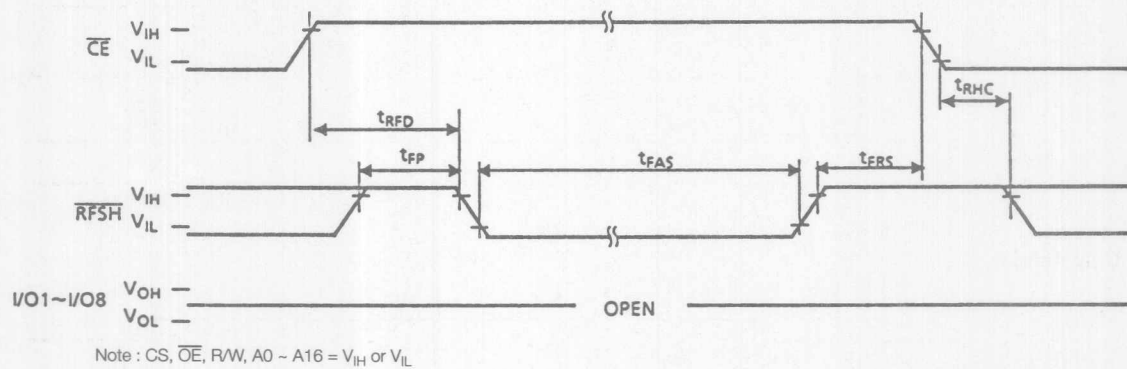
Note : A9 ~ A16 = V_{IH} or V_{IL}

▨ : H or L

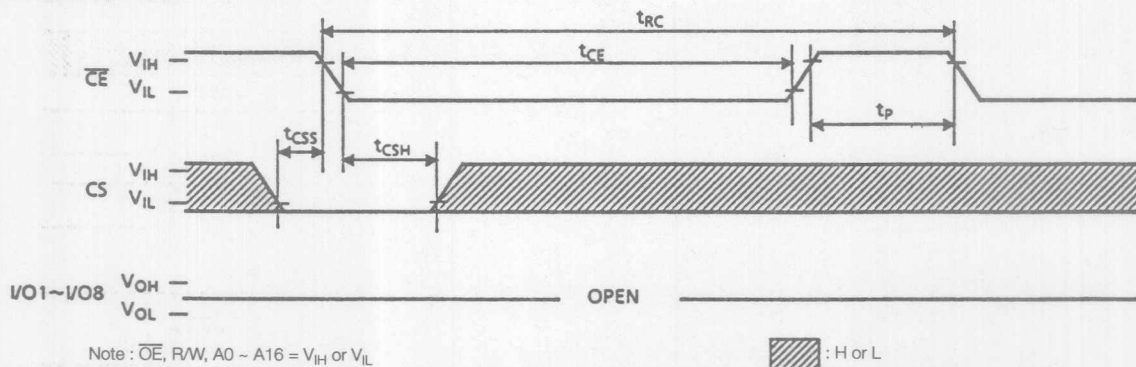
Auto Refresh



Self Refresh



CS Standby Mode



Notes

TC518129BPL/BFL/BFWL/BFTL-70V/80V/10V

SILICON GATE CMOS

131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518129B-V is a 1M bit high speed CMOS pseudo static RAM organized as 131,072 words by 8 bits. The TC518129B-V utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518129B-V operates from a single power supply of 2.7 ~ 5.5V. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC518129B-V features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

A CS standby mode interface is incorporated in the TC518129B-V family, with the CE2 pin in the TC518128B-V family changed to a CS pin. The TC518129B-V is available in a 32-pin, 0.6 inch width plastic DIP, a small outline plastic flat package, and a 32-pin thin small outline plastic package (forward type).

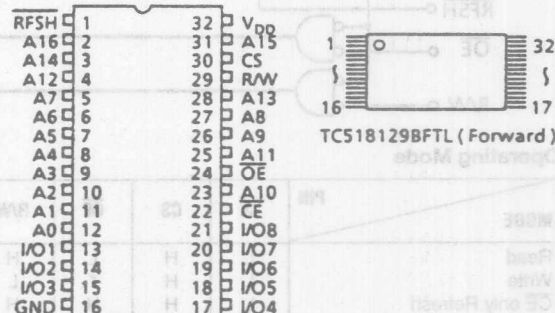
Features

- Organization: 131,072 words x 8 bits
- Low voltage operation: 2.7V ~ 5.5V
- Data retention supply voltage: 2.7V ~ 5.5V
- Fast access time

		TC518129B-V Family		
		-70	-80	-10
t_{CEA} \overline{CE} Access Time		70ns	80ns	100ns
t_{OEA} \overline{OE} Access Time		25ns	30ns	40ns
t_{RC} Cycle Time		115ns	130ns	160ns
Power Dissipation		385mW	330mW	275mW
Self Refresh Current	5.5V	50 μ A		
	3.0V	25 μ A		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 512 refresh cycles/8ms
- Auto refresh power down feature
- Package
 - TC518129BPL-V: DIP32-P-600
 - TC518129BFL-V: SOP32-P-450
 - TC518129BFWL-V: SOP32-P-525
 - TC518129BFTL-V: TSOP32-P-0820

Pin Connection (Top View)



TC518129BPL / BFL / BFWL

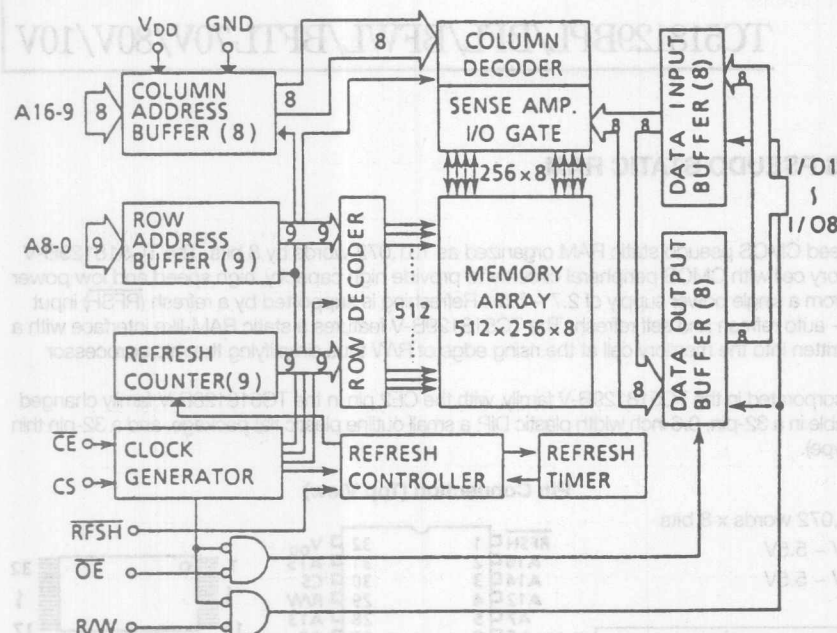
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
RFSH	Refresh Input
\overline{CE}	Chip Enable Input
CS	Chip Select Input
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

(TSOP)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CS	A ₁₅	V _{DD}	RFSH	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀	\overline{OE}

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	CS	\overline{OE}	R/W	RFSH	A0 ~ A16	I/O1 ~ 8
Read		L	H	L	H	*	V*	OUT
Write		L	H	*	L	*	V*	IN
\overline{CE} only Refresh		L	H	H	H	*	V*	HZ
CS Standby		L	L	*	*	*	*	HZ
Auto/Self Refresh		H	*	*	*	L	*	HZ
Standby		H	*	*	*	H	*	HZ

H = High level input (V_{IH})L = Low level input (V_{IL})* = V_{IH} or V_{IL} V* = At the falling edge of \overline{CE} , all address inputs are latched. At all other times, the address inputs are **.

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1.0$	V	
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC \text{ min.}}$	70ns version	—	50	70	mA 3,4
		80ns version	—	40	60	
		100ns version	—	35	50	
I_{DDS1}	Standby Current $\overline{CE} = V_{IH}$, $RFSH = V_{IH}$	—	—	1	mA	
I_{DDS2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$, $RFSH = V_{DD} - 0.2V$	—	35	50	μA	
I_{DDF1}	Self Refresh Current (Average) $\overline{CE} = V_{IH}$, $RFSH = V_{IL}$	—	—	1	mA	
I_{DDF2}	Self Refresh Current (Average) $\overline{CE} = V_{DD} - 0.2V$, $RFSH = 0.2V$	—	35	50	μA	
I_{DDF3}	Auto Refresh Current (Average) $RFSH$ cycling: $t_{FC} = t_{FC \text{ min.}}$	—	—	2	mA	
I_{DDF4}	\overline{CE} only Refresh Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC \text{ min.}}$	70ns version	—	50	70	mA 3
		80ns version	—	40	60	
		100ns version	—	35	50	
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = $0V$	—	—	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disabled ($\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $R/W = V_{IL}$), $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level $I_{OH} = -1.0\text{mA}$	2.4	—	—	V	
V_{OL}	Output Low Level $I_{OL} = 2.1\text{mA}$	—	—	0.4	V	

Capacitance* ($V_{DD} = 5V$, $T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	—	5	pF
C_{I2}	Input Capacitance (\overline{CE} , CS, \overline{OE} , R/W, $RFSH$)	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	115	—	130	—	160	—		
t _{RMW}	Read Modify Write Cycle Time	160	—	180	—	220	—		
t _{CE}	$\overline{\text{CE}}$ Pulse Width	70	10,000	80	10,000	100	10,000		
t _p	$\overline{\text{CE}}$ Precharge Time	35	—	40	—	50	—		
t _{CEA}	$\overline{\text{CE}}$ Access Time	—	70	—	80	—	100		
t _{OEa}	$\overline{\text{OE}}$ Access Time	—	25	—	30	—	40		
t _{CLZ}	$\overline{\text{CE}}$ to Output in Low -Z	20	—	20	—	20	—		
t _{OLZ}	$\overline{\text{OE}}$ to Output in Low -Z	0	—	0	—	0	—		
t _{WLZ}	Output Active from End of Write	0	—	0	—	0	—		
t _{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	0	25		9
t _{OHZ}	$\overline{\text{OE}}$ Disable to Output in High-Z	0	20	0	20	0	25		9
t _{WHZ}	Write Enable to Output in High-Z	0	25	0	25	0	30		9
t _{ODS}	$\overline{\text{OE}}$ Output Disable Setup Time	0	—	0	—	0	—		
t _{ODH}	$\overline{\text{OE}}$ Output Disable Hold Time	10	—	10	—	10	—		
t _{RCS}	Read Command Setup Time	0	—	0	—	0	—		
t _{RCH}	Read Command Hold Time	0	—	0	—	0	—		
t _{CSS}	Chip Select Setup Time	0	—	0	—	0	—		
t _{CSH}	Chip Select Hold Time	20	—	25	—	30	—	ns	
t _{WP}	Write Pulse Width	20	—	25	—	30	—		
t _{WCH}	Write Command Hold Time	35	10,000	40	10,000	50	10,000		
t _{CWL}	Write Command to $\overline{\text{CE}}$ Lead Time	20	10,000	25	10,000	30	10,000		
t _{DSW}	Data Setup Time from R/W	15	—	20	—	25	—		10
t _{DSC}	Data Setup Time from $\overline{\text{CE}}$	15	—	20	—	25	—		10
t _{DHW}	Data Hold Time from R/W	0	—	0	—	0	—		10
t _{DHC}	Data Hold Time from $\overline{\text{CE}}$	0	—	0	—	0	—		10
t _{ASC}	Address Setup Time	0	—	0	—	0	—		11
t _{AHC}	Address Hold Time	20	—	25	—	30	—		11
t _{RHC}	RFSH Command Hold Time	15	—	15	—	15	—		
t _{FC}	Auto Refresh Cycle Time	115	—	130	—	160	—		
t _{RFD}	RFSH Delay Time from $\overline{\text{CE}}$	35	—	40	—	50	—		
t _{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000		12
t _{FP}	RFSH Precharge Time	30	—	30	—	30	—		12
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—		12
t _{FRS}	$\overline{\text{CE}}$ Delay Time from RFSH (Self Refresh)	160	—	160	—	190	—		12
t _{REF}	Refresh Period (512 cycles, A0 ~ A8)	—	8	—	8	—	8	ms	
t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

3.0V Operation

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	2.7	3.0	3.3	V	2
V_{IH}	Input High Voltage	$V_{DD} - 0.2V$	—	$V_{DD} + 1.0V$	V	
V_{IL}	Input Low Voltage	-0.5	—	0.2	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 3.0V \pm 0.3V$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) CE Address cycling: $t_{RC} = t_{RC} \text{ min.}$	—	15	20	mA	3,4
I_{DDS2}	Standby Current	—	15	25	μA	
I_{DDF2}	Self Refresh Current (Average)	—	15	25	μA	
I_{DDF3}	Auto Refresh Current (Average) RFSH cycling: $t_{FC} = t_{FC} \text{ min.}$	—	—	2	mA	
I_{DDF4}	CE only Refresh Current (Average) CE Address cycling: $t_{RC} = t_{RC} \text{ min.}$	—	15	20	mA	3
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = $0V$	—	—	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable, $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level	$I_{OH} = -1\text{mA}$	2.4	—	V	
		$I_{OH} = -100\mu\text{A}$	$V_{DD} - 0.2V$	—		
V_{OL}	Output Low Level	$I_{OL} = 2.1\text{mA}$	—	0.4	V	
		$I_{OL} = 100\mu\text{A}$	—	0.2		

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 3.0\text{V} \pm 0.3\text{V}$) (Notes: 5, 6, 8)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t_{RC}	Random Read, Write Cycle Time	240	—		
t_{RMW}	Read Modify Write Cycle Time	320	—		
t_{CE}	\overline{CE} Pulse Width	150	10,000		13
t_p	\overline{CE} Precharge Time	80	—		
t_{CEA}	\overline{CE} Access Time	—	150		
t_{OEA}	\overline{OE} Access Time	—	80		
t_{CLZ}	\overline{CE} to Output in Low -Z	20	—		
t_{OLZ}	\overline{OE} to Output in Low -Z	5	—		
t_{WLZ}	Output Active from End of Write	5	—		
t_{CHZ}	Chip Disable to Output in High-Z	0	30		9
t_{OHZ}	\overline{OE} Disable to Output in High-Z	0	30		9
t_{WHZ}	Write Enable to Output in High-Z	0	40		9
t_{ODS}	\overline{OE} Output Disable Setup Time	0	—		
t_{ODH}	\overline{OE} Output Disable Hold Time	10	—		
t_{RCS}	Read Command Setup Time	0	—		
t_{RCH}	Read Command Hold Time	0	—	ns	
t_{WP}	Write Pulse Width	35	—		
t_{WCH}	Write Command Hold Time	70	10,000		
t_{CWL}	Write Command to \overline{CE} Lead Time	35	10,000		
t_{DSW}	Data Setup Time from R/W	30	—		10
t_{DSC}	Data Setup Time from \overline{CE}	30	—		10
t_{DHW}	Data Hold Time from R/W	0	—		10
t_{DHC}	Data Hold Time from \overline{CE}	0	—		10
t_{ASC}	Address Setup Time	0	—		11
t_{AHC}	Address Hold Time	35	—		11
t_{RHC}	\overline{RFSH} Command Hold Time	15	—		
t_{FC}	Auto Refresh Cycle Time	240	—		
t_{RFD}	\overline{RFSH} Delay Time from \overline{CE}	80	—		
t_{FAP}	\overline{RFSH} Pulse Width (Auto Refresh)	50	8,000		12
t_{FP}	\overline{RFSH} Precharge Time	50	—		12
t_{FAS}	\overline{RFSH} Pulse Width (Self Refresh)	8,000	—		12
t_{FRS}	\overline{CE} Delay Time from \overline{RFSH} (Self Refresh)	300	—		12
t_{REF}	Refresh Period (512 cycles, A0 ~ A8)	—	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	ns	

Timing Reference Levels:

Input Reference Levels: 1.5V/1.5V

Output Reference Levels: 1.5V/1.5V

Notes:

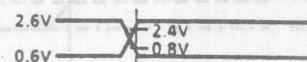
- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DD0} and I_{DDF4} depend on the cycle time.
- 4) I_{DD0} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

7) Timing reference levels

Input Levels

$$\begin{aligned} &: V_{IH} = 2.6V \\ &V_{IL} = 0.6V \end{aligned}$$

INPUT



Input Reference Levels

$$\begin{aligned} &: V_{IH} = 2.4V \\ &V_{IL} = 0.8V \end{aligned}$$

OUTPUT



Output Reference Levels

$$\begin{aligned} &: V_{OH} = 2.2V \\ &V_{OL} = 0.8V \end{aligned}$$

INPUT REFERENCE
LEVELOUTPUT REFERENCE
LEVEL

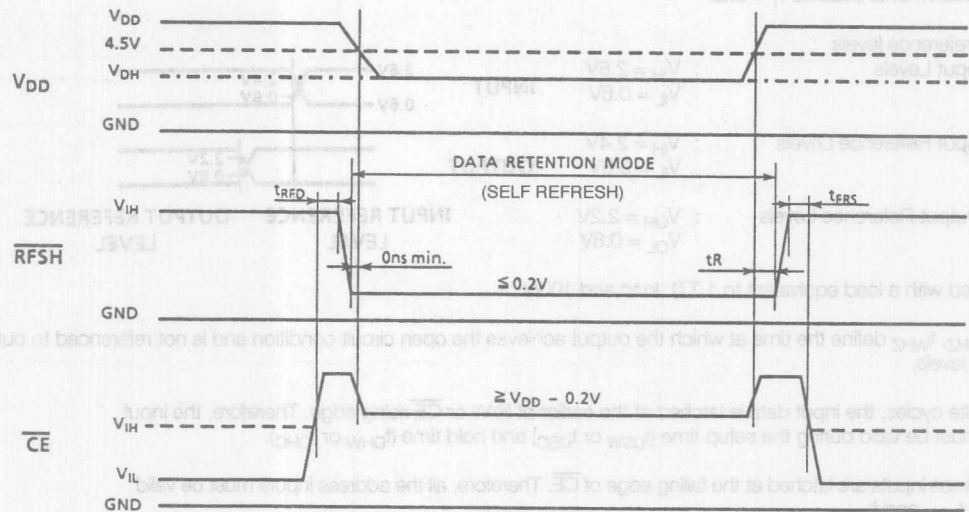
- 8) Measured with a load equivalent to 1 TTL load and 100pF.
- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) For write cycles, the input data is latched at the earlier of R/W or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
- 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.
 - Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 - Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

- after self refresh
- if $\overline{RFSH} = "L"$ after power-up

Data Retention Characteristics (Ta = 0 ~ 70°C)

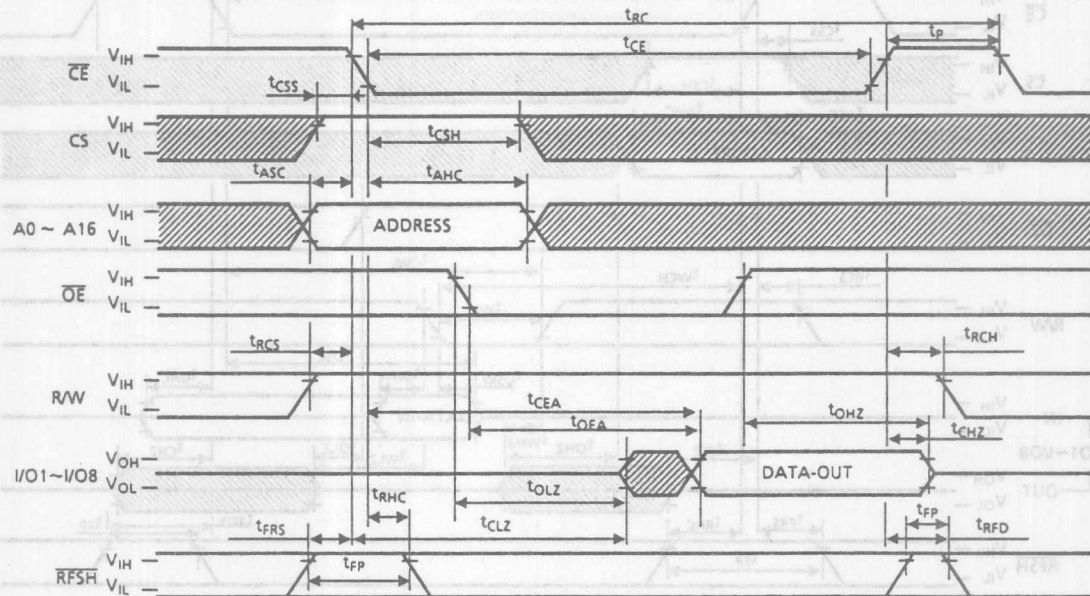
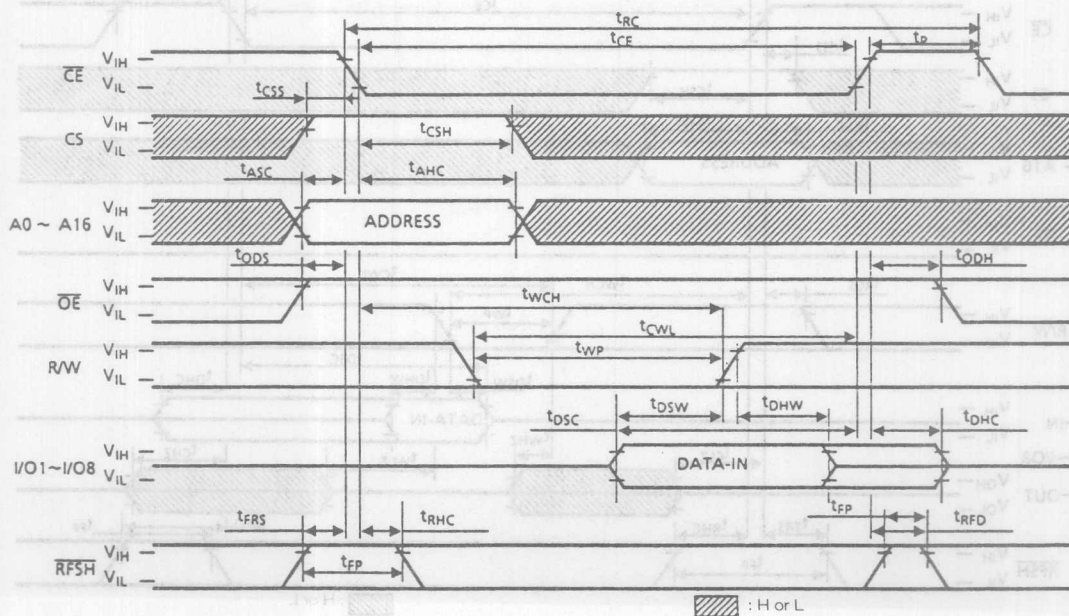
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DH}	Data Retention Supply Voltage	2.7	—	5.5	V
I _{DDF2}	Self Refresh Current	V _{DH} = 3.0V	—	15	μA
		V _{DH} = 5.5V	—	35	
t _R	Recovery Time	5	—	—	ms



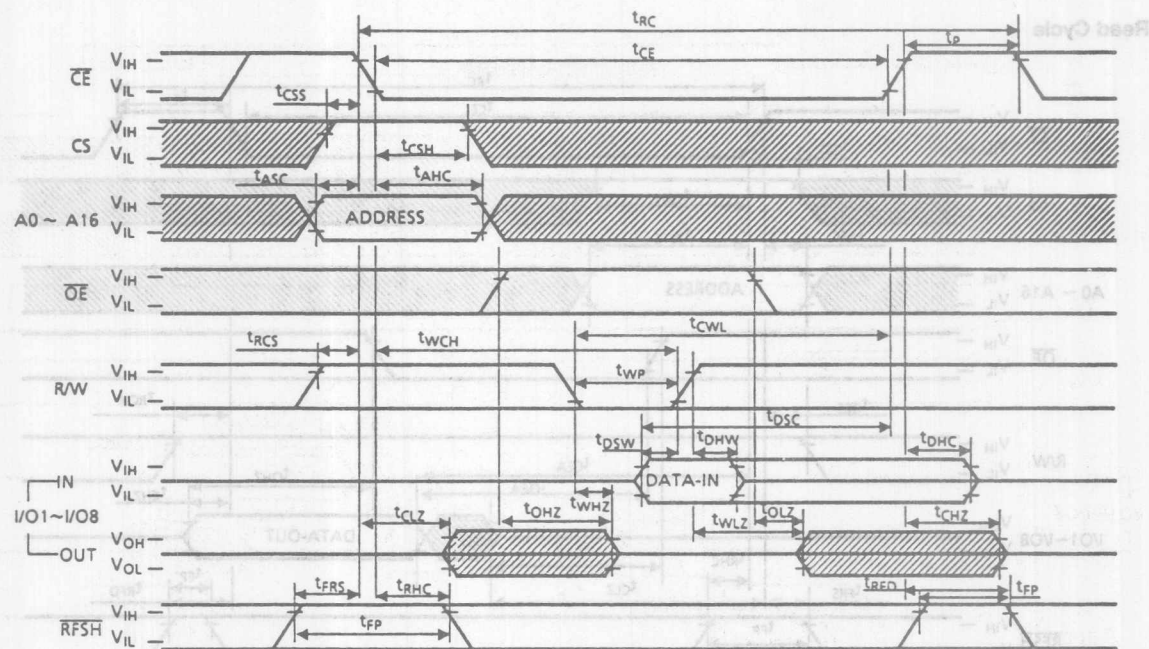
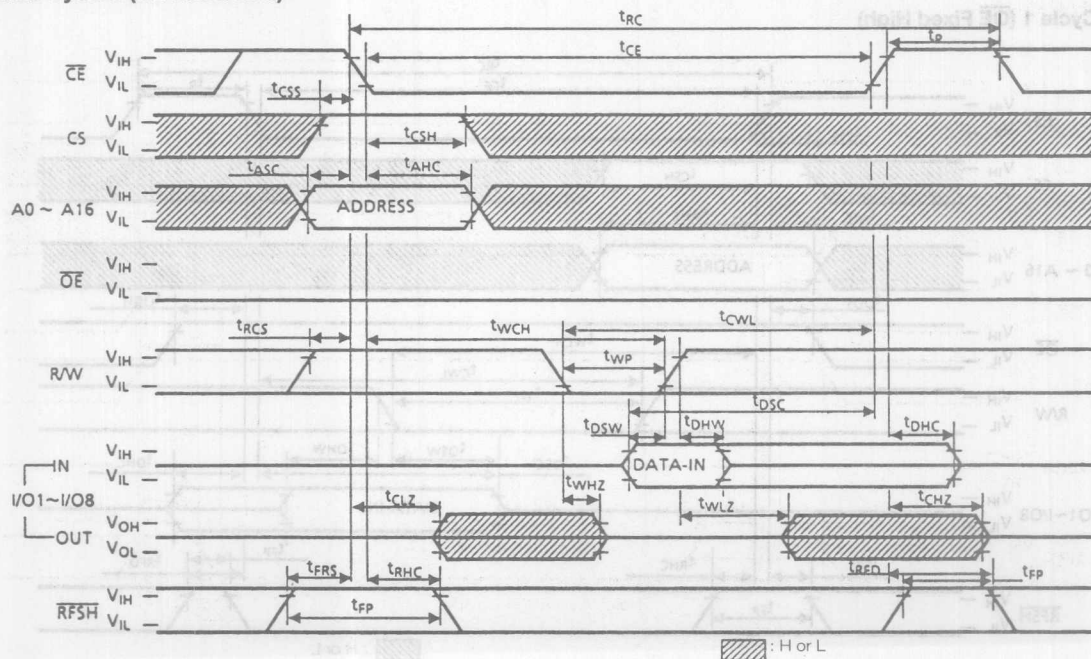
Notes: CS, \overline{OE} , RW, A0 ~ A16 = V_{IH} or V_{IL}
I_{DDF1} is applicable when RFSH = V_{IL} (max.), \overline{CE} = V_{IH} (min.).

Timing Waveforms

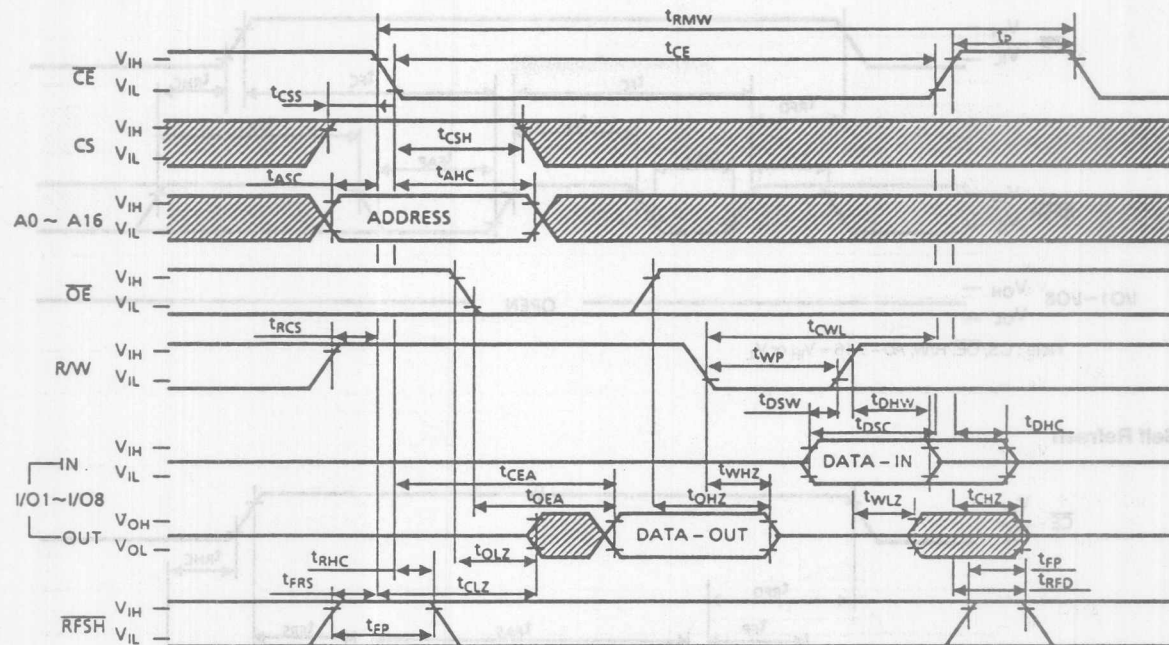
Read Cycle

Write Cycle 1 (\overline{OE} Fixed High)

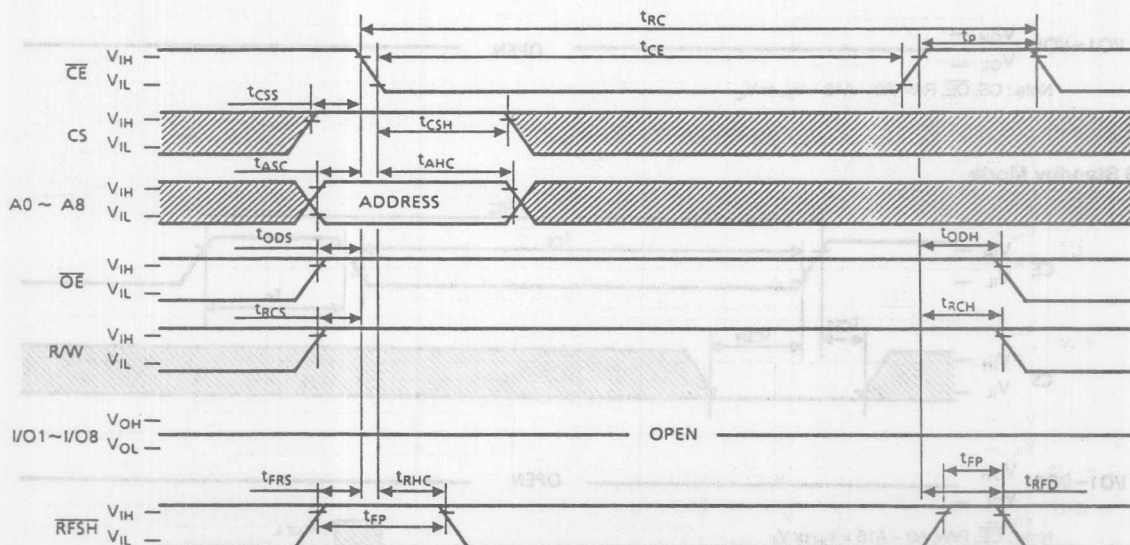
: H or L

Write Cycle 2 ($\overline{\text{OE}}$ Clocked)Write Cycle 3 ($\overline{\text{OE}}$ Fixed Low)

Read Modify Write Cycle

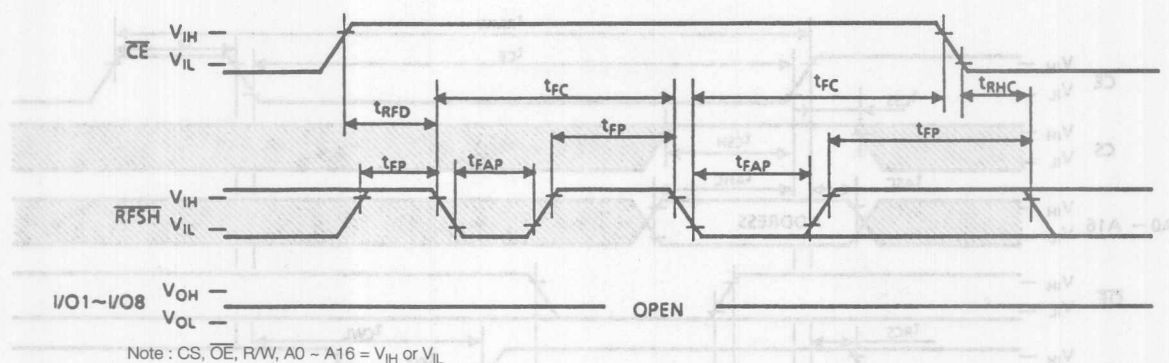


CE Only Refresh

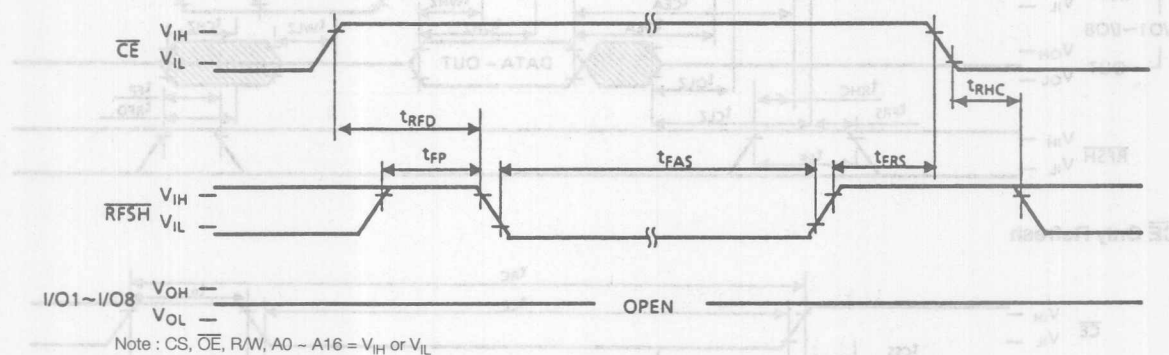
Note : A9 ~ A16 = V_{IH} or V_{IL}

: H or L

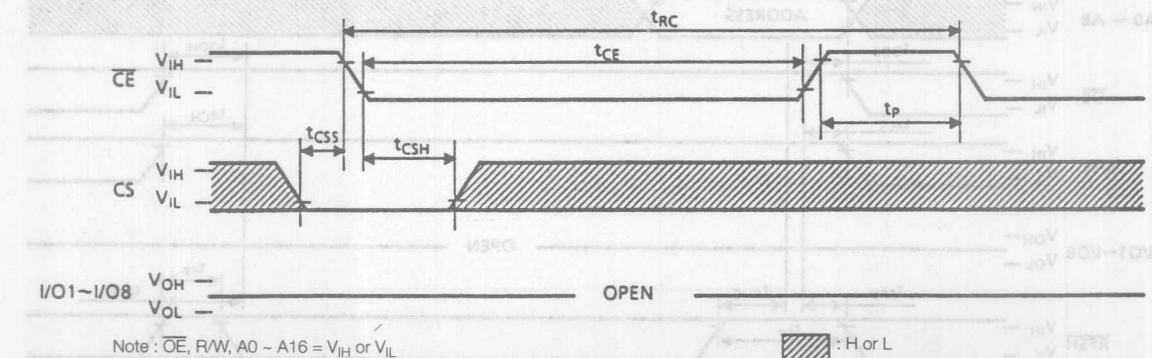
Auto Refresh



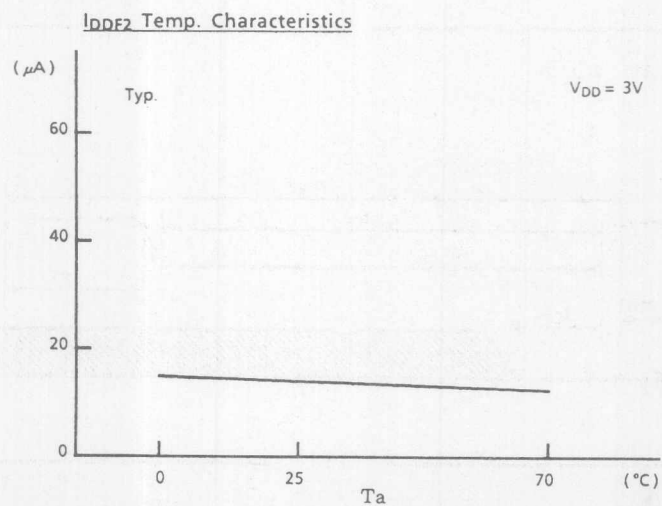
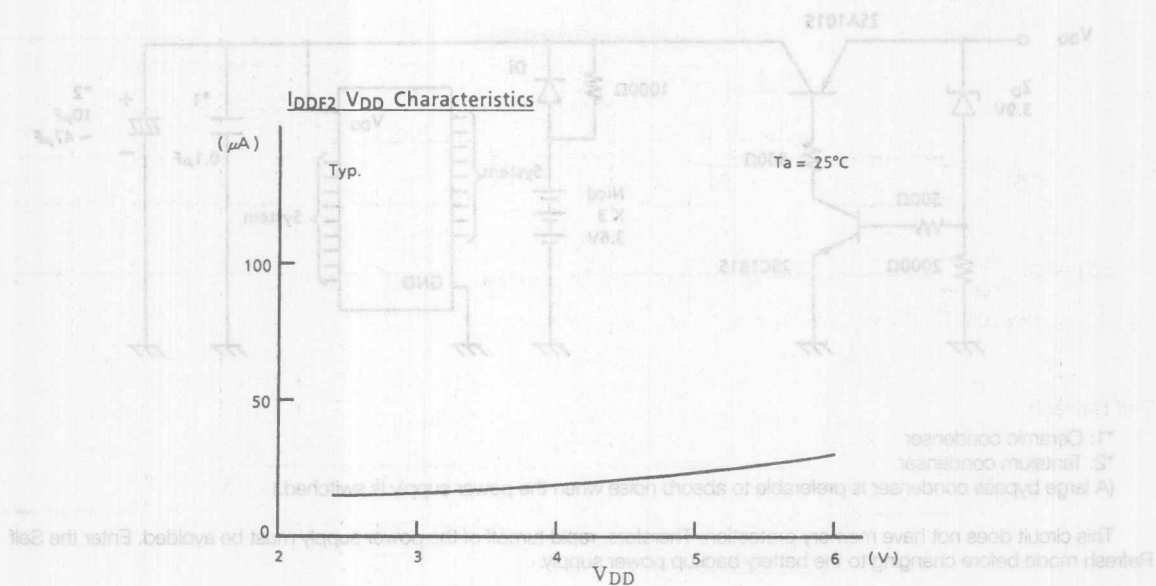
Self Refresh



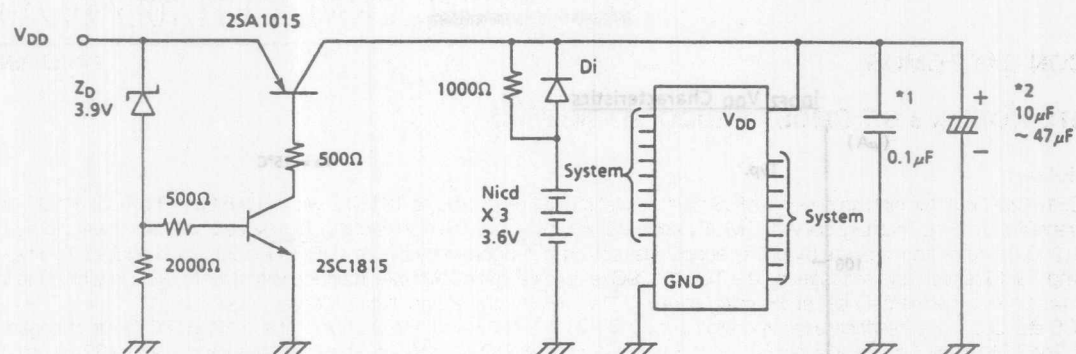
CS Standby Mode



Battery Backup Application Example



Battery Backup Application Example



*1: Ceramic condenser

*2: Tantalum condenser

(A large bypass condenser is preferable to absorb noise when the power supply is switched.)

This circuit does not have memory protection. Therefore, rapid turnoff of the power supply must be avoided. Enter the Self Refresh mode before changing to the battery backup power supply.

TC518129CPL/CFWL/CFTL-70/80/10 TC518129CPL/CFWL/CFTL-70L/80L/10L

SILICON GATE CMOS

PRELIMINARY

131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518129C is a 1M bit high speed CMOS pseudo static RAM organized as 131,072 words by 8 bits. The TC518129C utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518129C operates from a single 5V power supply. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC518129C features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

A CS standby mode interface is incorporated in the TC518129C family, with the CE2 pin in the TC518128C family changed to a CS pin. The TC518129C is available in a 32-pin, 0.6 inch width plastic DIP, a small outline plastic flat package, and a 32-pin thin small outline plastic package (forward type).

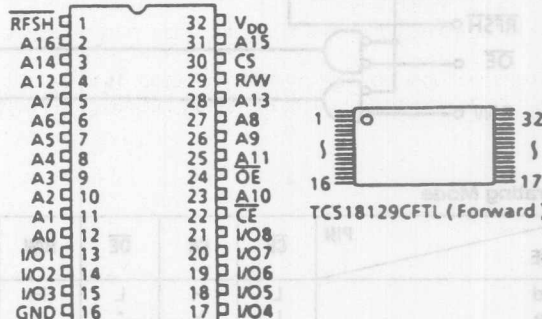
Features

- Organization: 131,072 words x 8 bits
- Single 5V power supply
- Fast access time

	TC518129C Family		
	-70	-80	-10
t _{CEA} \overline{CE} Access Time	70ns	80ns	100ns
t _{OE} \overline{OE} Access Time	25ns	30ns	40ns
t _{RC} Cycle Time	115ns	130ns	160ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	100 μ A (L version) 50 μ A (LL version)		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 512 refresh cycles/8ms
- Auto refresh power down feature
- Package
 - TC518129CPL : DIP32-P-600
 - TC518129CFWL : SOP32-P-525
 - TC518129CFTL : TSOP32-P-0820

Pin Connection (Top View)



TC518129CPL/CFWL

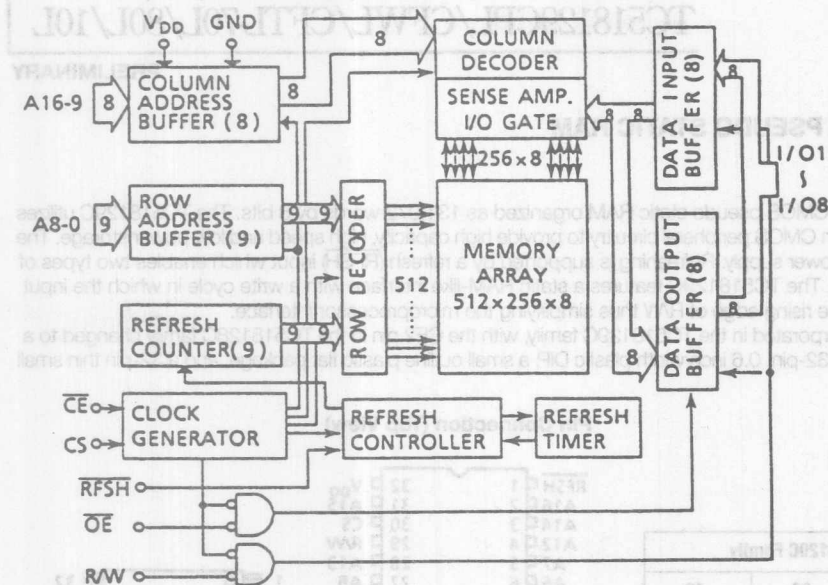
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
RFSH	Refresh Input
\overline{CE}	Chip Enable Input
CS	Chip Select Input
I/O1 ~ I/O8	Data Inputs/Outputs
V _{DD}	Power
GND	Ground

(TSOP)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CS	A ₁₅	V _{DD}	RFSH	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀	\overline{OE}

Block Diagram



Operating Mode

MODE	PIN	CE	CS	OE	R/W	RFSH	A0 ~ A16	I/O1 ~ 8
Read		L	H	L	H	*	V*	OUT
Write		L	H	*	L	*	V*	IN
CE only Refresh		L	H	H	H	*	V*	HZ
CS Standby		L	L	*	*	*	*	HZ
Auto/Self Refresh		H	*	*	*	L	*	HZ
Standby		H	*	*	*	H	*	HZ

H = High level input (V_{IH})

L = Low level input (V_{IL})

* = V_{IH} or V_{IL}

V* = At the falling edge of CE, all address inputs are latched. At all other times, the address inputs are ***.

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1.0$	V	2
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC \text{ min.}}$	70ns version	—	50	70	mA 3,4
		80ns version	—	40	60	
		100ns version	—	35	50	
I_{DDS1}	Standby Current $\overline{CE} = V_{IH}$, $RFSH = V_{IH}$	—	—	1	mA	
I_{DDS2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$, $RFSH = V_{DD} - 0.2V$	L version	—	50	100	μA
		LL version	—	35	50	μA
I_{DDF1}	Self Refresh Current (Average) $\overline{CE} = V_{IH}$, $RFSH = V_{IL}$	—	—	1	mA	
I_{DDF2}	Self Refresh Current (Average) $\overline{CE} = V_{DD} - 0.2V$, $RFSH = 0.2V$	L version	—	50	100	μA
		LL version	—	35	50	μA
I_{DDF3}	Auto Refresh Current (Average) $RFSH$ cycling: $t_{FC} = t_{FC \text{ min}}$	—	—	2	mA	
I_{DDF4}	\overline{CE} only Refresh Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC \text{ min.}}$	70ns version	—	50	70	mA 3
		80ns version	—	40	60	
		100ns version	—	35	50	
I_{IL}	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = $0V$	—	—	± 10	μA	
I_{OL}	Output Leakage Current Output Disabled ($\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $R/W = V_{IL}$), $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level $I_{OH} = -1mA$	2.4	—	—	V	
V_{OL}	Output Low Level $I_{OL} = 2.1mA$	—	—	0.4	V	

Capacitance* ($V_{DD} = 5V$, $T_a = 25^\circ\text{C}$, $f = 1MHz$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	—	5	pF
C_{I2}	Input Capacitance (\overline{CE} , CS, \overline{OE} , R/W, $RFSH$)	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, VDD = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	115	—	130	—	160	—		
t _{RMW}	Read Modify Write Cycle Time	160	—	180	—	220	—		
t _{CE}	CE Pulse Width	70	10,000	80	10,000	100	10,000		
t _p	CE Precharge Time	35	—	40	—	50	—		
t _{CEA}	CE Access Time	—	70	—	80	—	100		
t _{OEa}	OE Access Time	—	25	—	30	—	40		
t _{CLZ}	CE to Output in Low -Z	20	—	20	—	20	—		
t _{OLZ}	OE to Output in Low -Z	0	—	0	—	0	—		
t _{WLZ}	Output Active from End of Write	0	—	0	—	0	—		
t _{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	0	25		9
t _{OHZ}	OE Disable to Output in High-Z	0	20	0	20	0	25		9
t _{WHZ}	Write Enable to Output in High-Z	0	25	0	25	0	30		9
t _{ODS}	OE Output Disable Setup Time	0	—	0	—	0	—		
t _{ODH}	OE Output Disable Hold Time	10	—	10	—	10	—		
t _{RCS}	Read Command Setup Time	0	—	0	—	0	—		
t _{RCH}	Read Command Hold Time	0	—	0	—	0	—		
t _{CSS}	Chip Select Setup Time	0	—	0	—	0	—		
t _{CSH}	Chip Select Hold Time	20	—	25	—	30	—	ns	
t _{WP}	Write Pulse Width	20	—	25	—	30	—		
t _{WCH}	Write Command Hold Time	35	10,000	40	10,000	50	10,000		
t _{CWL}	Write Command to CE Lead Time	20	10,000	25	10,000	30	10,000		
t _{DSW}	Data Setup Time from R/W	15	—	20	—	25	—		10
t _{DSC}	Data Setup Time from CE	15	—	20	—	25	—		10
t _{DHW}	Data Hold Time from R/W	0	—	0	—	0	—		10
t _{DHC}	Data Hold Time from CE	0	—	0	—	0	—		10
t _{ASC}	Address Setup Time	0	—	0	—	0	—		11
t _{AHC}	Address Hold Time	20	—	25	—	30	—		11
t _{RHC}	RFSH Command Hold Time	15	—	15	—	15	—		
t _{FC}	Auto Refresh Cycle Time	115	—	130	—	160	—		
t _{RFD}	RFSH Delay Time from CE	35	—	40	—	50	—		
t _{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000		12
t _{FP}	RFSH Precharge Time	30	—	30	—	30	—		12
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—		12
t _{FRS}	CE Delay Time from RFSH (Self Refresh)	160	—	160	—	190	—		12
t _{REF}	Refresh Period (512 cycles, A0 ~ A8)	—	8	—	8	—	8	ms	
t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

Notes:

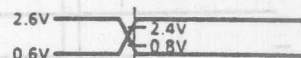
- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DD0} and I_{DDF4} depend on the cycle time.
- 4) I_{DD0} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_f = 5$ ns.

7) Timing reference levels

Input Levels

$$\begin{aligned} &: V_{IH} = 2.6V \\ &V_{IL} = 0.6V \end{aligned}$$

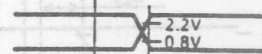
INPUT



Input Reference Levels

$$\begin{aligned} &: V_{IH} = 2.4V \\ &V_{IL} = 0.8V \end{aligned}$$

OUTPUT



Output Reference Levels

$$\begin{aligned} &: V_{OH} = 2.2V \\ &V_{OL} = 0.8V \end{aligned}$$

INPUT REFERENCE
LEVELOUTPUT REFERENCE
LEVEL

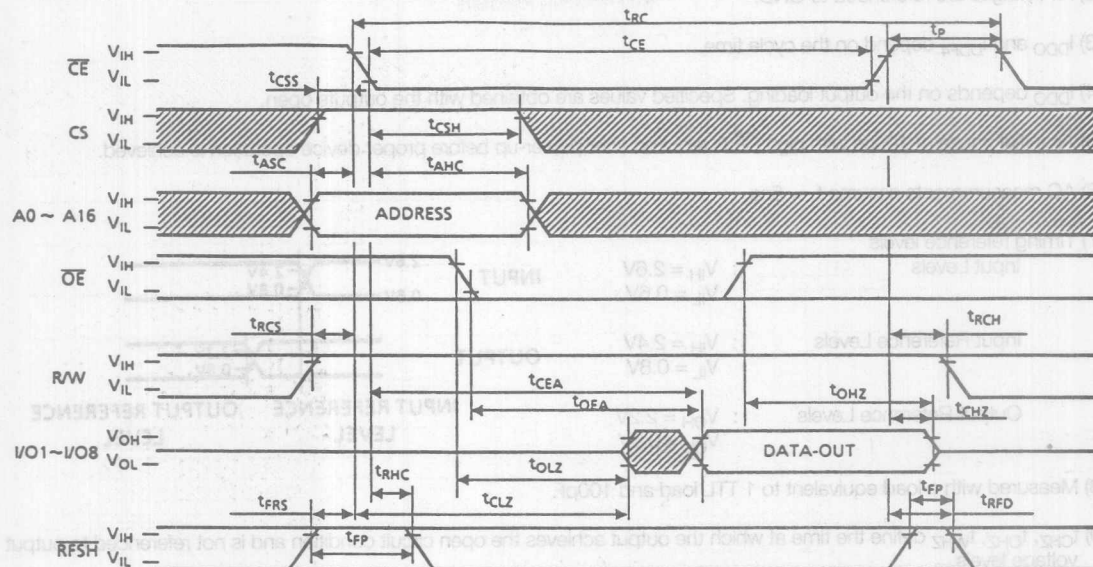
- 8) Measured with a load equivalent to 1 TTL load and 100pF.
- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) For write cycles, the input data is latched at the earlier of R/W or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
- 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.
 - Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 - Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

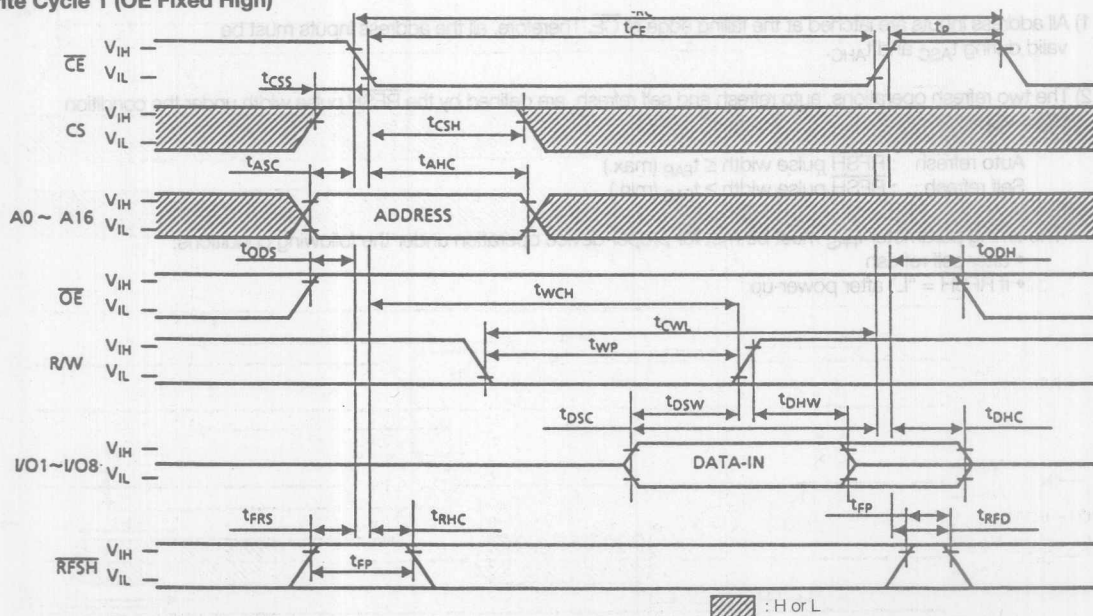
- after self refresh
- if $\overline{RFSH} = "L"$ after power-up

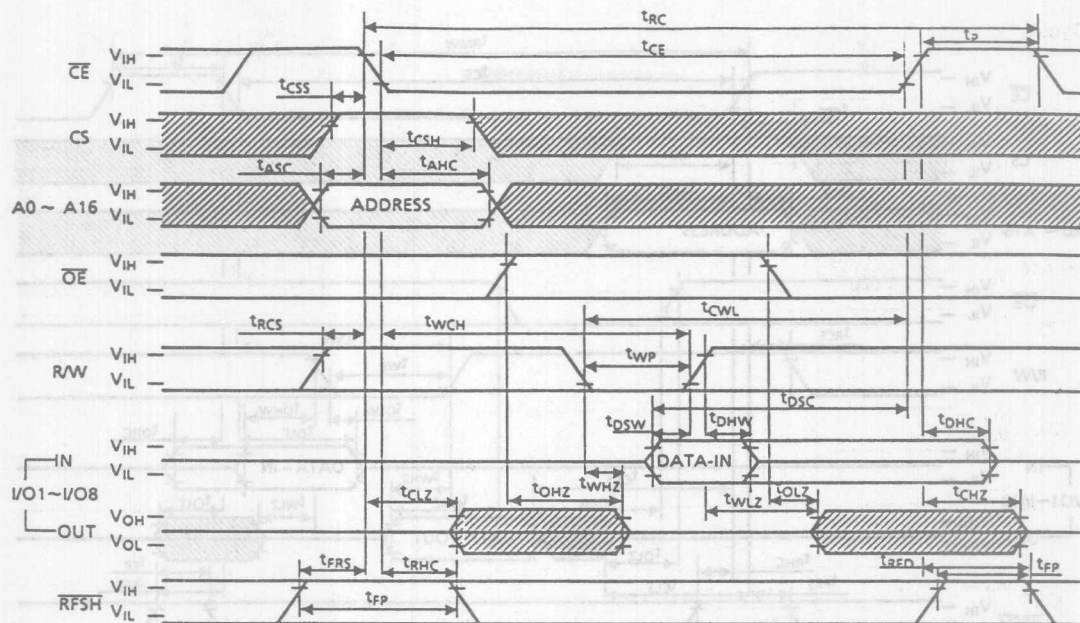
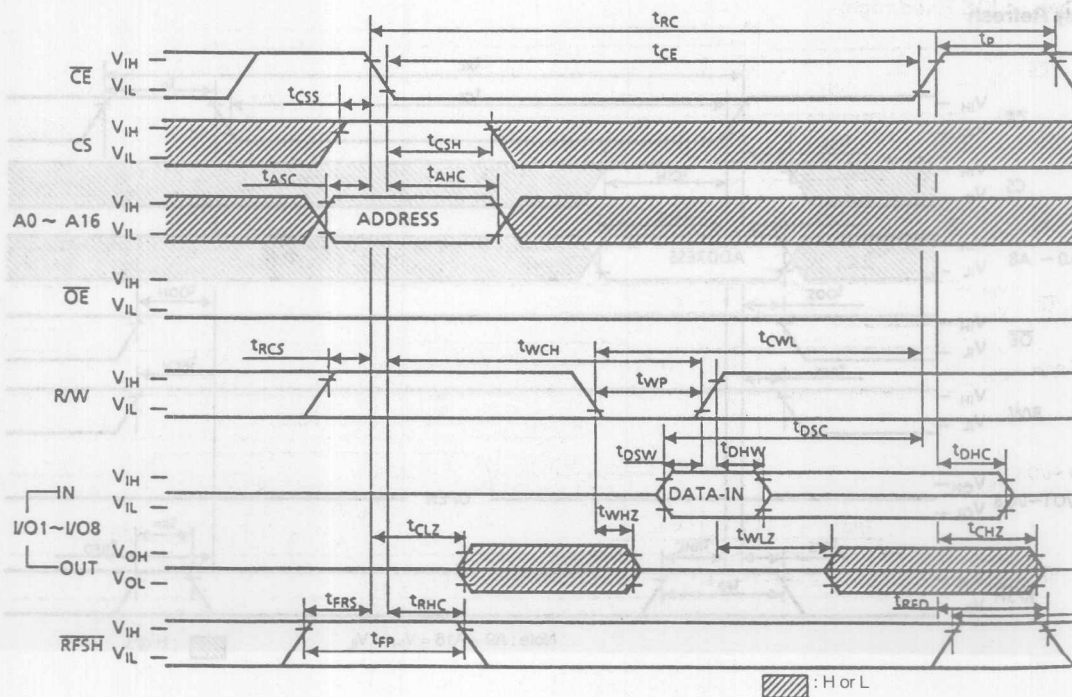
Timing Waveforms

Read Cycle



Write Cycle 1 (\overline{OE} Fixed High)

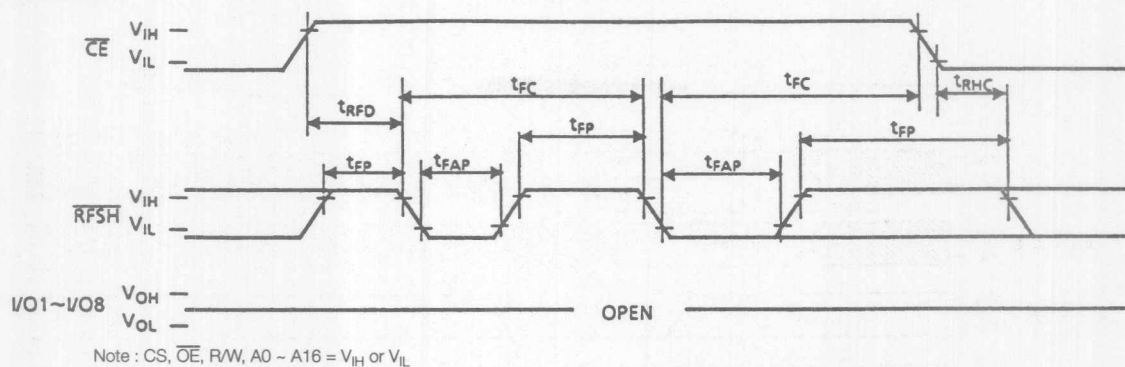


Write Cycle 2 (\overline{OE} Clocked)Write Cycle 3 (\overline{OE} Fixed Low)

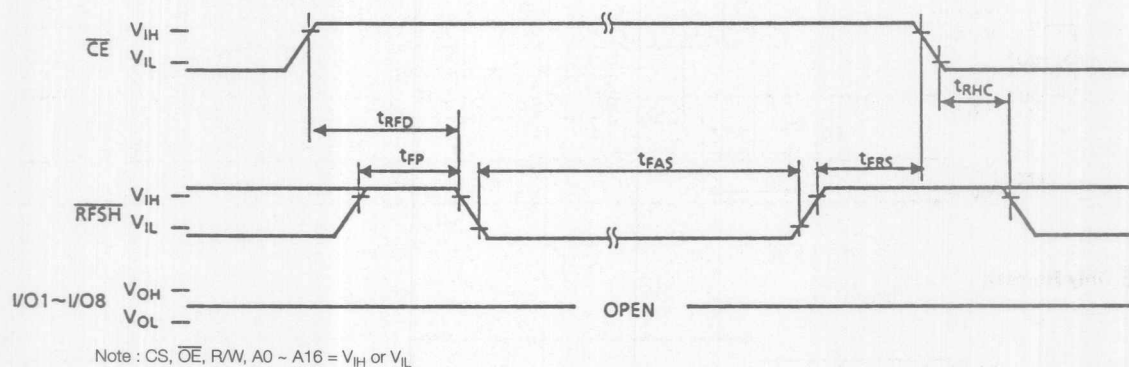
Note : A9 ~ A16 = V_{IH} or V_{IL}

 : H or L

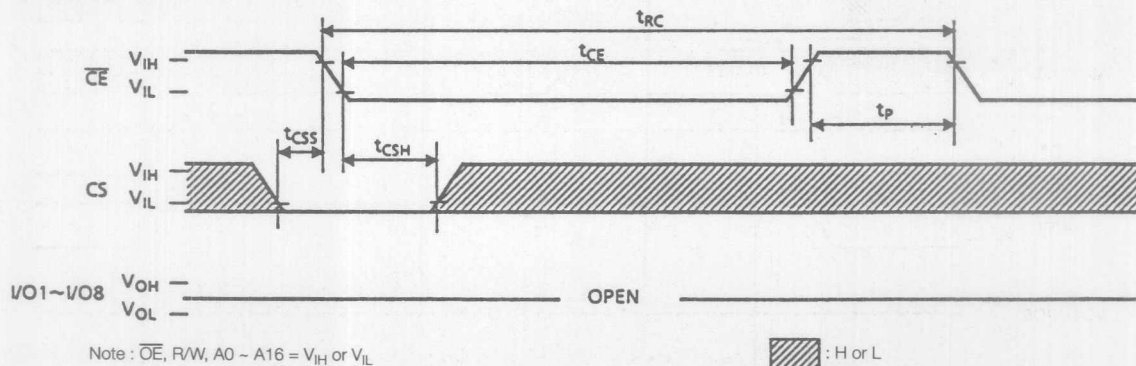
Auto Refresh



Self Refresh

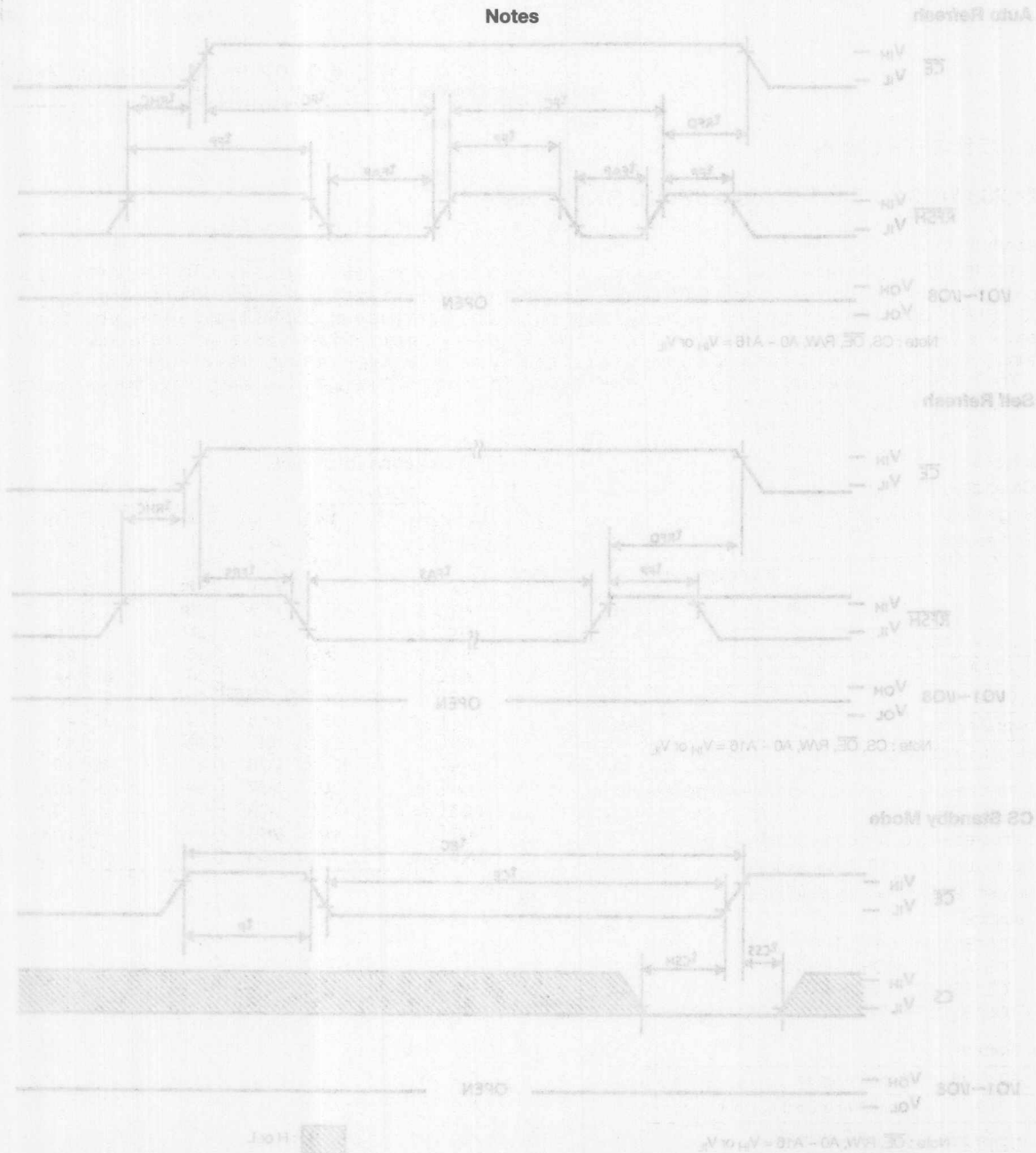


CS Standby Mode



Static RAM

Notes



TC518512PL/FL/FTL/TRL-70/80/10

SILICON GATE CMOS

524,288 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518512PL is a 4M bit high speed CMOS pseudo static RAM organized as 524,288 words by 8 bits. The TC518512PL utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518512PL operates from a single 5V power supply. Refreshing is supported by a refresh ($\overline{OE}/RFSH$) input which enables two types of refreshing - auto refresh and self refresh. The TC518512PL features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

The TC518512PL is available in a 32-pin, 0.6 inch width plastic DIP, a small outline plastic flat package, and a thin small outline package (forward type, reverse type).

Features

- Organization: 524,288 words x 8 bits
- Single 5V power supply
- Fast access time

	TC518512PL Family		
	-70	-80	-10
t_{CEA} \overline{CE} Access Time	70ns	80ns	100ns
t_{OEA} \overline{OE} Access Time	30ns	30ns	40ns
t_{RC} Cycle Time	115ns	130ns	160ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	200 μ A		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 2048 refresh cycles/32ms
- Package
 - TC518512PL: DIP32-P-600
 - TC518512FL: SOP32-P-525
 - TC518512FTL: TSOP32-P-400
 - TC518512TRL: TSOP32-P-400A

Pin Names

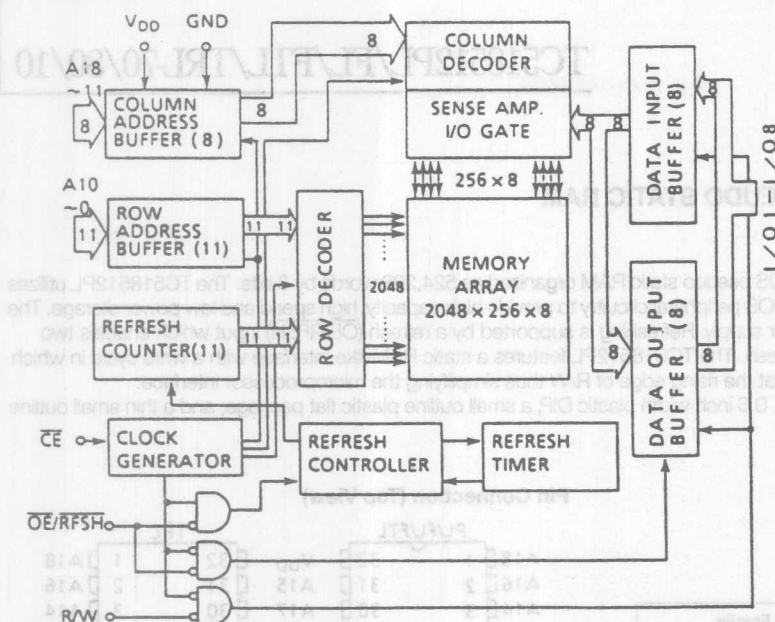
A0 ~ A18	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}/RFSH$	Output Enable Input Refresh Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O8	Data Inputs/Outputs
V _{DD}	Power
GND	Ground

Pin Connection (Top View)

PL/FL/FTL				TRL			
A18	1	32	V _{DD}	32	1	A18	
A16	2	31	A15	31	2	A16	
A14	3	30	A17	30	3	A14	
A12	4	29	R/W	29	4	A12	
A7	5	28	A13	28	5	A7	
A6	6	27	A8	27	6	A6	
A5	7	26	A9	26	7	A5	
A4	8	25	A11	25	8	A4	
A3	9	24	$\overline{OE}/RFSH$	24	9	A3	
A2	10	23	A10	23	10	A2	
A1	11	22	\overline{CE}	22	11	A1	
A0	12	21	I/O8	21	12	A0	
I/O1	13	20	I/O7	20	13	I/O1	
I/O2	14	19	I/O6	19	14	I/O2	
I/O3	15	18	I/O5	18	15	I/O3	
GND	16	17	I/O4	17	16	GND	

SYMBOL	ITEM	RATING	UNIT	NOTES
V _{IN}	Input Voltage	-1.0 ~ 7.0	V	
V _{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V _{CC}	Power Supply Voltage	-1.0 ~ 7.0	V	
T _{OP}	Operating Temperature	0 ~ 70	°C	
T _{STG}	Storage Temperature	-55 ~ 150	°C	
t _{DEL}	Retention Time	250 ~ 10	°C + sec	
P _D	Power Dissipation	385	mW	
I _{CC}	Self Refresh Current	80	mA	

Block Diagram



Operating Mode

MODE	PIN	CE	OE/RFSH	R/W	A0 ~ A18	I/O1 ~ 8
Read		L	L	H	V*	OUT
Write		L	*	L	V*	IN
CE only Refresh		L	H	H	V*	HZ
Auto/Self Refresh		H	L	*	*	HZ
Standby		H	H	*	*	HZ

H = High level input (V_{IH})L = Low level input (V_{IL})* = V_{IH} or V_{IL} V* = At the falling edge of \overline{CE} , all address inputs are latched. At all other times, the address inputs are ***.

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1.0$	V	
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC} \text{ min.}$	70ns version	—	50	70	mA 3,4
		80ns version	—	45	60	
		100ns version	—	35	50	
I_{DDs1}	Standby Current $\overline{CE} = V_{IH}$, $\overline{OE}/\overline{RFSH} = V_{IH}$	—	—	1	mA	
I_{DDs2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$, $\overline{OE}/\overline{RFSH} = V_{DD} - 0.2V$	—	—	200	μA	
I_{DDF1}	Self Refresh Current (Average) $\overline{CE} = V_{IH}$, $\overline{OE}/\overline{RFSH} = V_{IL}$	—	—	1	mA	
I_{DDF2}	Self Refresh Current (Average) $\overline{CE} = V_{DD} - 0.2V$, $\overline{OE}/\overline{RFSH} = 0.2V$	—	—	200	μA	
I_{DDF3}	Auto Refresh Current (Average) $\overline{OE}/\overline{RFSH}$ cycling: $t_{FC} = t_{FC} \text{ min.}$	70ns version	—	—	70	mA 3
		80ns version	—	—	60	
		100ns version	—	—	50	
I_{DDF4}	\overline{CE} only Refresh Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC} \text{ min.}$	70ns version	—	—	70	mA 3
		80ns version	—	—	60	
		100ns version	—	—	50	
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = $0V$	—	—	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disabled ($\overline{CE} = V_{IH}$ or $\overline{OE}/\overline{RFSH} = V_{IH}$ or $R/W = V_{IL}$) $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level $I_{OH} = -1.0\text{mA}$	2.4	—	—	V	
V_{OL}	Output Low Level $I_{OL} = 2.1\text{mA}$	—	—	0.4	V	

Capacitance* ($V_{DD} = 5V$, $T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A18)	—	5	pF
C_{I2}	Input Capacitance (\overline{CE} , $\overline{OE}/\overline{RFSH}$, R/W)	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	115	—	130	—	160	—		
t _{RMW}	Read Modify Write Cycle Time	165	—	180	—	220	—		
t _{CE}	$\overline{\text{CE}}$ Pulse Width	70	10,000	80	10,000	100	10,000		
t _p	$\overline{\text{CE}}$ Precharge Time	35	—	40	—	50	—		
t _{CEA}	$\overline{\text{CE}}$ Access Time	—	70	—	80	—	100		
t _{OEa}	$\overline{\text{OE}}$ Access Time	—	30	—	30	—	40		
t _{CLZ}	$\overline{\text{CE}}$ to Output in Low -Z	20	—	20	—	20	—		
t _{OLZ}	$\overline{\text{OE}}$ to Output in Low -Z	0	—	0	—	0	—		
t _{WLZ}	Output Active from End of Write	0	—	0	—	0	—		
t _{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	0	25	ns	9
t _{OHZ}	$\overline{\text{OE}}$ Disable to Output in High-Z	0	20	0	20	0	25		9
t _{WHZ}	Write Enable to Output in High-Z	0	20	0	20	0	25		9
t _{OSC}	$\overline{\text{OE}}$ Setup Time Referenced to $\overline{\text{CE}}$	10	—	10	—	10	—		9
t _{OHC}	$\overline{\text{OE}}$ Hold Time Referenced to $\overline{\text{CE}}$	0	—	0	—	0	—		9
t _{RCS}	Read Command Setup Time	0	—	0	—	0	—		
t _{RCH}	Read Command Hold Time	0	—	0	—	0	—		
t _{WP}	Write Pulse Width	25	—	25	—	30	—		
t _{WCH}	Write Command Hold Time	40	—	40	—	50	—		
t _{CWL}	Write Command to $\overline{\text{CE}}$ Lead Time	25	—	25	—	30	—		
t _{DSW}	Data Setup Time from R/W	20	—	20	—	25	—		10
t _{DSC}	Data Setup Time from $\overline{\text{CE}}$	20	—	20	—	25	—		10
t _{DHW}	Data Hold Time from R/W	0	—	0	—	0	—		10
t _{DHC}	Data Hold Time from $\overline{\text{CE}}$	0	—	0	—	0	—		10
t _{ASC}	Address Setup Time	0	—	0	—	0	—		11
t _{AHC}	Address Hold Time	15	—	20	—	25	—		11
t _{FC}	Auto Refresh Cycle Time	130	—	130	—	160	—		
t _{RFD}	RFSH Delay Time from $\overline{\text{CE}}$	40	—	40	—	50	—		
t _{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000		12
t _{FP}	RFSH Precharge Time	30	—	30	—	30	—		12
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—		12
t _{FRS}	$\overline{\text{CE}}$ Delay Time from RFSH (Self Refresh)	160	—	160	—	190	—		12
t _{REF}	Refresh Period (2048 cycles, A0 ~ A10)	—	32	—	32	—	32	ms	
t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

Notes:

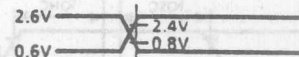
- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DDO} , I_{DDF3} , and I_{DDF4} depend on the cycle time.
- 4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_f = 5$ ns.

7) Timing reference levels

Input Levels

$$\begin{aligned} &: V_{IH} = 2.6V \\ &V_{IL} = 0.6V \end{aligned}$$

INPUT



Input Reference Levels

$$\begin{aligned} &: V_{IH} = 2.4V \\ &V_{IL} = 0.8V \end{aligned}$$

OUTPUT



Output Reference Levels

$$\begin{aligned} &: V_{OH} = 2.2V \\ &V_{OL} = 0.8V \end{aligned}$$

INPUT REFERENCE
LEVELOUTPUT REFERENCE
LEVEL

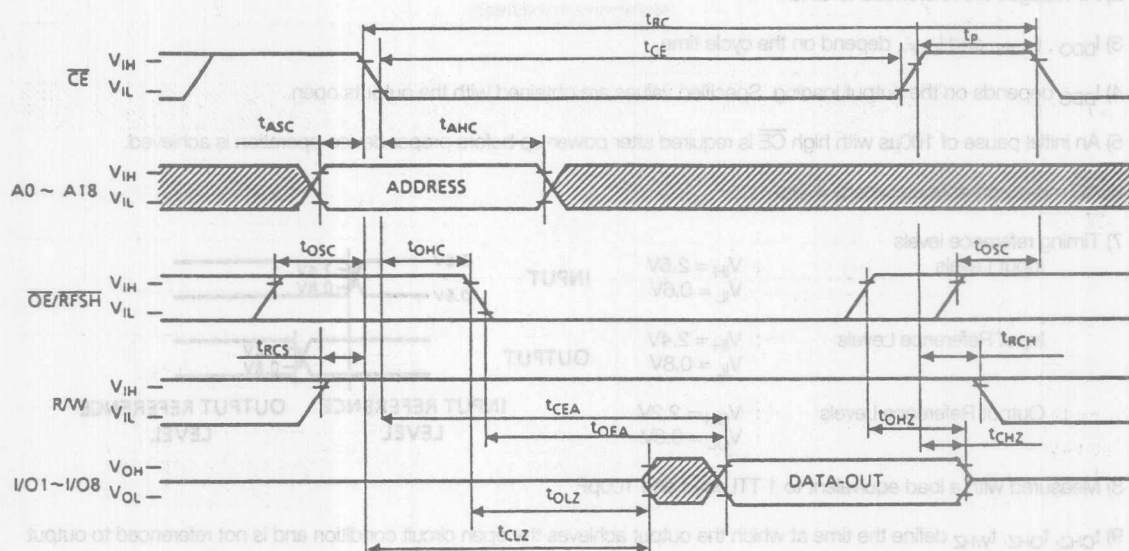
- 8) Measured with a load equivalent to 1 TTL load and 100pF.
- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) For write cycles, the input data is latched at the earlier of RW or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
- 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.
 Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

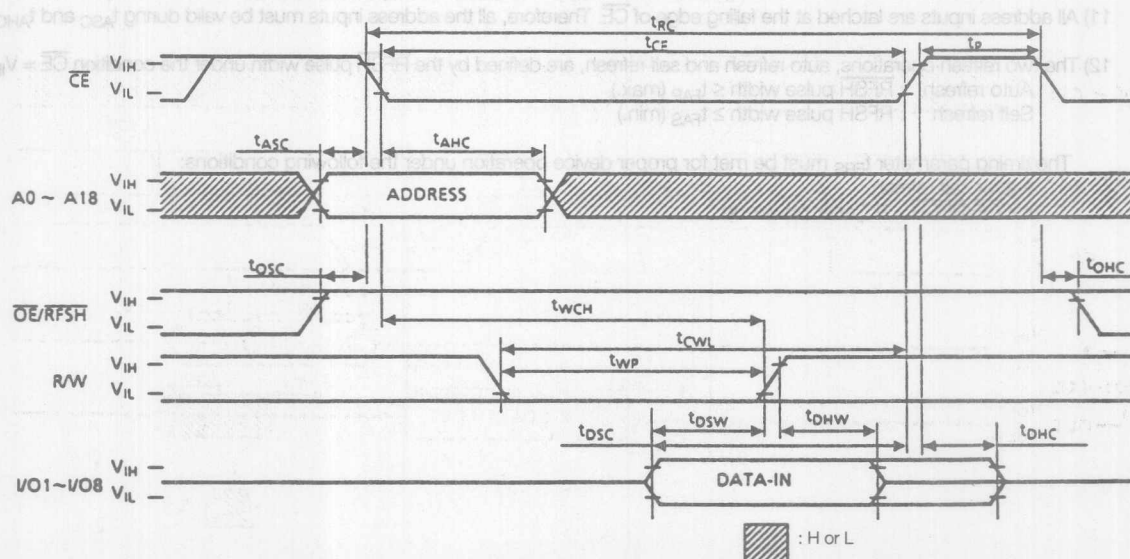
- after self refresh
- if $\overline{OE}/\overline{RFSH} = "L"$ after power-up

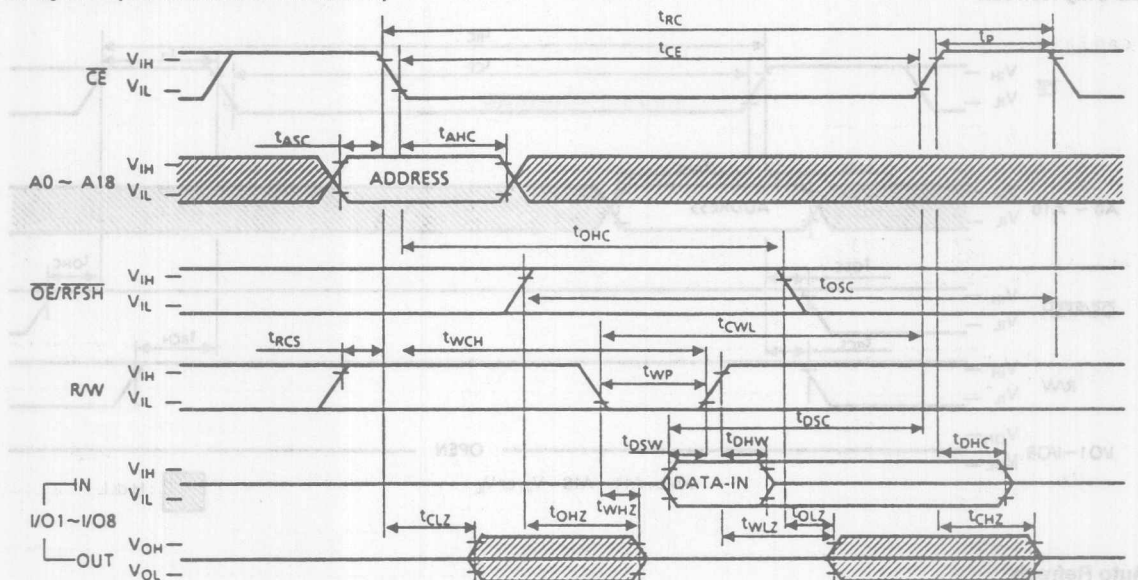
Timing Waveforms

Read Cycle

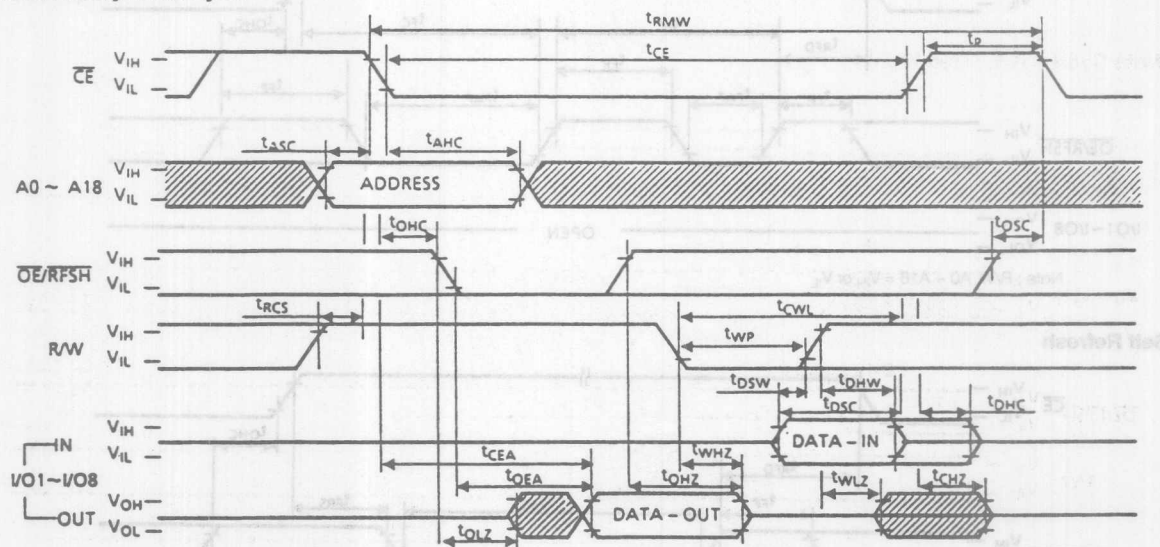


Write Cycle 1 (OE Fixed High)

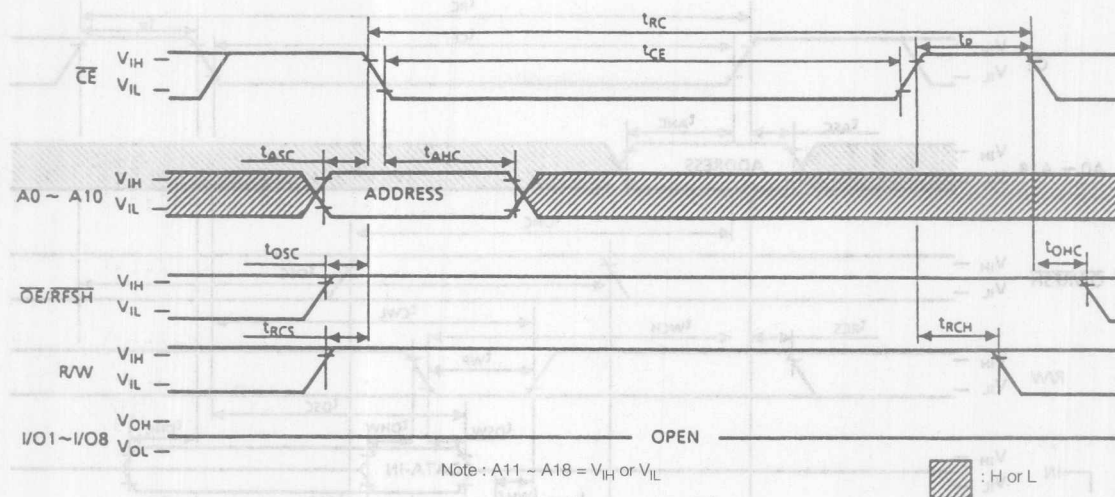
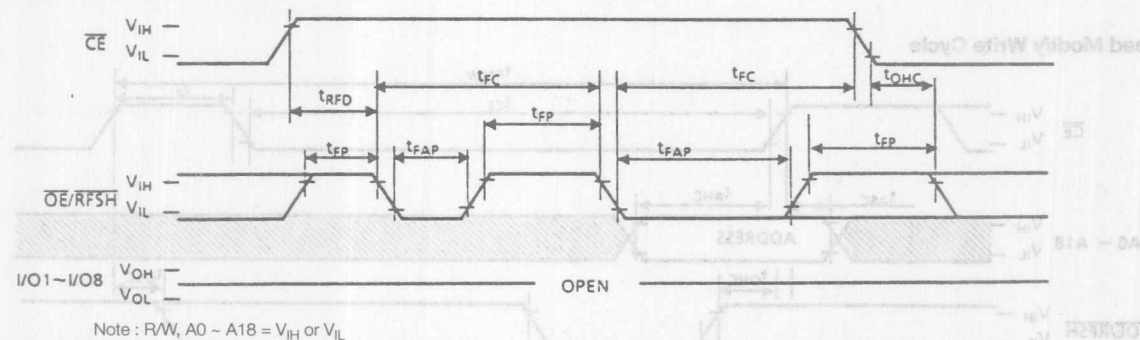
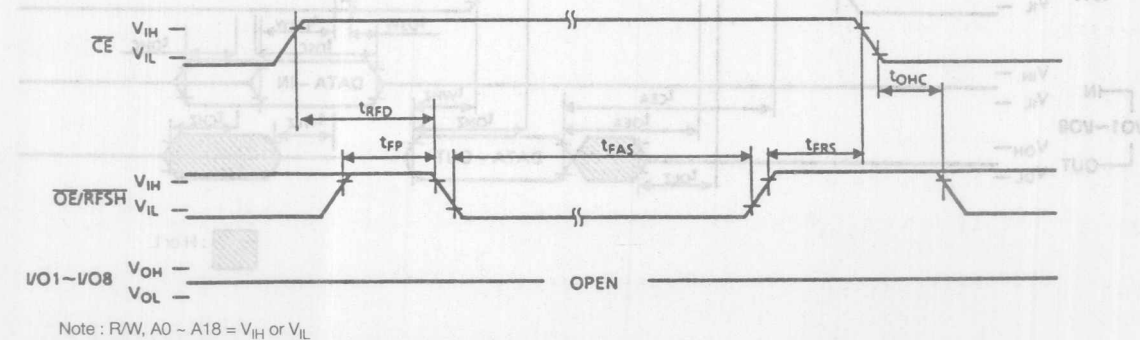


Write Cycle 2 (\overline{OE} Clocked or Fixed Low)

Read Modify Write Cycle



■ : H or L

\overline{CE} Only Refresh**Auto Refresh****Self Refresh**

TC518512PL/FL/FTL/TRL-70(LT)/80(LT)/10(LT)

SILICON GATE CMOS

524,288 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518512PL is a 4M bit high speed CMOS pseudo static RAM organized as 524,288 words by 8 bits. The TC518512PL utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518512PL operates from a single 5V power supply. Refreshing is supported by a refresh ($\overline{\text{OE}}/\text{RFSH}$) input which enables two types of refreshing - auto refresh and self refresh. The TC518512PL features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface. The TC518512PL-(LT) is guaranteed over an operating temperature range of $-20 \sim 70^\circ\text{C}$.

The TC518512PL is available in a 32-pin, 0.6 inch width plastic DIP, a small outline plastic flat package, and a thin small outline package (forward type, reverse type).

Features

- Organization: 524,288 words x 8 bits
- Single 5V power supply
- Fast access time

	TC518512PL-(LT) Family		
	-70	-80	-10
t_{CEA} $\overline{\text{CE}}$ Access Time	70ns	80ns	100ns
t_{OEA} $\overline{\text{OE}}$ Access Time	30ns	30ns	40ns
t_{RC} Cycle Time	115ns	130ns	160ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	220 μA		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Wide operating temperature: $-20 \sim 70^\circ\text{C}$
- Refresh: 2048 refresh cycles/32ms
- Package
 - TC518512PL: DIP32-P-600
 - TC518512FL: SOP32-P-525
 - TC518512FTL: TSOP32-P-400
 - TC518512TRL: TSOP32-P-400A

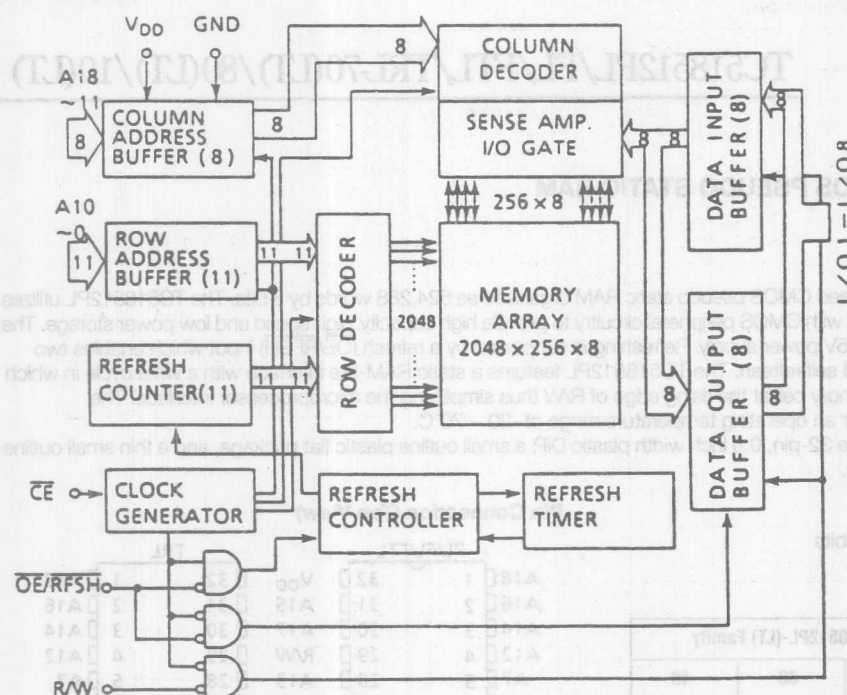
Pin Names

A0 ~ A18	Address Inputs
R/W	Read/Write Control Input
$\overline{\text{OE}}/\text{RFSH}$	Output Enable Input Refresh Input
$\overline{\text{CE}}$	Chip Enable Input
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

Pin Connection (Top View)

PL/FL/FTL				TRL			
A18	1	32	V_{DD}	32	1	A18	
A16	2	31	A15	31	2	A16	
A14	3	30	A17	30	3	A14	
A12	4	29	R/W	29	4	A12	
A7	5	28	A13	28	5	A7	
A6	6	27	A8	27	6	A6	
A5	7	26	A9	26	7	A5	
A4	8	25	A11	25	8	A4	
A3	9	24	$\overline{\text{OE}}/\text{RFSH}$	24	9	A3	
A2	10	23	A10	23	10	A2	
A1	11	22	$\overline{\text{CE}}$	22	11	A1	
A0	12	21	I/O8	21	12	A0	
I/O1	13	20	I/O7	20	13	I/O1	
I/O2	14	19	I/O6	19	14	I/O2	
I/O3	15	18	I/O5	18	15	I/O3	
GND	16	17	I/O4	17	16	GND	

Block Diagram



Operating Mode

MODE	PIN	CE	OE/RFSH	R/W	A0 ~ A18	I/O1 ~ 8
Read		L	L	H	V*	OUT
Write		L	*	L	V*	IN
CE only Refresh		L	H	H	V*	HZ
Auto/Self Refresh		H	L	*	*	HZ
Standby		H	H	*	*	HZ

H = High level input (V_{IH})L = Low level input (V_{IL})* = V_{IH} or V_{IL} V* = At the falling edge of \overline{CE} , all address inputs are latched. At all other times, the address inputs are **.

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	-20 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1.0$	V	
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics ($T_a = -20 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC \text{ min.}}$	70ns version	—	50	70	3,4
		80ns version	—	45	60	
		100ns version	—	35	50	
I_{DDS1}	Standby Current $\overline{CE} = V_{IH}$, $\overline{OE}/\overline{RFSH} = V_{IH}$	—	—	1	mA	
I_{DDS2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$, $\overline{OE}/\overline{RFSH} = V_{DD} - 0.2V$	—	—	200	μA	
I_{DDF1}	Self Refresh Current (Average) $\overline{CE} = V_{IH}$, $\overline{OE}/\overline{RFSH} = V_{IL}$	—	—	1	mA	
I_{DDF2}	Self Refresh Current (Average) $\overline{CE} = V_{DD} - 0.2V$, $\overline{OE}/\overline{RFSH} = 0.2V$	—	100	220	μA	
I_{DDF3}	Auto Refresh Current (Average) $\overline{OE}/\overline{RFSH}$ cycling: $t_{FC} = t_{FC \text{ min.}}$	70ns version	—	—	70	3
		80ns version	—	—	60	
		100ns version	—	—	50	
I_{DDF4}	\overline{CE} only Refresh Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC \text{ min.}}$	70ns version	—	—	70	3
		80ns version	—	—	60	
		100ns version	—	—	50	
$I_{IL(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = $0V$	—	—	± 10	μA	
$I_{OL(L)}$	Output Leakage Current Output Disabled ($\overline{CE} = V_{IH}$ or $\overline{OE}/\overline{RFSH} = V_{IH}$ or $R/W = V_{IL}$) $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level $I_{OH} = -1.0\text{mA}$	2.4	—	—	V	
V_{OL}	Output Low Level $I_{OL} = 2.1\text{mA}$	—	—	0.4	V	

Capacitance* ($V_{DD} = 5V$, $T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A18)	—	5	pF
C_{I2}	Input Capacitance (\overline{CE} , $\overline{OE}/\overline{RFSH}$, R/W)	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -20 ~ 70°C, V_{DD} = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	115	—	130	—	160	—		
t _{RMW}	Read Modify Write Cycle Time	165	—	180	—	220	—		
t _{CE}	$\overline{\text{CE}}$ Pulse Width	70	10,000	80	10,000	100	10,000		
t _p	$\overline{\text{CE}}$ Precharge Time	35	—	40	—	50	—		
t _{CEA}	$\overline{\text{CE}}$ Access Time	—	70	—	80	—	100		
t _{OEA}	$\overline{\text{OE}}$ Access Time	—	30	—	30	—	40		
t _{CLZ}	$\overline{\text{CE}}$ to Output in Low -Z	20	—	20	—	20	—		
t _{OLZ}	$\overline{\text{OE}}$ to Output in Low -Z	0	—	0	—	0	—		
t _{WLZ}	Output Active from End of Write	0	—	0	—	0	—		
t _{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	0	25	9	
t _{OHZ}	$\overline{\text{OE}}$ Disable to Output in High-Z	0	20	0	20	0	25	9	
t _{WHZ}	Write Enable to Output in High-Z	0	20	0	20	0	25	9	
t _{OSC}	$\overline{\text{OE}}$ Setup Time Referenced to $\overline{\text{CE}}$	10	—	10	—	10	—	9	
t _{OHC}	$\overline{\text{OE}}$ Hold Time Referenced to $\overline{\text{CE}}$	0	—	0	—	0	—	9	
t _{RCS}	Read Command Setup Time	0	—	0	—	0	—		
t _{RCH}	Read Command Hold Time	0	—	0	—	0	—	ns	
t _{WP}	Write Pulse Width	25	—	25	—	30	—		
t _{WCH}	Write Command Hold Time	40	—	40	—	50	—		
t _{CWL}	Write Command to $\overline{\text{CE}}$ Lead Time	25	—	25	—	30	—		
t _{DSW}	Data Setup Time from R/W	20	—	20	—	25	—	10	
t _{DSC}	Data Setup Time from $\overline{\text{CE}}$	20	—	20	—	25	—	10	
t _{DHW}	Data Hold Time from R/W	0	—	0	—	0	—	10	
t _{DHC}	Data Hold Time from $\overline{\text{CE}}$	0	—	0	—	0	—	10	
t _{ASC}	Address Setup Time	0	—	0	—	0	—	11	
t _{AHC}	Address Hold Time	15	—	20	—	25	—	11	
t _{FC}	Auto Refresh Cycle Time	130	—	130	—	160	—		
t _{RFD}	RFSH Delay Time from $\overline{\text{CE}}$	40	—	40	—	50	—		
t _{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	12	
t _{FP}	RFSH Precharge Time	30	—	30	—	30	—	12	
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—	12	
t _{FRS}	$\overline{\text{CE}}$ Delay Time from RFSH (Self Refresh)	160	—	160	—	190	—	12	
t _{REF}	Refresh Period (2048 cycles, A0 ~ A10)	—	32	—	32	—	32	ms	
t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

Notes:

- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DD0} , I_{DDF3} , and I_{DDF4} depend on the cycle time.
- 4) I_{DD0} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

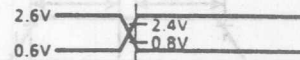
7) Timing reference levels

Input Levels

$$V_{IH} = 2.6V$$

$$V_{IL} = 0.6V$$

INPUT

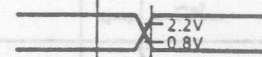


Input Reference Levels

$$V_{IH} = 2.4V$$

$$V_{IL} = 0.8V$$

OUTPUT



Output Reference Levels

$$V_{OH} = 2.2V$$

$$V_{OL} = 0.8V$$

INPUT REFERENCE
LEVELOUTPUT REFERENCE
LEVEL

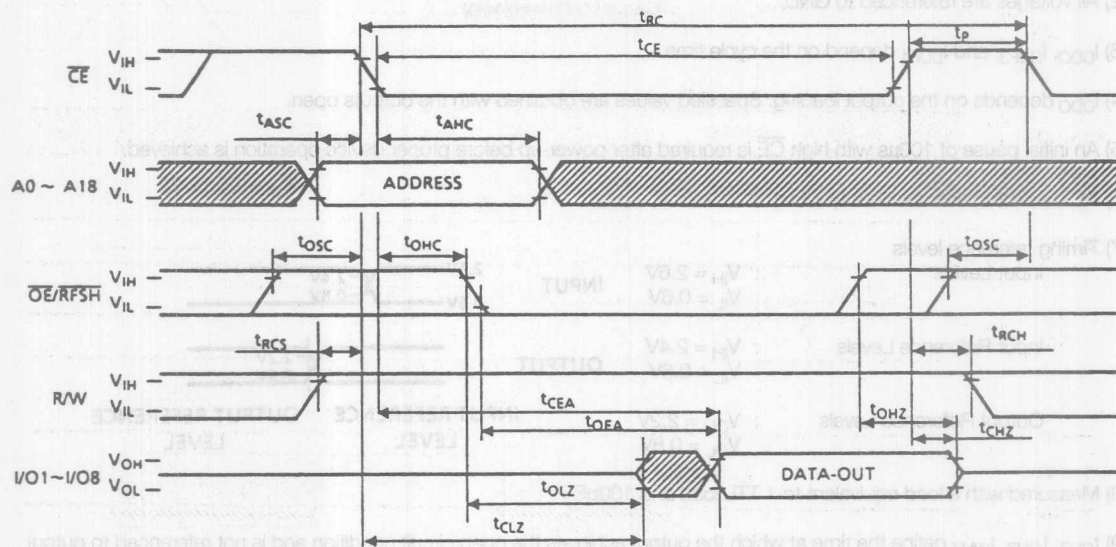
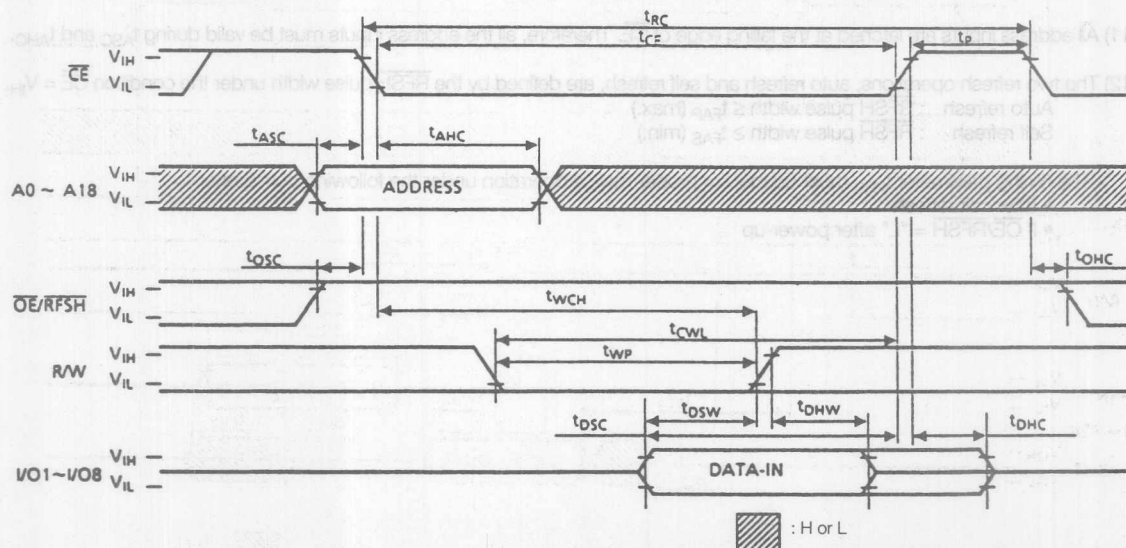
- 8) Measured with a load equivalent to 1 TTL load and 100pF.
- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) For write cycles, the input data is latched at the earlier of R/W or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
- 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.
 - Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 - Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

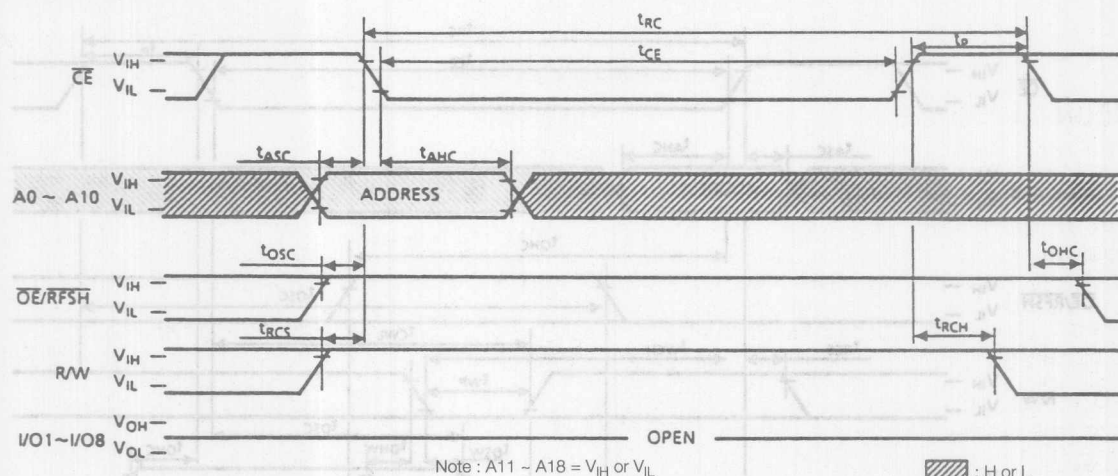
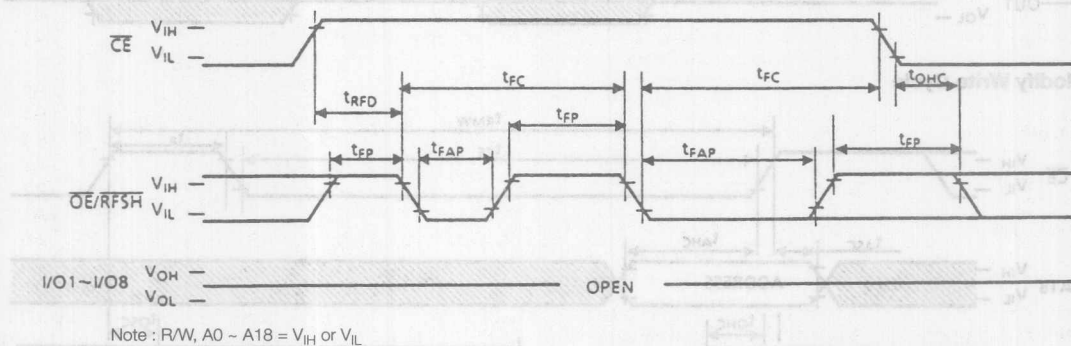
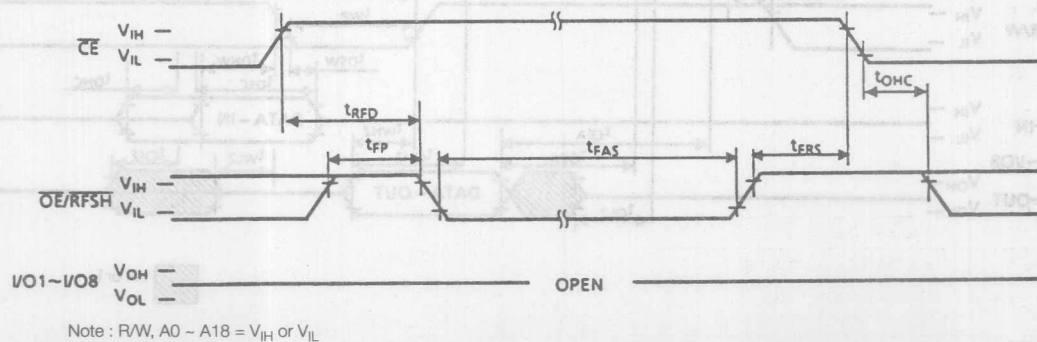
- after self refresh
- if $\overline{OE}/\overline{RFSH} = "L"$ after power-up

Timing Waveforms

Read Cycle

Write Cycle 1 (\overline{OE} Fixed High)



\overline{CE} Only Refresh**Auto Refresh****Self Refresh**

TC518512PL/FL/FTL/TRL-70(DR)/80(DR)/10(DR)

SILICON GATE CMOS

524,288 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518512PL is a 4M bit high speed CMOS pseudo static RAM organized as 524,288 words by 8 bits. The TC518512PL utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518512PL operates from a single 5V power supply. Refreshing is supported by a refresh ($\overline{OE}/RFSH$) input which enables two types of refreshing - auto refresh and self refresh. The TC518512PL features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

The TC518512PL is available in a 32-pin, 0.6 inch width plastic DIP, a small outline plastic flat package, and a thin small outline package (forward type, reverse type).

Features

- Organization: 524,288 words x 8 bits
- Single 5V power supply
- Data retention supply voltage: 3.0V ~ 5.5V
- Fast access time

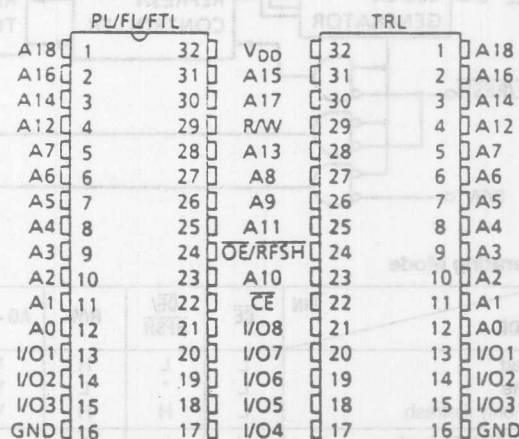
	TC518512PL-(DR) Family		
	-70	-80	-10
t_{CEA} \overline{CE} Access Time	70ns	80ns	100ns
t_{OEA} \overline{OE} Access Time	30ns	30ns	40ns
t_{RC} Cycle Time	115ns	130ns	160ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	5.5V	200 μ A	
	3.0V	100 μ A	

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 2048 refresh cycles/32ms
- Package
 - TC518512PL: DIP32-P-600
 - TC518512FL: SOP32-P-525
 - TC518512FTL: TSOP32-P-400
 - TC518512TRL: TSOP32-P-400A

Pin Names

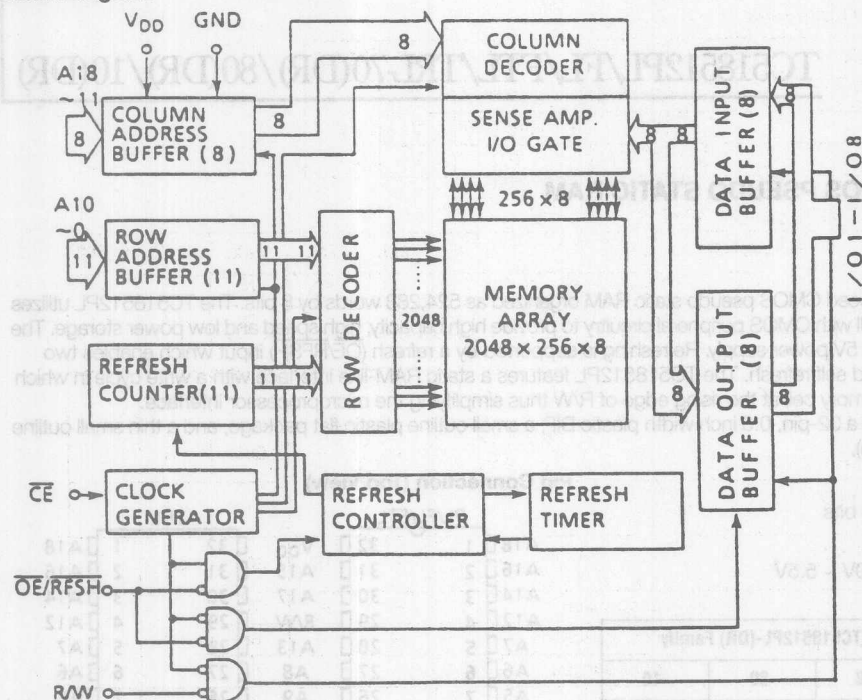
A0 ~ A18	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}/RFSH$	Output Enable Input Refresh Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

Pin Connection (Top View)



SYMBOL	UNIT	RATING	TEST
V_{DD}	V	4.5 - 5.5	Input Voltage
V_{OUT}	V	4.5 - 5.5	Output Voltage
V_{DD}	V	4.5 - 5.5	Power Supply Voltage
T_{amb}	°C	0 - 70	Operating Temperature
T_{stg}	°C	-55 - 150	Storage Temperature
t_{access}	ns	280 - 10	Access Time
P_d	mW	600	Power Dissipation
I_{out}	mA	80	Short Circuit Output Current

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	$\overline{OE/RFSH}$	R/W	A0 ~ A18	I/O1 ~ 8
Read		L	L	H	V*	OUT
Write		L	*	L	V*	IN
\overline{CE} only Refresh		L	H	H	V*	HZ
Auto/Self Refresh		H	L	*	*	HZ
Standby		H	H	*	*	HZ

H = High level input (V_{IH})L = Low level input (V_{IL})* = V_{IH} or V_{IL} V* = At the falling edge of \overline{CE} , all address inputs are latched. At all other times, the address inputs are "**".

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1.0$	V	
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC} \text{ min.}$	70ns version	—	50	70	mA 3,4
		80ns version	—	45	60	
		100ns version	—	35	50	
I_{DDS1}	Standby Current $\overline{CE} = V_{IH}$, $\overline{OE}/\overline{RFSH} = V_{IH}$	—	—	1	mA	
I_{DDS2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$, $\overline{OE}/\overline{RFSH} = V_{DD} - 0.2V$	—	—	200	μA	
I_{DDF1}	Self Refresh Current (Average) $\overline{CE} = V_{IH}$, $\overline{OE}/\overline{RFSH} = V_{IL}$	—	—	1	mA	
I_{DDF2}	Self Refresh Current (Average) $\overline{CE} = V_{DD} - 0.2V$, $\overline{OE}/\overline{RFSH} = 0.2V$	—	100	200	μA	
I_{DDF3}	Auto Refresh Current (Average) $\overline{OE}/\overline{RFSH}$ cycling: $t_{FC} = t_{FC} \text{ min.}$	70ns version	—	—	70	mA 3
		80ns version	—	—	60	
		100ns version	—	—	50	
I_{DDF4}	\overline{CE} only Refresh Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC} \text{ min.}$	70ns version	—	—	70	mA 3
		80ns version	—	—	60	
		100ns version	—	—	50	
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = $0V$	—	—	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disabled ($\overline{CE} = V_{IH}$ or $\overline{OE}/\overline{RFSH} = V_{IH}$ or $R/W = V_{IL}$) $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level $I_{OH} = -1.0\text{mA}$	2.4	—	—	V	
V_{OL}	Output Low Level $I_{OL} = 2.1\text{mA}$	—	—	0.4	V	

Capacitance* ($V_{DD} = 5V$, $T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A18)	—	5	pF
C_{I2}	Input Capacitance (\overline{CE} , $\overline{OE}/\overline{RFSH}$, R/W)	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	115	—	130	—	160	—		
t _{RMW}	Read Modify Write Cycle Time	165	—	180	—	220	—		
t _{CE}	CE Pulse Width	70	10,000	80	10,000	100	10,000		
t _p	CE Precharge Time	35	—	40	—	50	—		
t _{CEA}	CE Access Time	—	70	—	80	—	100		
t _{OEA}	OE Access Time	—	30	—	30	—	40		
t _{CLZ}	CE to Output in Low -Z	20	—	20	—	20	—		
t _{OLZ}	OE to Output in Low -Z	0	—	0	—	0	—		
t _{WLZ}	Output Active from End of Write	0	—	0	—	0	—		
t _{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	0	25		9
t _{OHZ}	OE Disable to Output in High-Z	0	20	0	20	0	25		9
t _{WHZ}	Write Enable to Output in High-Z	0	20	0	20	0	25		9
t _{OSC}	OE Setup Time Referenced to CE	10	—	10	—	10	—		9
t _{OHC}	OE Hold Time Referenced to CE	0	—	0	—	0	—		9
t _{RCS}	Read Command Setup Time	0	—	0	—	0	—		
t _{RCH}	Read Command Hold Time	0	—	0	—	0	—	ns	
t _{WP}	Write Pulse Width	25	—	25	—	30	—		
t _{WCH}	Write Command Hold Time	40	—	40	—	50	—		
t _{CWL}	Write Command to CE Lead Time	25	—	25	—	30	—		
t _{DSW}	Data Setup Time from R/W	20	—	20	—	25	—		10
t _{DSC}	Data Setup Time from CE	20	—	20	—	25	—		10
t _{DHW}	Data Hold Time from R/W	0	—	0	—	0	—		10
t _{DHC}	Data Hold Time from CE	0	—	0	—	0	—		10
t _{ASC}	Address Setup Time	0	—	0	—	0	—		11
t _{AHC}	Address Hold Time	15	—	20	—	25	—		11
t _{FC}	Auto Refresh Cycle Time	130	—	130	—	160	—		
t _{RFD}	RFSH Delay Time from CE	40	—	40	—	50	—		
t _{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000		12
t _{FP}	RFSH Precharge Time	30	—	30	—	30	—		12
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—		12
t _{FRS}	CE Delay Time from RFSH (Self Refresh)	160	—	160	—	190	—		12
t _{REF}	Refresh Period (2048 cycles, A0 ~ A10)	—	32	—	32	—	32	ms	
t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

Notes:

- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DD0} , I_{DDF3} , and I_{DDF4} depend on the cycle time.
- 4) I_{DD0} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

7) Timing reference levels

Input Levels

 $V_{IH} = 2.6V$
 $V_{IL} = 0.6V$

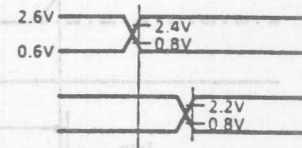
INPUT

Input Reference Levels

 $V_{IH} = 2.4V$
 $V_{IL} = 0.8V$

OUTPUT

Output Reference Levels

 $V_{OH} = 2.2V$
 $V_{OL} = 0.8V$
INPUT REFERENCE
LEVELOUTPUT REFERENCE
LEVEL

- 8) Measured with a load equivalent to 1 TTL load and 100pF.
- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) For write cycles, the input data is latched at the earlier of R/W or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
- 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.
 - Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 - Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

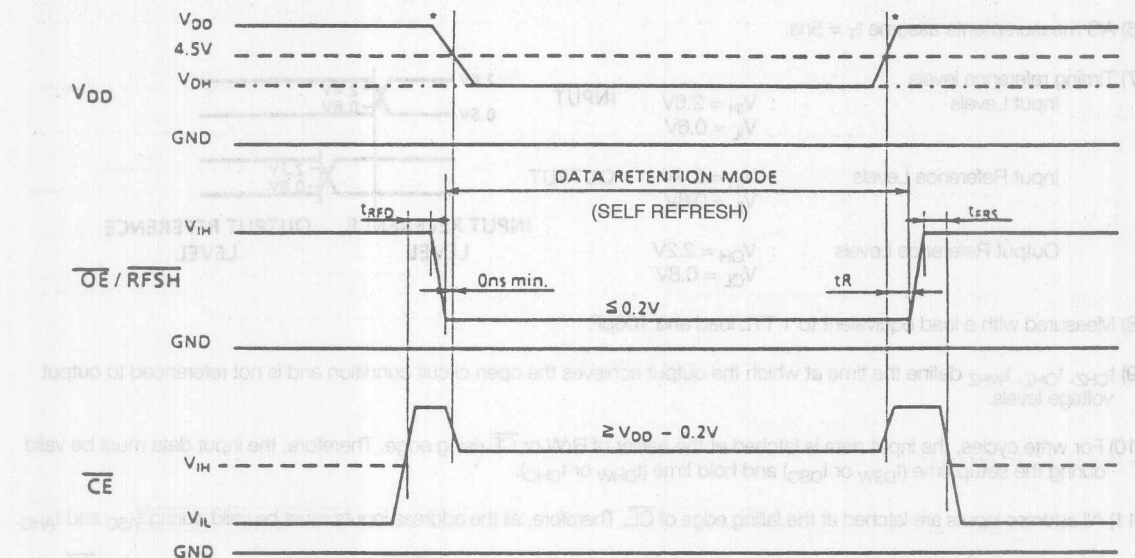
The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

- after self refresh
- if $\overline{OE}/\overline{RFSH} = "L"$ after power-up

Data Retention Characteristics ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	3.0	—	5.5	V
I_{DDF2}	Self Refresh Current	$V_{DH} = 3.0\text{V}$	—	50	μA
		$V_{DH} = 5.5\text{V}$	—	100	
t_R	Recovery Time	5	—	—	ms

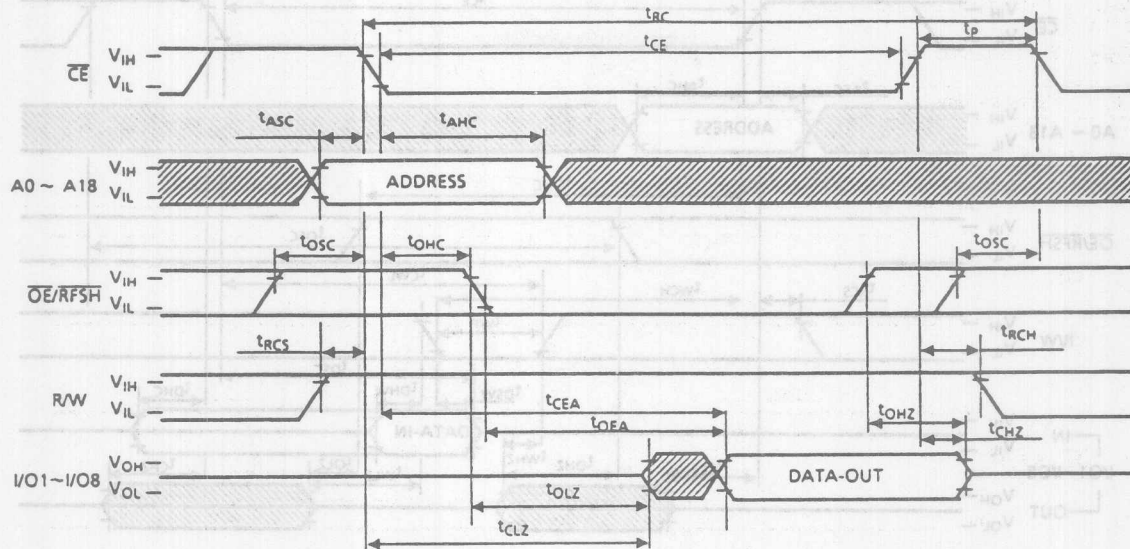
*The rising and falling slope of V_{DD} must be more than 50ms/V for proper device operation (20ms/V).



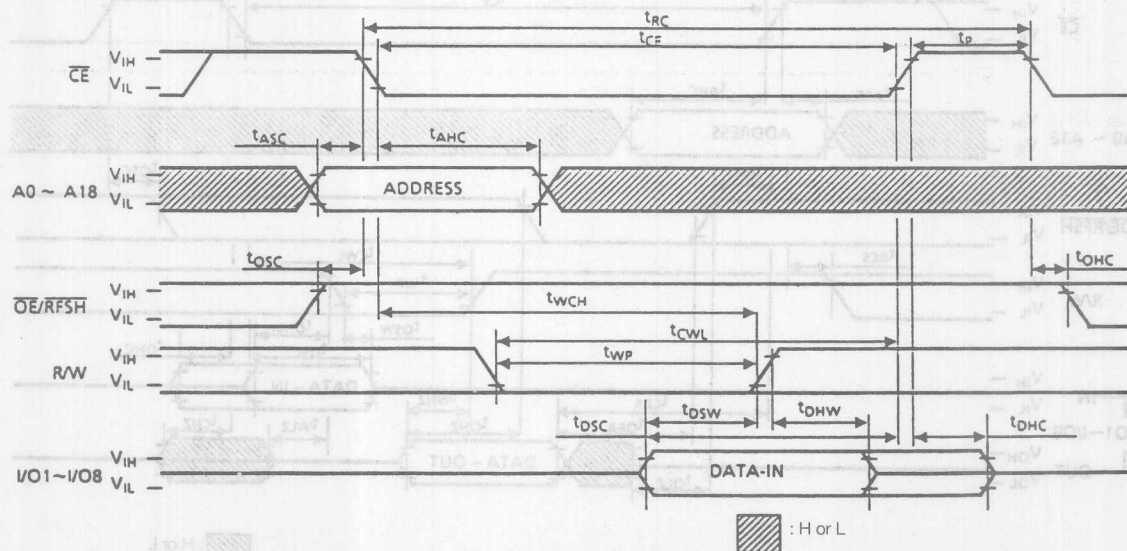
Notes: R/W, A0 ~ A18 = V_{IH} or V_{IL}
 I_{DDF1} is applicable when $\overline{OE}/\text{RFSH} = V_{IL}(\text{max.})$, $\overline{CE} = V_{IH}(\text{min.})$.

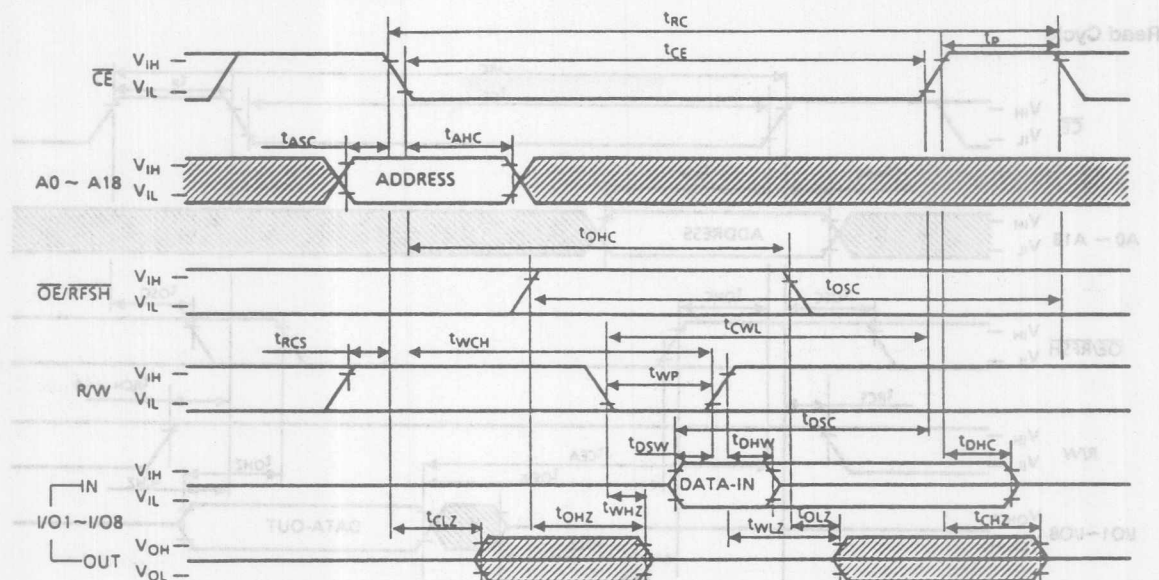
Timing Waveforms

Read Cycle

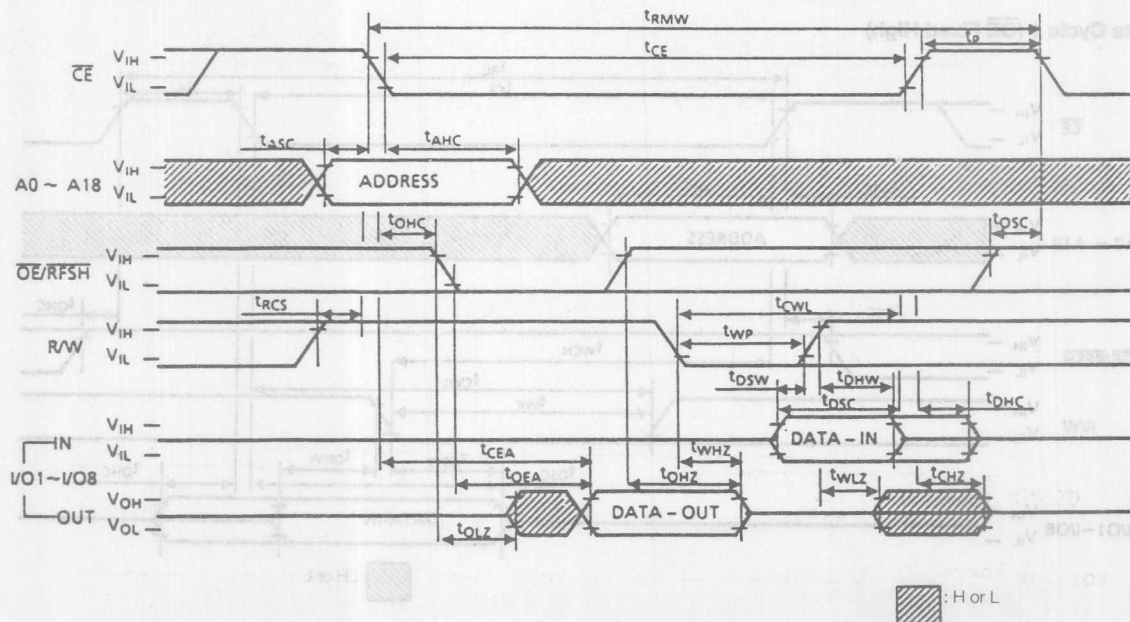


Write Cycle 1 (\overline{OE} Fixed High)

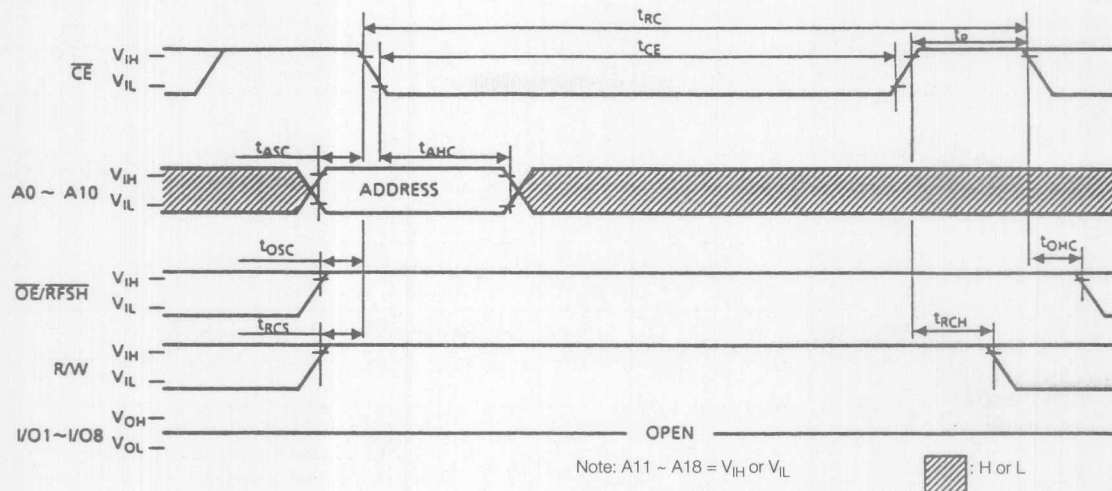


Write Cycle 2 ($\overline{\text{OE}}$ Clocked or Fixed Low)

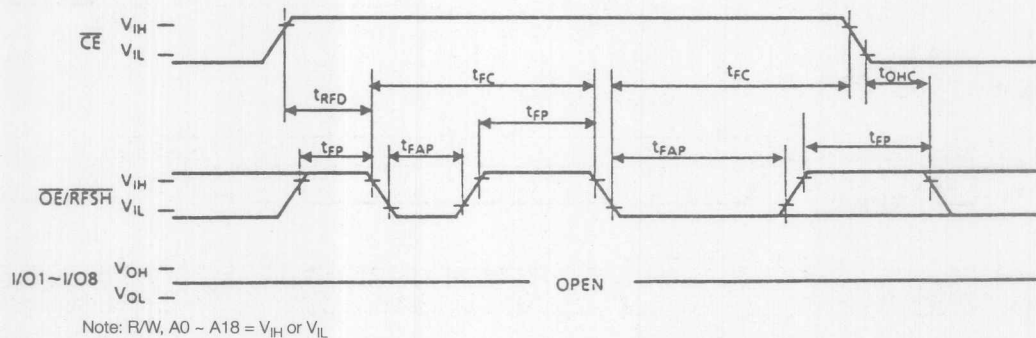
Read Modify Write Cycle



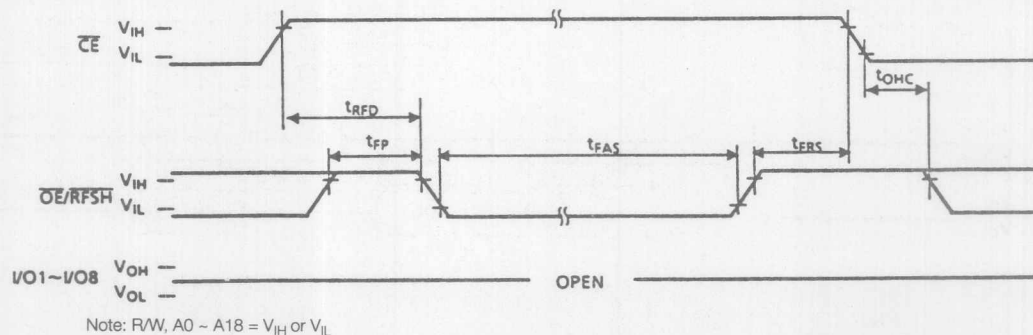
\overline{CE} Only Refresh



Auto Refresh



Self Refresh



Notes

TC518512PL/FL/FTL/TRL-70LV/80LV/10LV

SILICON GATE CMOS

524,288 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518512PL is a 4M bit high speed CMOS pseudo static RAM organized as 524,288 words by 8 bits. The TC518512PL utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518512PL-LV operates from a single 3.0V ~ 5.5V power supply. Refreshing is supported by a refresh ($\overline{OE}/\overline{RFSH}$) input which enables two types of refreshing - auto refresh and self refresh. The TC518512PL features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

The TC518512PL is available in a 32-pin, 0.6 inch width plastic DIP, a small outline plastic flat package, and a thin small outline package (forward type, reverse type).

Features

- Organization: 524,288 words x 8 bits
- Low voltage operation: 3.0V ~ 5.5V
- Data retention supply voltage: 3.0V ~ 5.5V
- Fast access time

	TC518512PL-LV Family		
	-70	-80	-10
t_{CEA} \overline{CE} Access Time	70ns	80ns	100ns
t_{OEA} \overline{OE} Access Time	30ns	30ns	40ns
t_{RC} Cycle Time	115ns	130ns	160ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	5.5V	200 μ A	
Self Refresh Current	3.0V	100 μ A	

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 2048 refresh cycles/32ms
- Package
 - TC518512PL: DIP32-P-600
 - TC518512FL: SOP32-P-525
 - TC518512FTL: TSOP32-P-400
 - TC518512TRL: TSOP32-P-400A

Pin Names

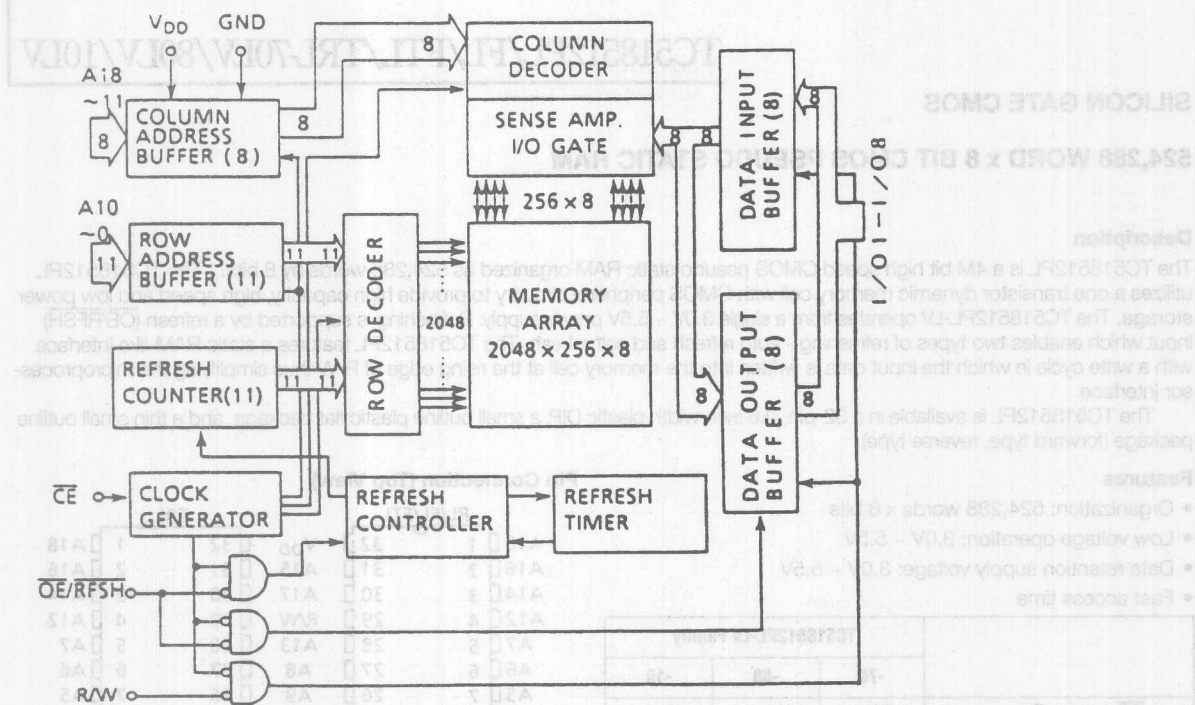
A0 ~ A18	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}/\overline{RFSH}$	Output Enable Input Refresh Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

Pin Connection (Top View)

PL/FL/FTL				TRL			
A18	1	32	V_{DD}	32	1	A18	
A16	2	31	A15	31	2	A16	
A14	3	30	A17	30	3	A14	
A12	4	29	R/W	29	4	A12	
A7	5	28	A13	28	5	A7	
A6	6	27	A8	27	6	A6	
A5	7	26	A9	26	7	A5	
A4	8	25	A11	25	8	A4	
A3	9	24	$\overline{OE}/\overline{RFSH}$	24	9	A3	
A2	10	23	A10	23	10	A2	
A1	11	22	\overline{CE}	22	11	A1	
A0	12	21	I/O8	21	12	A0	
I/O1	13	20	I/O7	20	13	I/O1	
I/O2	14	19	I/O6	19	14	I/O2	
I/O3	15	18	I/O5	18	15	I/O3	
GND	16	17	I/O4	17	16	GND	

SYMBOL	ITEM	UNIT	MAXIMUM
V_{in}	Input Voltage	V	-1.0 ~ 7.0
V_{out}	Output Voltage	V	-1.0 ~ 7.0
V_{DD}	Power Supply Voltage	V	-1.0 ~ 7.0
T_{op}	Operating Temperature	$^{\circ}$ C	0 ~ 70
T_{stg}	Storage Temperature	$^{\circ}$ C	-55 ~ 125
T_{acc}	Accelerating Temperature	$^{\circ}$ C/sec	200 ~ 10
P_d	Power Dissipation	W/m	800
I_{out}	Short Circuit Output Current	mA	50

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	$\overline{OE}/\overline{RFSH}$	R/W	A0 ~ A18	I/O1 ~ 8
Read		L	L	H	V*	OUT
Write		L	*	L	V*	IN
\overline{CE} only Refresh		L	H	H	V*	HZ
Auto/Self Refresh		H	L	*	*	HZ
Standby		H	H	*	*	HZ

H = High level input (V_{IH})L = Low level input (V_{IL})* = V_{IH} or V_{IL} V* = At the falling edge of \overline{CE} , all address inputs are latched. At all other times, the address inputs are "**".

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1.0$	V	
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC \min.}$	70ns version	—	50	70	mA 3,4
		80ns version	—	45	60	
		100ns version	—	35	50	
I_{DDs1}	Standby Current $\overline{CE} = V_{IH}$, $\overline{OE}/\overline{RFSH} = V_{IH}$	—	—	1	mA	
I_{DDs2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$, $\overline{OE}/\overline{RFSH} = V_{DD} - 0.2V$	—	—	200	μA	
I_{DDf1}	Self Refresh Current (Average) $\overline{CE} = V_{IH}$, $\overline{OE}/\overline{RFSH} = V_{IL}$	—	—	1	mA	
I_{DDf2}	Self Refresh Current (Average) $\overline{CE} = V_{DD} - 0.2V$, $\overline{OE}/\overline{RFSH} = 0.2V$	—	—	200	μA	
I_{DDf3}	Auto Refresh Current (Average) $\overline{OE}/\overline{RFSH}$ cycling: $t_{FC} = t_{FC \min.}$	70ns version	—	—	70	mA 3
		80ns version	—	—	60	
		100ns version	—	—	50	
I_{DDf4}	\overline{CE} only Refresh Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC \min.}$	70ns version	—	—	70	mA 3
		80ns version	—	—	60	
		100ns version	—	—	50	
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other inputs not under test = $0V$	—	—	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disabled ($\overline{CE} = V_{IH}$ or $\overline{OE}/\overline{RFSH} = V_{IH}$ or $R/W = V_{IL}$) $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level $I_{OH} = -1.0\text{mA}$	2.4	—	—	V	
V_{OL}	Output Low Level $I_{OL} = 2.1\text{mA}$	—	—	0.4	V	

Capacitance* ($V_{DD} = 5V$, $T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A18)	—	5	pF
C_{I2}	Input Capacitance (\overline{CE} , $\overline{OE}/\overline{RFSH}$, R/W)	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

SYMBOL	PARAMETER	MIN.		MAX.		MIN.		MAX.		UNIT	NOTES
t _{RC}	Random Read, Write Cycle Time	115	—	130	—	160	—				
t _{RMW}	Read Modify Write Cycle Time	165	—	180	—	220	—				
t _{CE}	\overline{CE} Pulse Width	70	10,000	80	10,000	100	10,000				
t _p	\overline{CE} Precharge Time	35	—	40	—	50	—				
t _{CEA}	\overline{CE} Access Time	—	70	—	80	—	100				
t _{OEa}	\overline{OE} Access Time	—	30	—	30	—	40				
t _{CLZ}	\overline{CE} to Output in Low -Z	20	—	20	—	20	—				
t _{OLZ}	\overline{OE} to Output in Low -Z	0	—	0	—	0	—				
t _{WLZ}	Output Active from End of Write	0	—	0	—	0	—				
t _{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	0	25			9	
t _{OHZ}	\overline{OE} Disable to Output in High-Z	0	20	0	20	0	25			9	
t _{WHZ}	Write Enable to Output in High-Z	0	20	0	20	0	25			9	
t _{OSC}	\overline{OE} Setup Time Referenced to \overline{CE}	10	—	10	—	10	—			9	
t _{OHC}	\overline{OE} Hold Time Referenced to \overline{CE}	0	—	0	—	0	—			9	
t _{RCS}	Read Command Setup Time	0	—	0	—	0	—				
t _{RCH}	Read Command Hold Time	0	—	0	—	0	—		ns		
t _{WP}	Write Pulse Width	25	—	25	—	30	—				
t _{WCH}	Write Command Hold Time	40	—	40	—	50	—				
t _{CWL}	Write Command to \overline{CE} Lead Time	25	—	25	—	30	—				
t _{DSW}	Data Setup Time from R/W	20	—	20	—	25	—			10	
t _{DSC}	Data Setup Time from \overline{CE}	20	—	20	—	25	—			10	
t _{DHW}	Data Hold Time from R/W	0	—	0	—	0	—			10	
t _{DHC}	Data Hold Time from \overline{CE}	0	—	0	—	0	—			10	
t _{ASC}	Address Setup Time	0	—	0	—	0	—			11	
t _{AHC}	Address Hold Time	15	—	20	—	25	—			11	
t _{FC}	Auto Refresh Cycle Time	130	—	130	—	160	—				
t _{RFD}	RFSH Delay Time from \overline{CE}	40	—	40	—	50	—				
t _{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000			12	
t _{FP}	RFSH Precharge Time	30	—	30	—	30	—			12	
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—			12	
t _{FRS}	\overline{CE} Delay Time from RFSH (Self Refresh)	160	—	160	—	190	—			12	
t _{REF}	Refresh Period (2048 cycles, A0 ~ A10)	—	32	—	32	—	32	ms			
t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns			

3.3V Operation

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V	2
V_{IH}	Input High Voltage	$V_{DD} - 0.2V$	—	$V_{DD} + 1.0$	V	
V_{IL}	Input Low Voltage	-0.5	—	0.2	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 3.3V \pm 0.3V$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) CE, Address cycling: $t_{RC} = t_{RC \text{ min.}}$	—	15	20	mA	3,4
I_{DDS2}	Standby Current	—	—	100	μA	
I_{DDF2}	Self Refresh Current (Average)	—	50	100	μA	
I_{DDF3}	Auto Refresh Current (Average) RFSH cycling: $t_{FC} = t_{FC \text{ min.}}$	—	—	20	mA	3
I_{DDF4}	CE only Refresh Current (Average) CE, Address cycling: $t_{RC} = t_{RC \text{ min.}}$	—	—	20	mA	3
I_{IL}	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = 0V	—	—	± 10	μA	
I_{OL}	Output Leakage Current Output Disabled, $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level, $I_{OH} = -100\mu\text{A}$	$V_{DD} - 0.2V$	—	—	V	
V_{OL}	Output Low Level, $I_{OL} = 100\mu\text{A}$	—	—	0.2	V	

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 3.3V \pm 0.3V$) (Notes: 5, 6, 8)

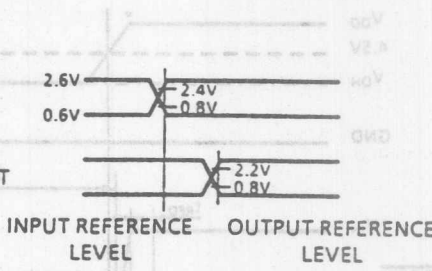
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t_{RC}	Random Read, Write Cycle Time	230	—		
t_{RMW}	Read Modify Write Cycle Time	305	—		
t_{CE}	\overline{CE} Pulse Width	150	10,000		
t_p	\overline{CE} Precharge Time	80	—		
t_{CEA}	\overline{CE} Access Time	—	150		
t_{OEA}	\overline{OE} Access Time	—	80		
t_{CLZ}	\overline{CE} to Output in Low -Z	20	—		
t_{OLZ}	\overline{OE} to Output in Low -Z	5	—		
t_{WLZ}	Output Active from End of Write	5	—		
t_{CHZ}	Chip Disable to Output in High-Z	0	30		9
t_{OHZ}	\overline{OE} Disable to Output in High-Z	0	30		9
t_{WHZ}	Write Enable to Output in High-Z	0	30		9
t_{OSC}	\overline{OE} Setup Time Referenced to \overline{CE}	10	—		9
t_{OHC}	\overline{OE} Hold Time Referenced to \overline{CE}	15	—		9
t_{RCS}	Read Command Setup Time	0	—		
t_{RCH}	Read Command Hold Time	0	—	ns	
t_{WP}	Write Pulse Width	35	—		
t_{WCH}	Write Command Hold Time	70	—		
t_{CWL}	Write Command to \overline{CE} Lead Time	35	—		
t_{DSW}	Data Setup Time from R/W	30	—		10
t_{DSC}	Data Setup Time from \overline{CE}	30	—		10
t_{DHW}	Data Hold Time from R/W	0	—		10
t_{DHC}	Data Hold Time from \overline{CE}	0	—		10
t_{ASC}	Address Setup Time	0	—		11
t_{AHC}	Address Hold Time	30	—		11
t_{FC}	Auto Refresh Cycle Time	230	—		
t_{RFD}	RFSH Delay Time from \overline{CE}	80	—		
t_{FAP}	RFSH Pulse Width (Auto Refresh)	80	8,000		12
t_{FP}	RFSH Precharge Time	50	—		12
t_{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—		12
t_{FRS}	\overline{CE} Delay Time from RFSH (Self Refresh)	300	—		12
t_{REF}	Refresh Period (2048 cycles, A0 ~ A10)	—	32	ms	
t_T	Transition Time (Rise and Fall)	3	50	ns	

Timing Reference Levels:

Input Reference Levels: 1.5V/1.5V

Output Reference Levels: 1.5V/1.5V

Notes:

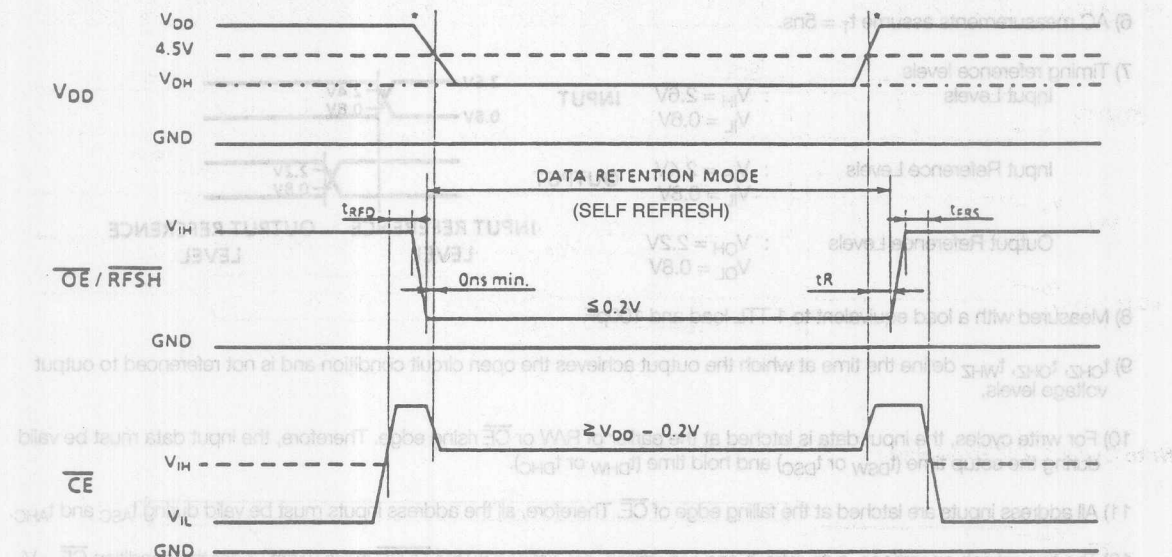
- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
 - 2) All voltages are referenced to GND.
 - 3) I_{DD0} , I_{DDF3} , and I_{DDF4} depend on the cycle time.
 - 4) I_{DD0} depends on the output loading. Specified values are obtained with the outputs open.
 - 5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.
 - 6) AC measurements assume $t_T = 5$ ns.
 - 7) Timing reference levels
 Input Levels : $V_{IH} = 2.6V$
 : $V_{IL} = 0.6V$
 Input Reference Levels : $V_{IH} = 2.4V$
 : $V_{IL} = 0.8V$
 Output Reference Levels : $V_{OH} = 2.2V$
 : $V_{OL} = 0.8V$
- 
- 8) Measured with a load equivalent to 1 TTL load and 100pF.
 - 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 - 10) For write cycles, the input data is latched at the earlier of R/W or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
 - 11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
 - 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.
 Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

- after self refresh
- if $\overline{OE}/\overline{RFSH} = "L"$ after power-up

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	3.0	—	5.5	V
I_{DDF2}	Self Refresh Current	$V_{DH} = 3.0V$	—	50	μA
		$V_{DH} = 5.5V$	—	100	
t_R	Recovery Time	5	—	—	ms

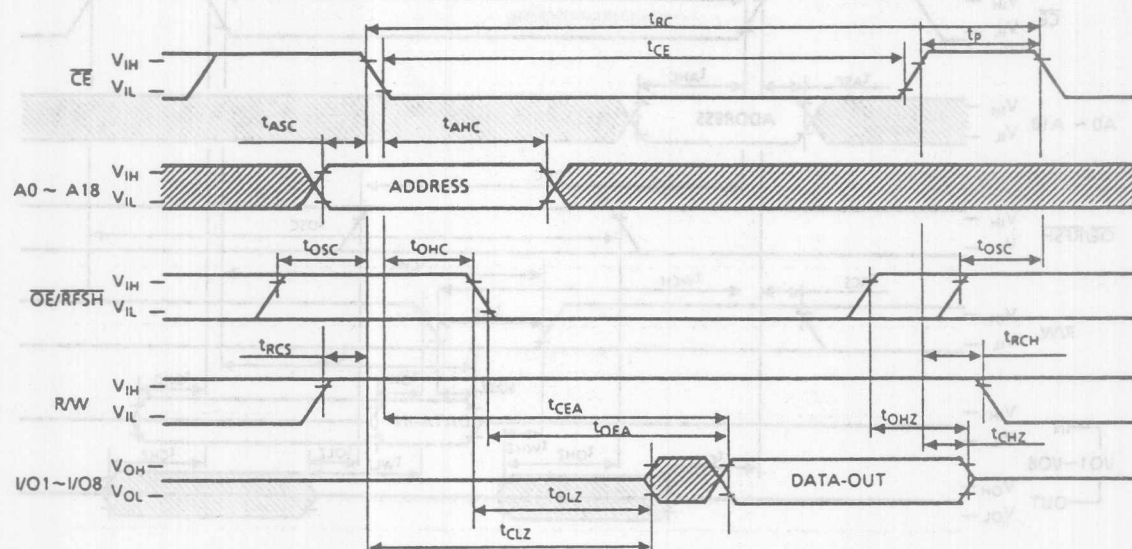
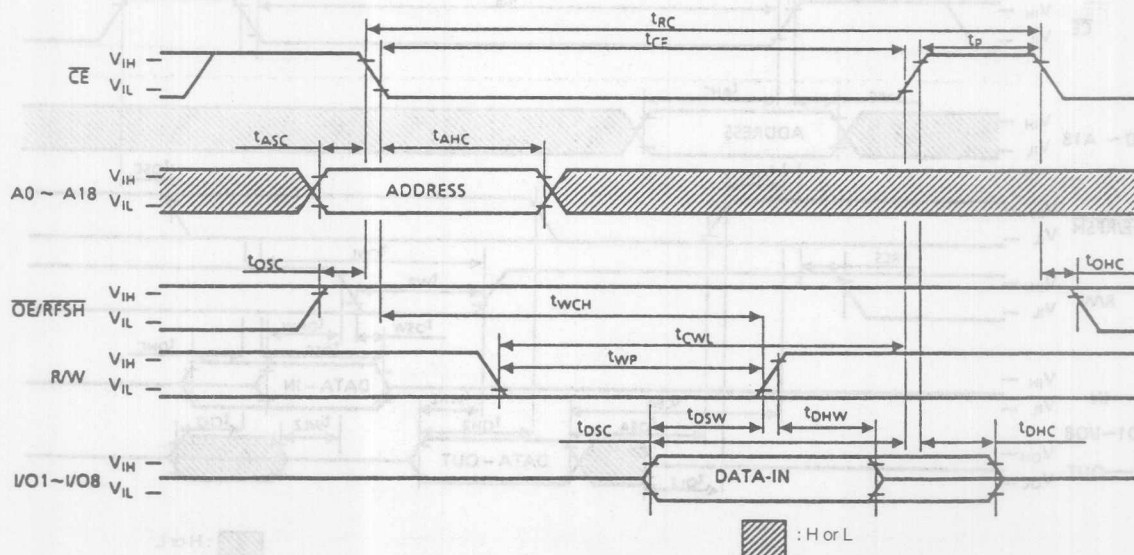
*The rising and falling slope of V_{DD} must be more than 50ms for proper device operation (20ms/V).

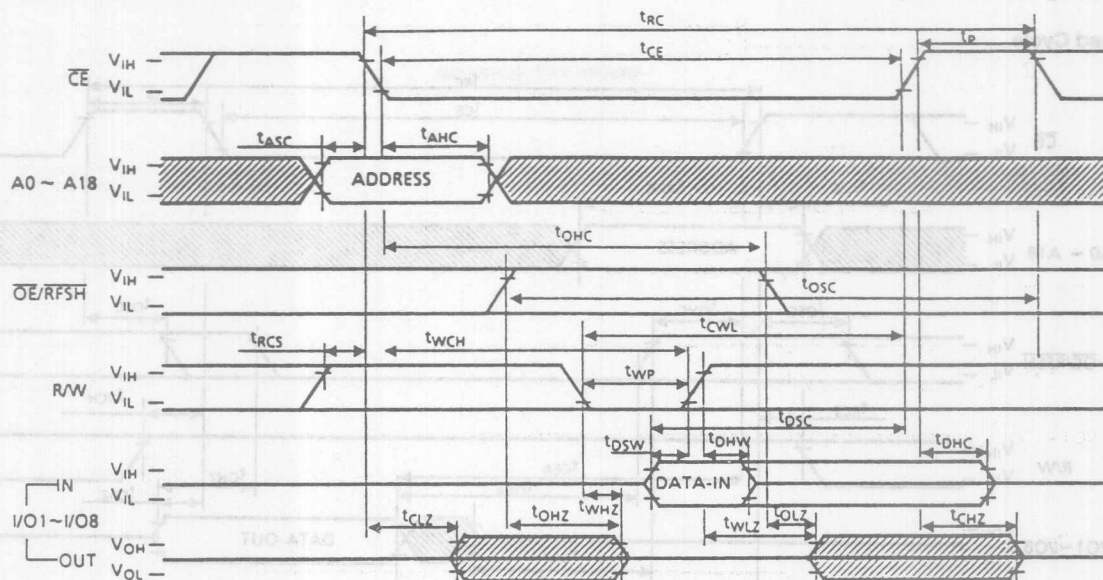


Notes: $RW, A0 \sim A18 = V_{IH}$ or V_{IL}
 I_{DDF1} is applicable when $\overline{OE} / \overline{RFSH} = V_{IL}$ (max.), $\overline{CE} = V_{IH}$ (min.).

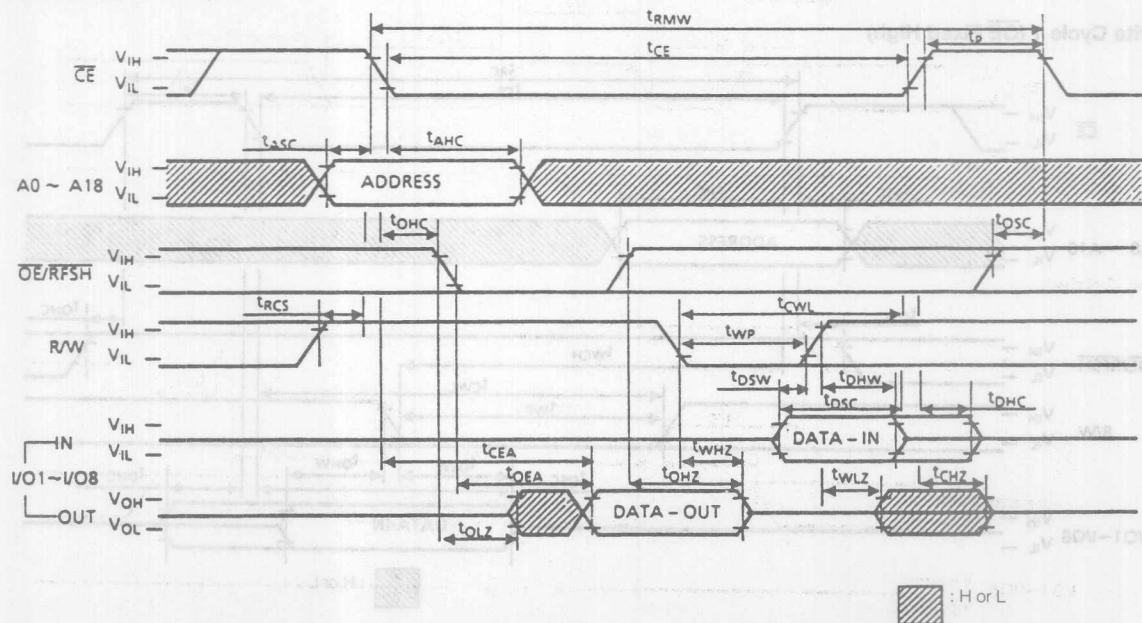
Timing Waveforms

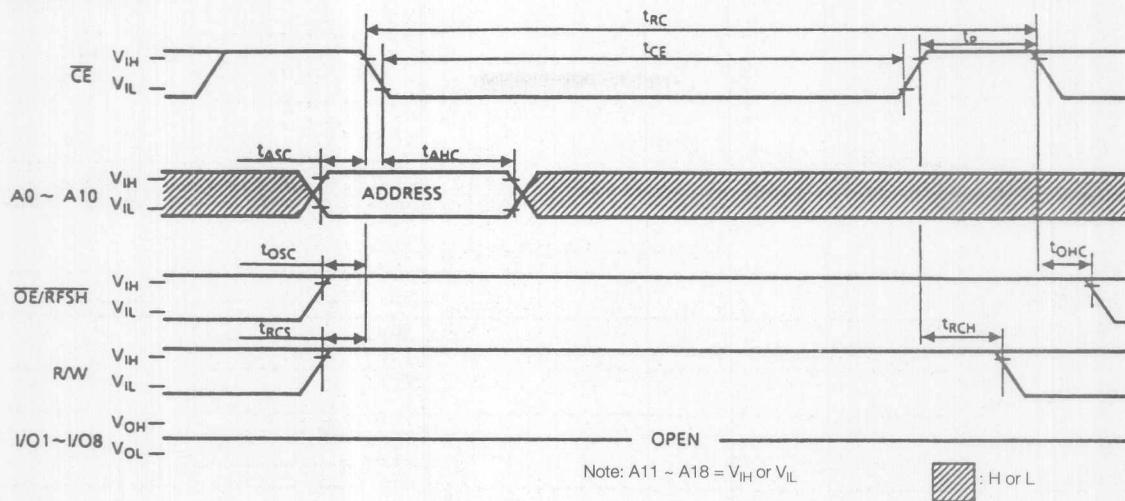
Read Cycle

Write Cycle 1 (\overline{OE} Fixed High)

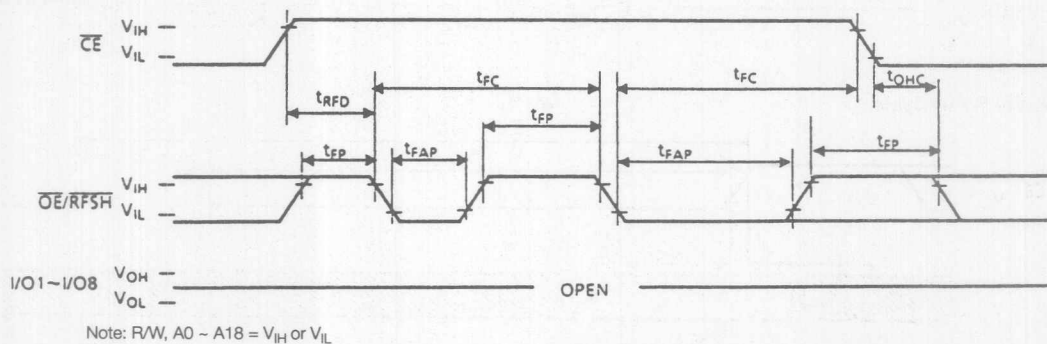
Write Cycle 2 (\overline{OE} Clocked or Fixed Low)

Read Modify Write Cycle

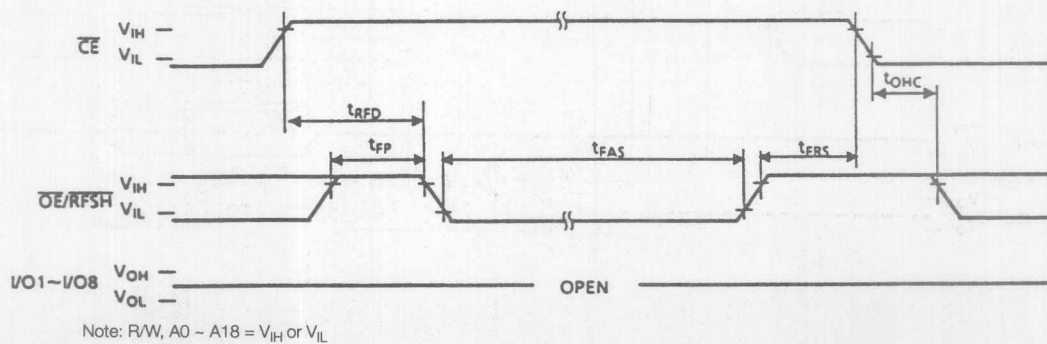


\overline{CE} Only Refresh

Auto Refresh



Self Refresh



TC518512PI/FI-80/10

SILICON GATE CMOS

524,288 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518512PI is a 4M bit high speed CMOS pseudo static RAM organized as 524,288 words by 8 bits. The TC518512PI utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518512PI operates from a single 5V power supply. Refreshing is supported by a refresh ($\overline{OE}/RFSH$) input which enables two types of refreshing - auto refresh and self refresh. The TC518512PI features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface. The TC518512PI is guaranteed over an operating temperature range of $-40 \sim 85^{\circ}\text{C}$.

The TC518512PI is available in a 32-pin, 0.6 inch width plastic DIP and a small outline plastic flat package.

Features

- Organization: 524,288 words x 8 bits
- Single 5V power supply
- Fast access time

	TC518512PI Family	
	-80	-10
t_{CEA} \overline{CE} Access Time	80ns	100ns
t_{OEA} \overline{OE} Access Time	30ns	40ns
t_{RC} Cycle Time	130ns	160ns
Power Dissipation	330mW	275mW
Self Refresh Current	300 μA	

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Wide operating temperature: $-40 \sim 85^{\circ}\text{C}$
- Inputs and outputs TTL compatible
- Refresh: 2048 refresh cycles/32ms
- Package
 - TC518512PI: DIP32-P-600
 - TC518512FI: SOP32-P-525

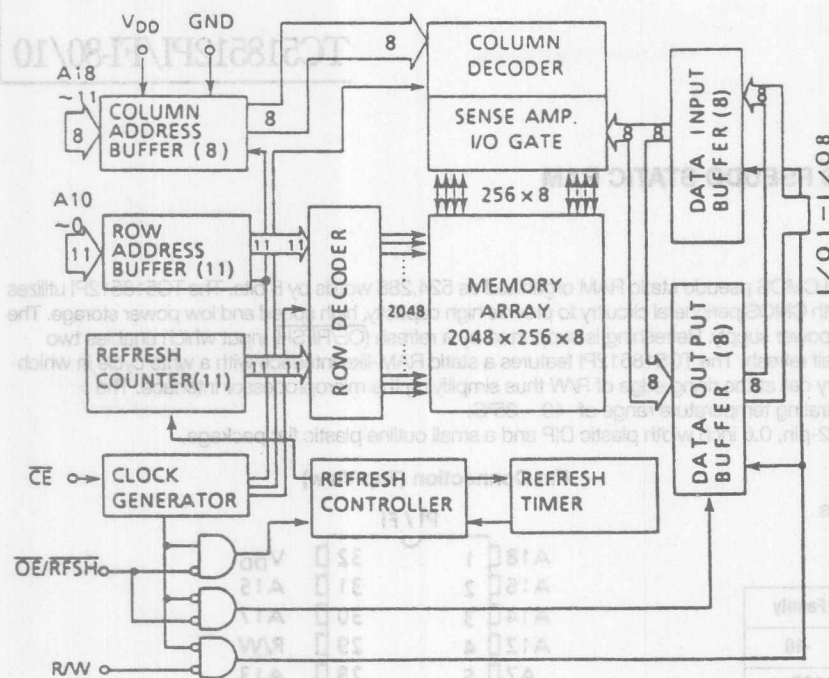
Pin Names

A0 ~ A18	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}/RFSH$	Output Enable Input Refresh Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

Pin Connection (Top View)

A18	1	32	V_{DD}
A16	2	31	A15
A14	3	30	A17
A12	4	29	R/W
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	$\overline{OE}/RFSH$
A2	10	23	A10
A1	11	22	\overline{CE}
A0	12	21	I/O8
I/O1	13	20	I/O7
I/O2	14	19	I/O6
I/O3	15	18	I/O5
GND	16	17	I/O4

Block Diagram



Operating Mode

MODE	PIN	CE	OE/ RFSH	R/W	A0 ~ A18	I/O1 ~ 8
Read		L	L	H	V*	OUT
Write		L	*	L	V*	IN
CE only Refresh		L	H	H	V*	HZ
Auto/Self Refresh		H	L	*	*	HZ
Standby		H	H	*	*	HZ

H = High level input (V_{IH})L = Low level input (V_{IL})* = V_{IH} or V_{IL} V* = At the falling edge of \overline{CE} , all address inputs are latched. At all other times, the address inputs are ***.

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	-40 ~ 85	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1.0$	V	
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	

DC Characteristics ($T_a = -40 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC \text{ min.}}$	80ns version	—	45	60	mA 3,4
		100ns version	—	35	50	
I_{DDS1}	Standby Current $\overline{CE} = V_{IH}$, $\overline{OE}/\overline{RFSH} = V_{IH}$	—	—	1	mA	
I_{DDS2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$, $\overline{OE}/\overline{RFSH} = V_{DD} - 0.2V$	—	—	200	μA	
I_{DDF1}	Self Refresh Current (Average) $\overline{CE} = V_{IH}$, $\overline{OE}/\overline{RFSH} = V_{IL}$	—	—	1	mA	
I_{DDF2}	Self Refresh Current (Average) $\overline{CE} = V_{DD} - 0.2V$, $\overline{OE}/\overline{RFSH} = 0.2V$	—	—	300	μA	
I_{DDF3}	Auto Refresh Current (Average) $\overline{OE}/\overline{RFSH}$ cycling: $t_{FC} = t_{FC \text{ min.}}$	80ns version	—	—	60	mA 3
		100ns version	—	—	50	
I_{DDF4}	\overline{CE} only Refresh Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC \text{ min.}}$	80ns version	—	—	60	mA 3
		100ns version	—	—	50	
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = $0V$	—	—	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disabled ($\overline{CE} = V_{IH}$ or $\overline{OE}/\overline{RFSH} = V_{IH}$ or $R/W = V_{IL}$) $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level $I_{OH} = -1.0\text{mA}$	2.4	—	—	V	
V_{OL}	Output Low Level $I_{OL} = 2.1\text{mA}$	—	—	0.4	V	

Capacitance* ($V_{DD} = 5V$, $T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A18)	—	5	pF
C_{I2}	Input Capacitance (\overline{CE} , $\overline{OE}/\overline{RFSH}$, R/W)	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics ($T_a = -40 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	130	—	160	—		
t_{RMW}	Read Modify Write Cycle Time	180	—	220	—		
t_{CE}	\overline{CE} Pulse Width	80	10,000	100	10,000		
t_p	\overline{CE} Precharge Time	40	—	50	—		
t_{CEA}	\overline{CE} Access Time	—	80	—	100		
t_{OEA}	\overline{OE} Access Time	—	30	—	40		
t_{CLZ}	\overline{CE} to Output in Low -Z	20	—	20	—		
t_{OLZ}	\overline{OE} to Output in Low -Z	0	—	0	—		
t_{WLZ}	Output Active from End of Write	0	—	0	—		
t_{CHZ}	Chip Disable to Output in High-Z	0	20	0	25		9
t_{OHZ}	\overline{OE} Disable to Output in High-Z	0	20	0	25		9
t_{WHZ}	Write Enable to Output in High-Z	0	20	0	25		9
t_{OSC}	\overline{OE} Setup Time Referenced to \overline{CE}	10	—	10	—		9
t_{OHC}	\overline{OE} Hold Time Referenced to \overline{CE}	0	—	0	—		9
t_{RCS}	Read Command Setup Time	0	—	0	—		
t_{RCH}	Read Command Hold Time	0	—	0	—	ns	
t_{WP}	Write Pulse Width	25	—	30	—		
t_{WCH}	Write Command Hold Time	40	—	50	—		
t_{CWL}	Write Command to \overline{CE} Lead Time	25	—	30	—		
t_{DSW}	Data Setup Time from R/W	20	—	25	—		10
t_{DSC}	Data Setup Time from \overline{CE}	20	—	25	—		10
t_{DHW}	Data Hold Time from R/W	0	—	0	—		10
t_{DHC}	Data Hold Time from \overline{CE}	0	—	0	—		10
t_{ASC}	Address Setup Time	0	—	0	—		11
t_{AHC}	Address Hold Time	20	—	25	—		11
t_{FC}	Auto Refresh Cycle Time	130	—	160	—		
t_{RFD}	\overline{RFSH} Delay Time from \overline{CE}	40	—	50	—		
t_{FAP}	\overline{RFSH} Pulse Width (Auto Refresh)	30	8,000	30	8,000		12
t_{FP}	\overline{RFSH} Precharge Time	30	—	30	—		12
t_{FAS}	\overline{RFSH} Pulse Width (Self Refresh)	8,000	—	8,000	—		12
t_{FRS}	\overline{CE} Delay Time from \overline{RFSH} (Self Refresh)	160	—	190	—		12
t_{REF}	Refresh Period (2048 cycles, A0 ~ A10)	—	32	—	32	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	

This parameter is statistically guaranteed and is not 100% tested.

Notes:

- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DD0} , I_{DDF3} , and I_{DDF4} depend on the cycle time.
- 4) I_{DD0} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

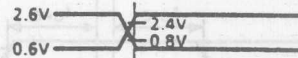
7) Timing reference levels

Input Levels

$$: V_{IH} = 2.6V$$

$$V_{IL} = 0.6V$$

INPUT

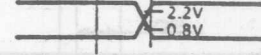


Input Reference Levels

$$: V_{IH} = 2.4V$$

$$V_{IL} = 0.8V$$

OUTPUT



Output Reference Levels

$$: V_{OH} = 2.2V$$

$$V_{OL} = 0.8V$$

INPUT REFERENCE
LEVELOUTPUT REFERENCE
LEVEL

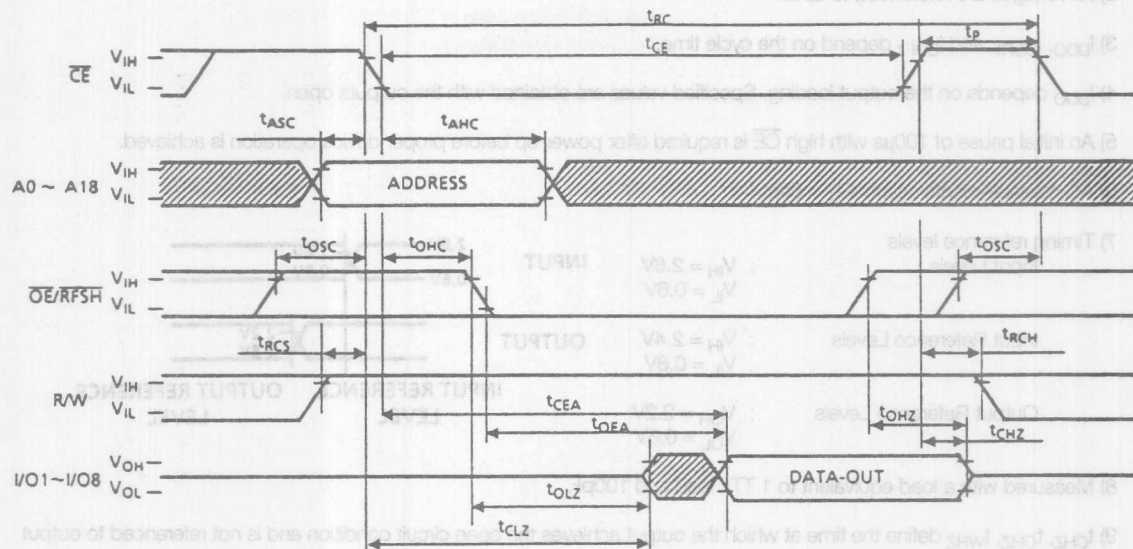
- 8) Measured with a load equivalent to 1 TTL load and 100pF.
- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) For write cycles, the input data is latched at the earlier of R/W or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
- 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.
 Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

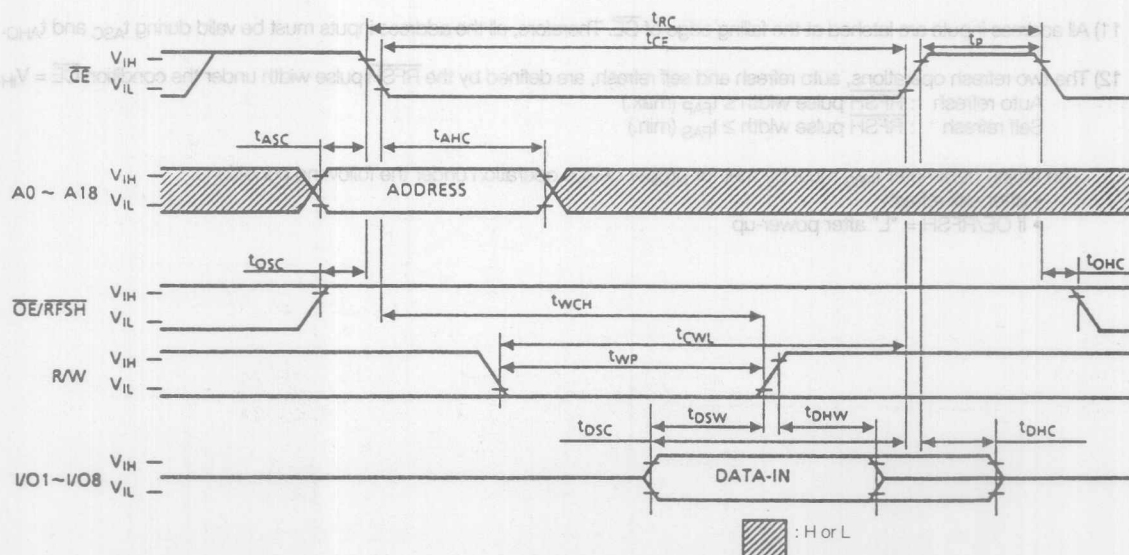
- after self refresh
- if $\overline{OE}/\overline{RFSH} = "L"$ after power-up

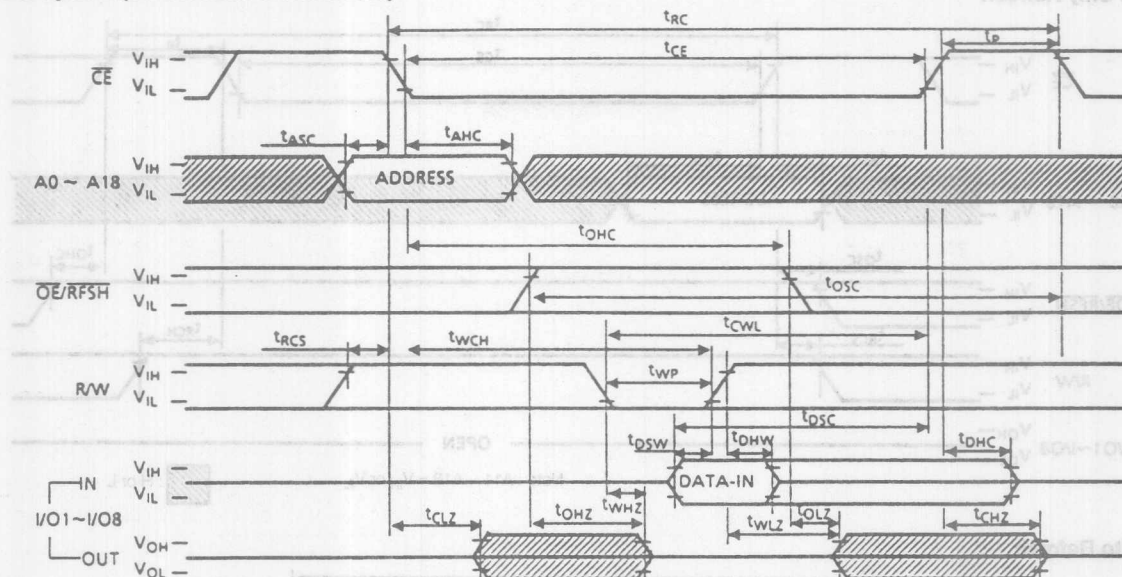
Timing Waveforms

Read Cycle

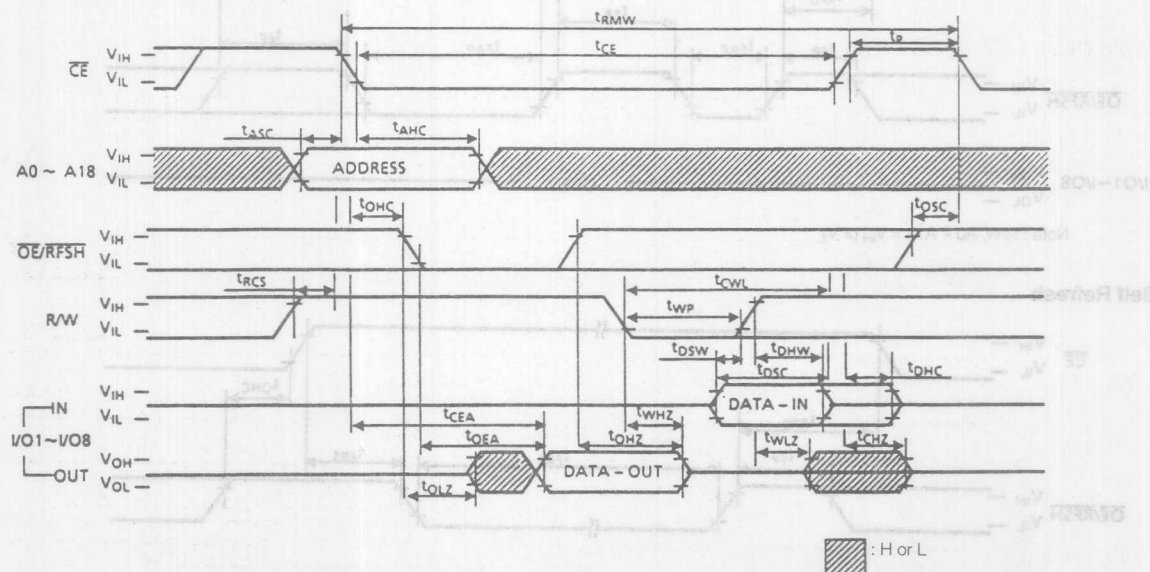


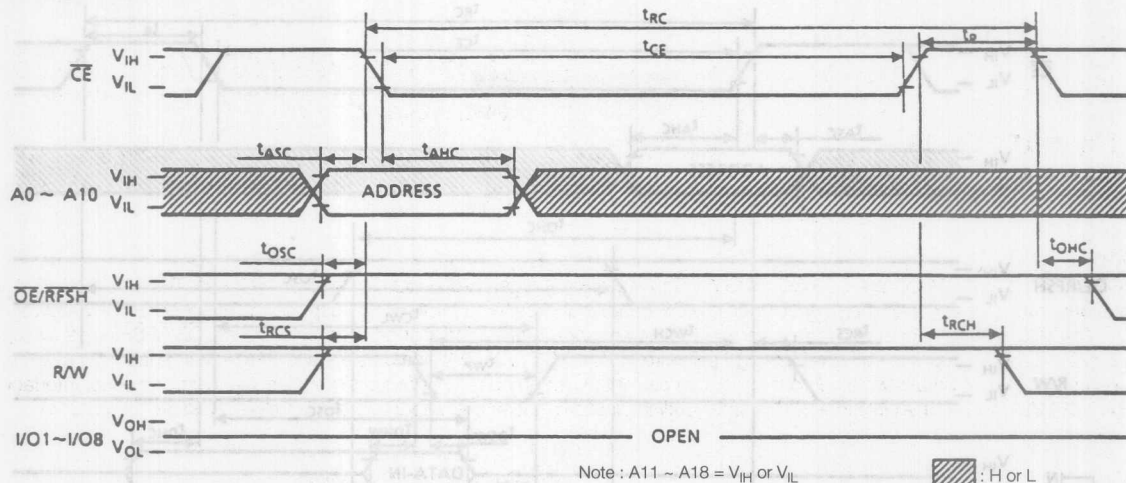
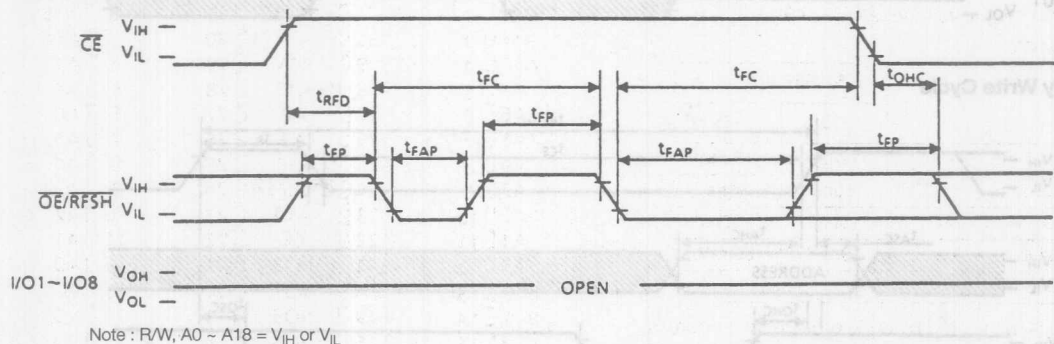
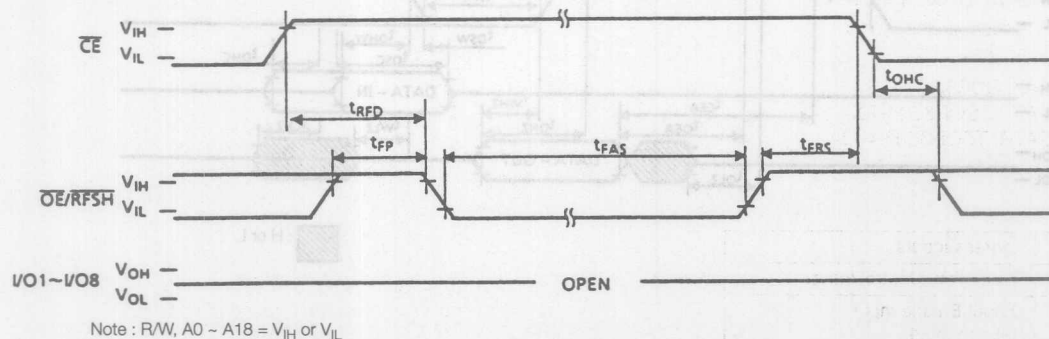
Write Cycle 1 ($\overline{\text{OE}}$ Fixed High)



Write Cycle 2 (\overline{OE} Clocked or Fixed Low)

Read Modify Write Cycle



\overline{CE} Only Refresh**Auto Refresh****Self Refresh**

TC51V8512AF/AFT/ATR-12/15

PRELIMINARY

SILICON GATE CMOS

524,288 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC51V8512AF is a 4M bit high speed CMOS pseudo static RAM organized as 524,288 words by 8 bits. The TC51V8512AF utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC51V8512AF operates from a single 3.0V power supply. Refreshing is supported by a refresh (OE/RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC51V8512AF features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

The TC51V8512AF is available in a 32-pin small outline plastic flat package, and a thin small outline package (forward type, reverse type).

Features

- Organization: 524,288 words x 8 bits
- Low voltage function: 3.0V±10%
- Data retention supply voltage: 2.0V ~ 3.3V
- Fast access time

	TC51V8512AF Family	
	-12	-15
t _{CEA} \overline{CE} Access Time	120ns	150ns
t _{OE} \overline{OE} Access Time	60ns	80ns
t _{RC} Cycle Time	190ns	230ns
Power Dissipation	99mW	66mW
Self Refresh Current	3.0V	40μA

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 2048 refresh cycles/32ms
- Package
 - TC51V8512AF: SOP32-P-525
 - TC51V8512AFT: TSOP32-P-400
 - TC518V512ATR: TSOP32-P-400A

Pin Connection (Top View)

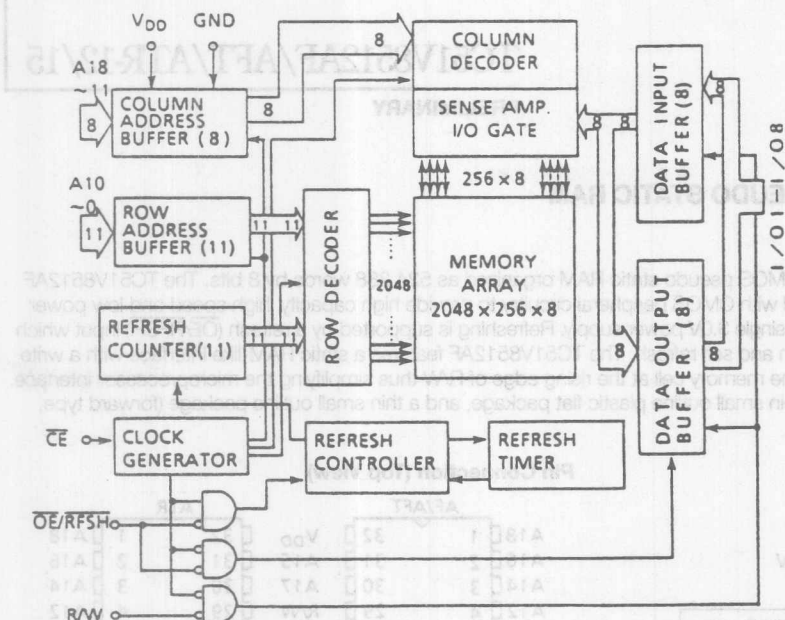
AF/AFT				ATR			
A18	1	32	V _{DD}	32	ATR	1	A18
A16	2	31	A15	31		2	A16
A14	3	30	A17	30		3	A14
A12	4	29	R/W	29		4	A12
A7	5	28	A13	28		5	A7
A6	6	27	A8	27		6	A6
A5	7	26	A9	26		7	A5
A4	8	25	A11	25		8	A4
A3	9	24	OE/RFSH	24		9	A3
A2	10	23	A10	23		10	A2
A1	11	22	\overline{CE}	22		11	A1
A0	12	21	I/O8	21		12	A0
I/O1	13	20	I/O7	20		13	I/O1
I/O2	14	19	I/O6	19		14	I/O2
I/O3	15	18	I/O5	18		15	I/O3
GND	16	17	I/O4	17		16	GND

Pin Names

A0 ~ A18	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}/RFSH$	Output Enable Input Refresh Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O8	Data Inputs/Outputs
V _{DD}	Power
GND	Ground

SYMBOL	ITEM	RATING	UNIT	NOTES
V _{in}	Input Voltage	-1.0 ~ 7.0	V	
V _{out}	Output Voltage	-1.0 ~ 7.0	V	
V _{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T _{amb}	Operating Temperature	0 ~ 70	°C	
T _{stg}	Storage Temperature	-55 ~ 150	°C	
T _{solder}	Soldering Temperature • Time	260 • 10	°C • sec	
P _D	Power Dissipation	800	mW	
I _{out}	Short Circuit Output Current	50	mA	

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	$\overline{OE}/RFSH$	R/W	A0 ~ A18	I/O1 ~ 8
Read		L	L	H	V*	OUT
Write		L	*	L	V*	IN
\overline{CE} only Refresh		L	H	H	V*	HZ
Auto/Self Refresh		H	L	*	*	HZ
Standby		H	H	*	*	HZ

H = High level input (V_{IH})L = Low level input (V_{IL})* = V_{IH} or V_{IL} V* = At the falling edge of \overline{CE} , all address inputs are latched. At all other times, the address inputs are ***.

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	2.7	3.0	3.3	V	2
V_{IH}	Input High Voltage	2.1	—	$V_{DD} + 0.5$	V	
V_{IL}	Input Low Voltage	-0.5	—	0.7	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 3V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC} \text{ min.}$	120ns version	—	20	30	mA 3,4
		150ns version	—	15	20	
I_{DDs1}	Standby Current $\overline{CE} = V_{IH}$, $\overline{OE}/\overline{RFSH} = V_{IH}$	—	—	0.5	mA	
I_{DDs2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$, $\overline{OE}/\overline{RFSH} = V_{DD} - 0.2V$	—	—	40	μA	
I_{DDf1}	Self Refresh Current (Average) $\overline{CE} = V_{IH}$, $\overline{OE}/\overline{RFSH} = V_{IL}$	—	—	0.5	mA	
I_{DDf2}	Self Refresh Current (Average) $\overline{CE} = V_{DD} - 0.2V$, $\overline{OE}/\overline{RFSH} = 0.2V$	—	—	40	μA	
I_{DDf3}	Auto Refresh Current (Average) $\overline{OE}/\overline{RFSH}$ cycling: $t_{FC} = t_{FC} \text{ min.}$	120ns version	—	20	30	mA 3
		150ns version	—	15	20	
I_{DDf4}	\overline{CE} only Refresh Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC} \text{ min.}$	120ns version	—	20	30	mA 3
		150ns version	—	15	20	
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = $0V$	—	—	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disabled ($\overline{CE} = V_{IH}$ or $\overline{OE}/\overline{RFSH} = V_{IH}$ or $R/W = V_{IL}$), $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level $I_{OH} = -100\mu\text{A}$	$V_{DD} - 0.2$	—	—	V	
V_{OL}	Output Low Level $I_{OL} = 100\mu\text{A}$	—	—	0.2	V	

Capacitance* ($V_{DD} = 3V$, $T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A18)	—	5	pF
C_{I2}	Input Capacitance (\overline{CE} , $\overline{OE}/\overline{RFSH}$, R/W)	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 3V±10%) (Notes: 5, 6, 7)

SYMBOL	PARAMETER	-120		-150		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	190	—	230	—		
t _{RMW}	Read Modify Write Cycle Time	250	—	290	—		
t _{CE}	CE Pulse Width	120	10,000	150	10,000		
t _p	CE Precharge Time	70	—	80	—		
t _{CEA}	CE Access Time	—	120	—	150		
t _{OEA}	OE Access Time	—	60	—	80		
t _{CLZ}	CE to Output in Low -Z	20	—	20	—		
t _{OLZ}	OE to Output in Low -Z	0	—	0	—		
t _{WLZ}	Output Active from End of Write	5	—	5	—		
t _{CHZ}	Chip Disable to Output in High-Z	0	30	0	30	8	
t _{OHZ}	OE Disable to Output in High-Z	0	30	0	30	8	
t _{WHZ}	Write Enable to Output in High-Z	0	30	0	30	8	
t _{OSC}	OE Setup Time Referenced to CE	0	—	0	—	8	
t _{OHC}	OE Hold Time Referenced to CE	15	—	15	—	8	
t _{RCS}	Read Command Setup Time	0	—	0	—		
t _{RCH}	Read Command Hold Time	0	—	0	—	ns	
t _{WP}	Write Pulse Width	35	—	35	—		
t _{WCH}	Write Command Hold Time	70	—	70	—		
t _{CWL}	Write Command to CE Lead Time	35	—	35	—		
t _{DSW}	Data Setup Time from R/W	30	—	30	—	9	
t _{DSC}	Data Setup Time from CE	30	—	30	—	9	
t _{DHW}	Data Hold Time from R/W	0	—	0	—	9	
t _{DHC}	Data Hold Time from CE	0	—	0	—	9	
t _{ASC}	Address Setup Time	0	—	0	—	10	
t _{AHC}	Address Hold Time	25	—	25	—	10	
t _{FC}	Auto Refresh Cycle Time	190	—	230	—		
t _{RFD}	RFSH Delay Time from CE	70	—	80	—		
t _{FAP}	RFSH Pulse Width (Auto Refresh)	80	8,000	80	8,000	11	
t _{FP}	RFSH Precharge Time	40	—	40	—	11	
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	8,000	—	11	
t _{FRS}	CE Delay Time from RFSH (Self Refresh)	250	—	300	—	11	
t _{REF}	Refresh Period (2048 cycles, A0 ~ A10)	—	32	—	32	ms	
t _T	Transition Time (Rise and Fall)	3	50	3	50	ns	

Notes:

- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DDO} , I_{DDF3} , and I_{DDF4} depend on the cycle time.
- 4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.
- 7) Measured with a load equivalent to 1 TTL load and 100pF.
- 8) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 9) For write cycles, the input data is latched at the earlier of R/W or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 10) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
- 11) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.
 Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

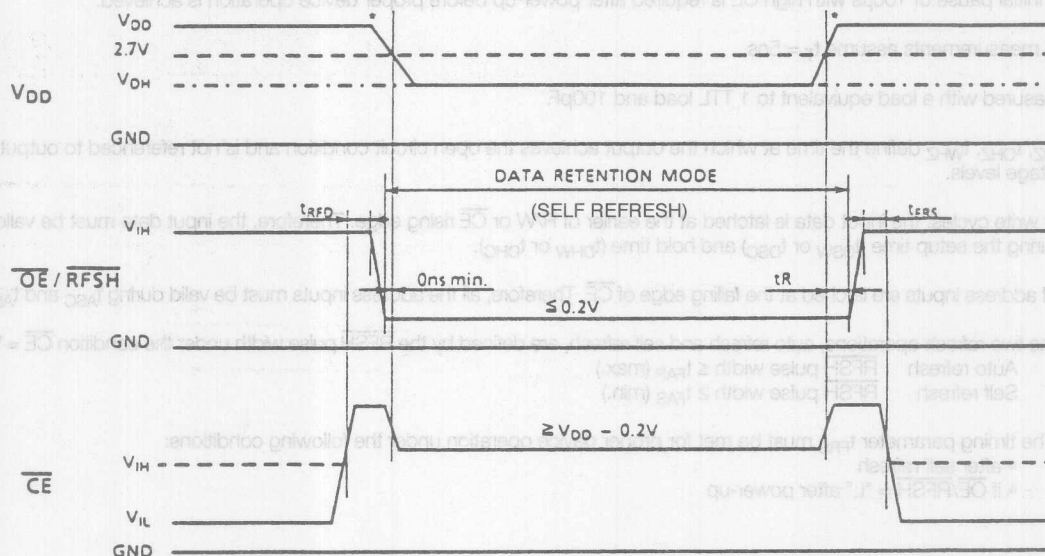
The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

- after self refresh
- if $\overline{OE}/\overline{RFSH} = "L"$ after power-up

Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	3.3	V
I_{DDF2}	Self Refresh Current	—	20	40	μA
t_R	Recovery Time	5	—	—	ms

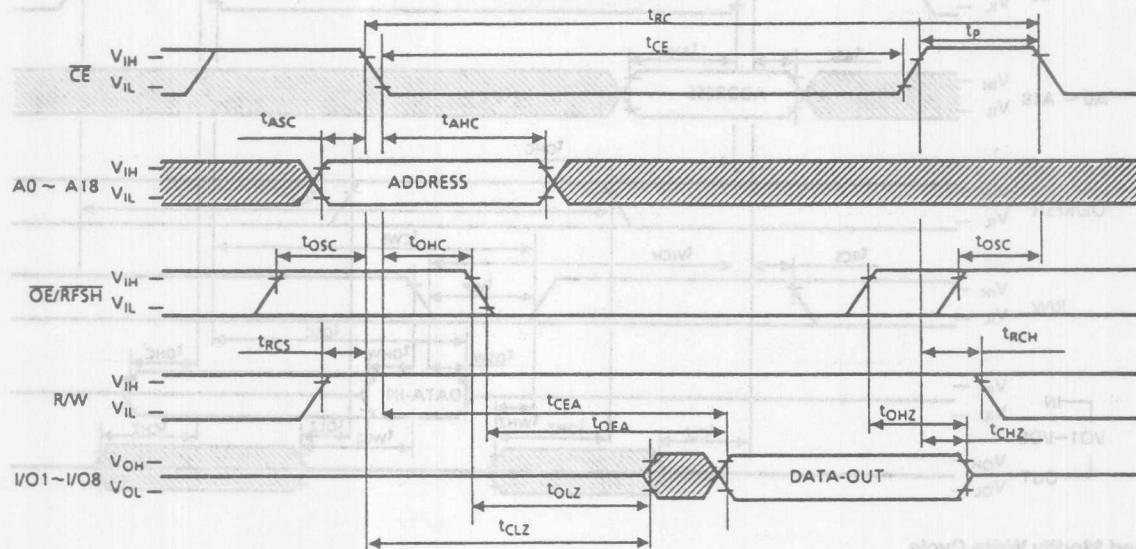
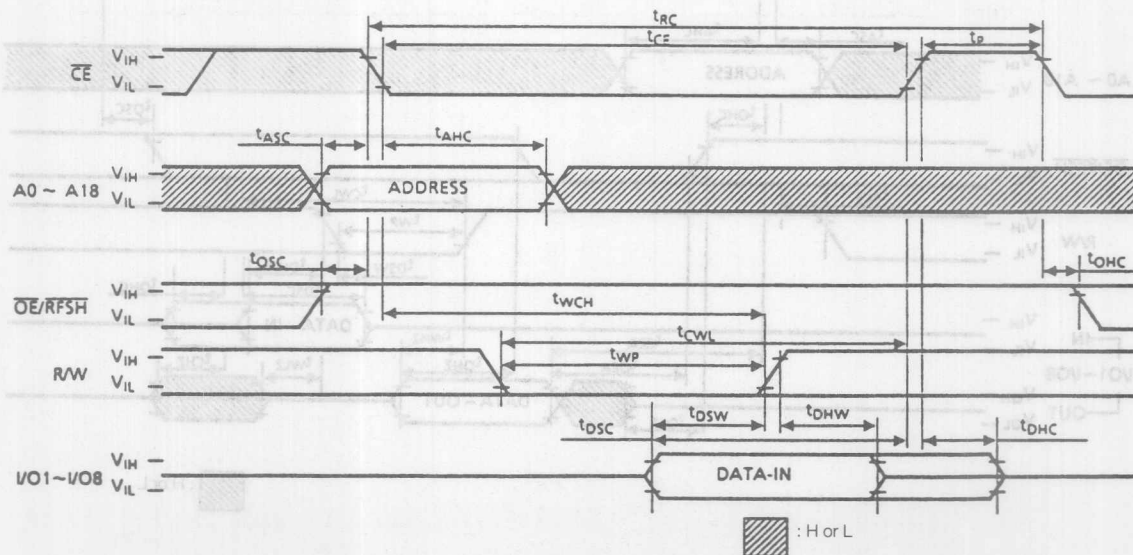
*The rising and falling slope of V_{DD} must be more than 50ms for proper device operation (20ms/V).

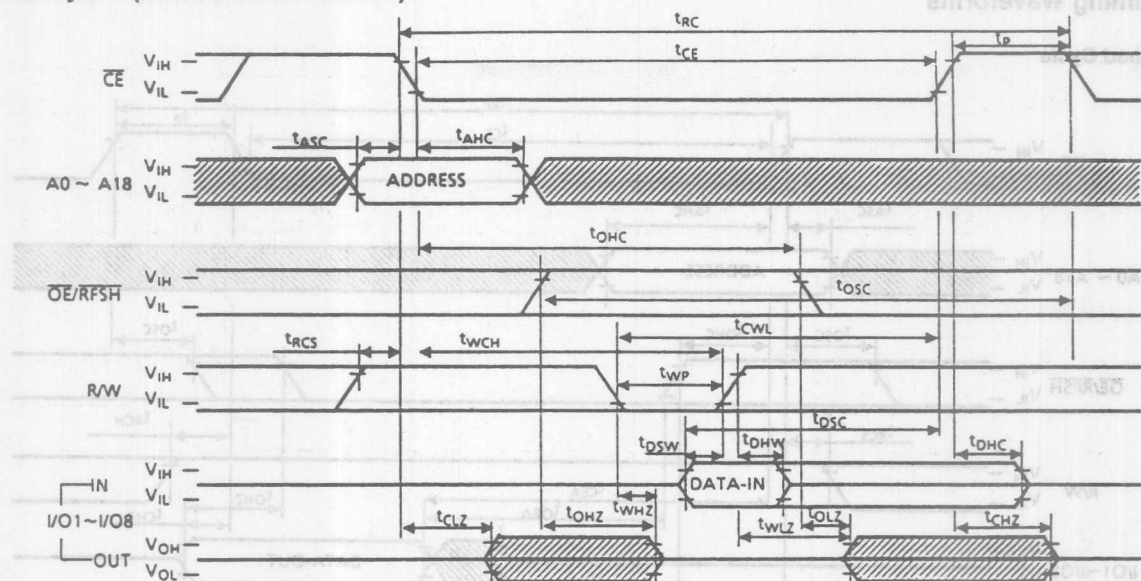


Notes: R/W, A0 ~ A18 = V_{IH} or V_{IL} .
 I_{DDF1} is applicable when $\overline{OE}/\overline{RFSH} = V_{IL}$ (max.), $\overline{CE} = V_{IH}$ (min.).

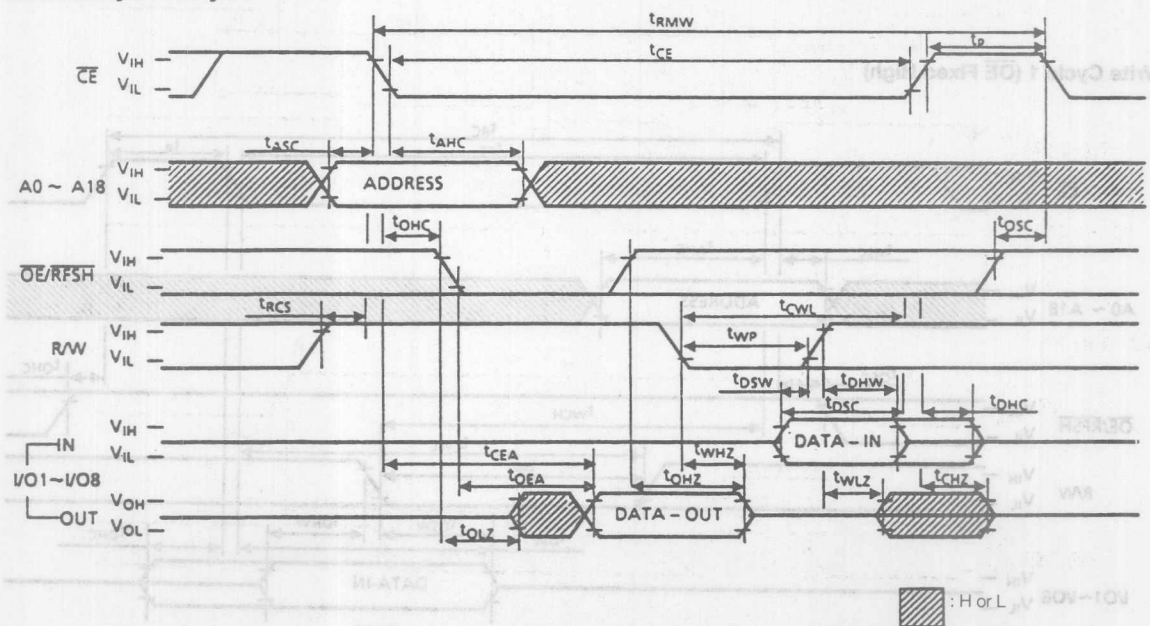
Timing Waveforms


Read Cycle

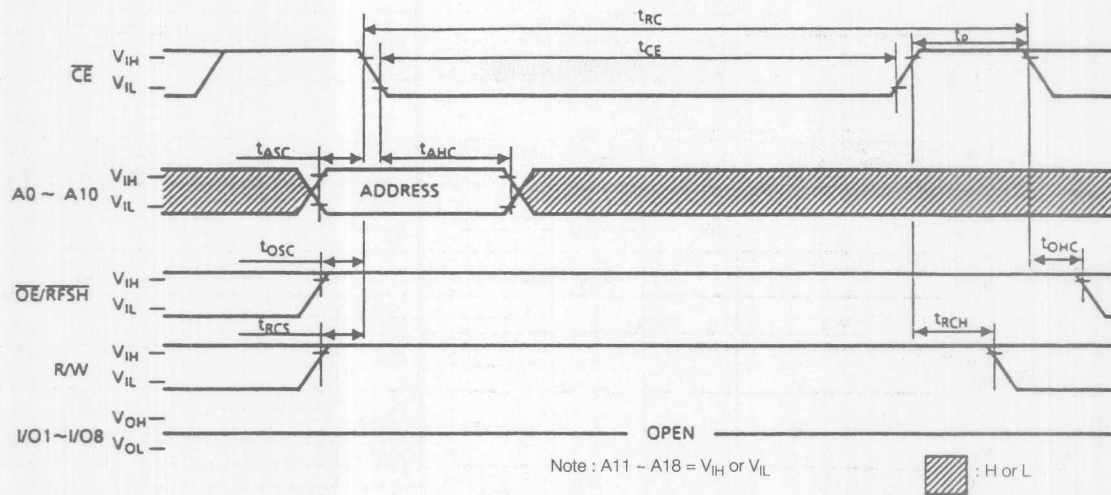
Write Cycle 1 (\overline{OE} Fixed High)

Write Cycle 2 (\overline{OE} Clocked or Fixed Low)

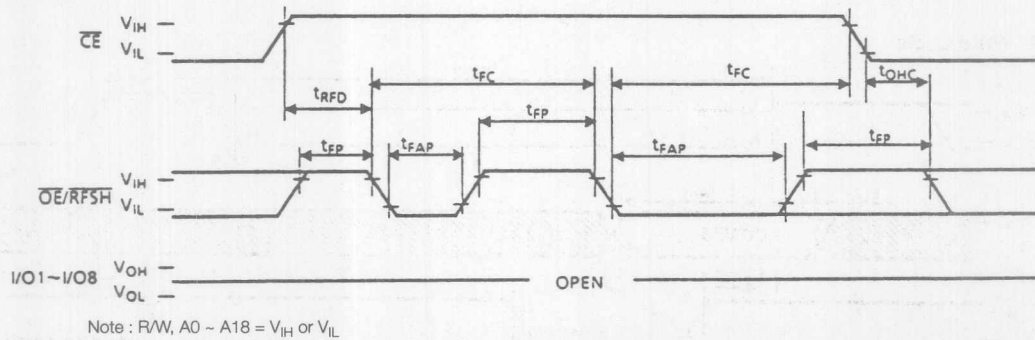
Read Modify Write Cycle



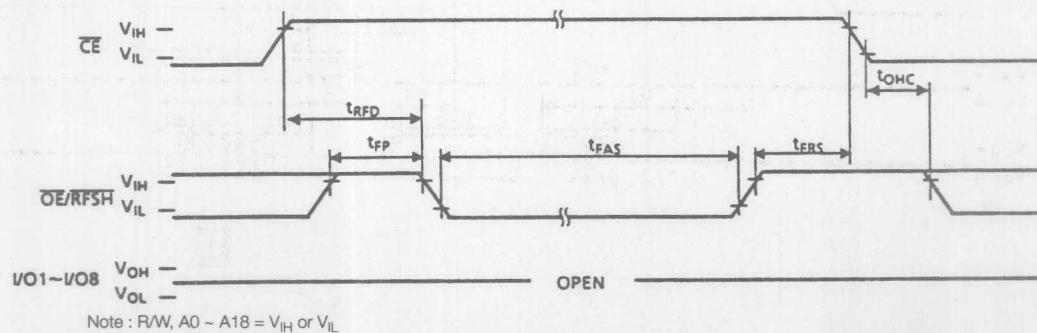
 : H or L

$\overline{\text{CE}}$ Only Refresh

Auto Refresh

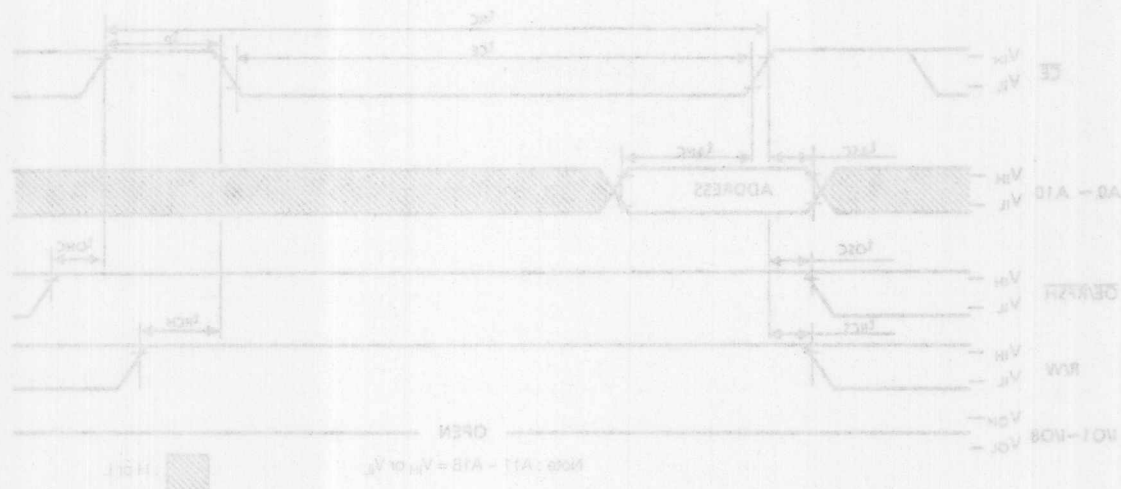


Self Refresh

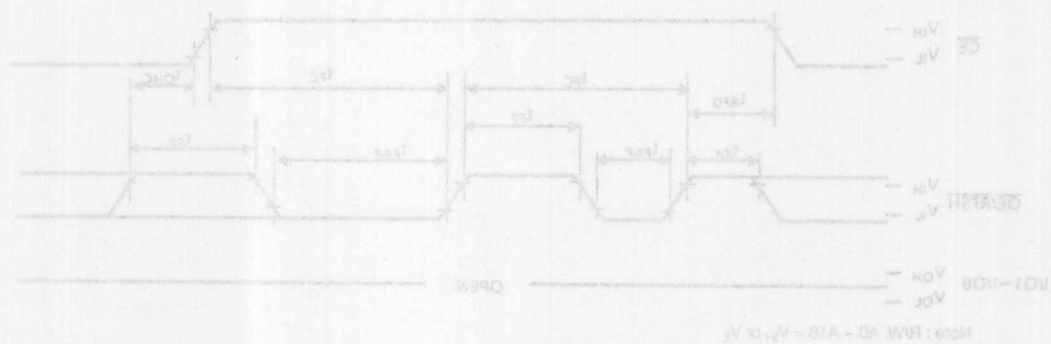


Notes

CE Only Refresh



Auto Refresh



Self Refresh

